A comparative study of defect energy distribution and its impact on degradation kinetics in GeO_2/Ge and SiON/Si pMOSFETs

J. Ma, W. Zhang, J. F. Zhang, B. Benbakhti, Z. Ji, J. Mitard, H. Arimura

***Abstract*— High mobility germanium (Ge) channel is considered as a strong candidate for replacing the Si in pMOSFETs in near future. It has been reported that the conventional power-law degradation kinetics of Si devices is inapplicable to Ge. In this work, further investigation is carried out on defect energy distribution, which clearly shows that this is because the defects in GeO_2/Ge and SiON/Si devices have different physical properties. Three main differences are: 1) Energy alternating defects (EAD) exist in Ge devices but insignificant in Si; 2) The distribution of as-grown hole traps (AHT) has a tail in the Ge band gap but not in Si, which plays an important role in degradation kinetics and device lifetime prediction; 3) EAD generation in Ge devices requires the injected charge carriers to overcome a 2nd energy barrier, but not in Si. Taking the above differences into account, the power law kinetics of EAD generation can be successfully restored by following a new procedure, which can assist in the Ge process/device optimization.**

***Index Terms*—Ge MOSFETs, Al_2O_3/GeO_2/Ge, NBTI, power law, lifetime prediction, High-k, Hole traps, Defects, Positive charges, Threshold voltage degradations, Instability.**

I. INTRODUCTION

The down-scaling of Si CMOS technology is approaching its physical limit [1]. Germanium, due to its high intrinsic hole mobility, is considered as one of the strong candidates to replace Si in MOSFETs for future technology nodes [2-11]. Two advanced gate stack fabrication approaches have been demonstrated [3-5], and high hole mobility has been reported [6-8]. One approach is with Al_2O_3/GeO_2 and the other is with HfO_2/SiO_2/Si-cap. Both are deposited on top of the Ge channel. With the Si-capped device it has been reported that bias induced degradation can be lower than its Si counterpart [8]. GeO_2/Ge devices, on the other hand, offer higher mobility for both p and n MOSFETs [9]. However, threshold voltage degradation in GeO_2/Ge devices is a severe and pressing issue and still poorly understood, currently impeding the progress for its commercial application [10-11].

It has been speculated that the degradation in GeO_2/Ge device is caused by hole trapping at low energy levels [8]. However, detailed information of these hole traps, such as the energy distribution, the differences from those in Si devices, and their corresponding degradation kinetics, have not been discussed. We have reported recently that the conventional power law degradation kinetics used for Si device, eq.1, cannot be applied to Al_2O_3/GeO_2/Ge devices with either DC or the fast pulse measurements [11,12]. It was not known how to restore the power law at that time. We speculated [11] that the defects in Ge devices can alternate their energy levels upon charging/discharging, but the defect energy distribution was not available to support the speculation at that time.

$$\Delta V_{th} = C \cdot V_{ov}^{\gamma} \cdot t^{n}, \quad (1)$$

In this work, by measuring the defect energy distribution using the technique we developed for Ge devices recently [13], we will demonstrate that the oxide defect properties are different in Ge and Si devices, based on which the power law degradation kinetics can be restored not only in GeO_2/Ge device, but also in Si-cap Ge device that has excellent reliability, enabling direct comparison of degradation kinetics and lifetime of various Ge technology to its Si counterparts. The paper is organized as follows. Devices and experiments used in this work will be described in section II. Defect differences in Ge and Si devices in energy distribution and the power law restoration method will be discussed in Section III.

II. DEVICES AND EXPERIMENTS

The GeO_2/Ge device gate dielectric stack used in this work is shown in Fig. 1a. 1.2 nm GeO_2 was prepared by exposing clean Ge grown directly on Cz–Si wafers to minimize interface states, and 4 nm Al_2O_3 was then produced by molecular beam deposition in the same chamber [14], resulting in a total SiO_2 equivalent oxide thickness of 2.35 nm for the stack. Although Al_2O_3 only has a modest dielectric constant, it can suppress the evaporation of GeO and, in turn, the deterioration of GeO_2/Ge interface [15]. The channel length used in this work is typically 1 μm and the width is 10 μm. The device used is a TaN/TiN metal gate pMOSFET. It has been reported that Ge pMOSFETs based on this process have shown record high hole mobility and outperformed the ITRS requirements [16].

The standard 'stress-and-sense' procedure [17, 18] was used to measure the threshold voltage shift. After certain stress times, ΔV_{th} was extracted from the Vg shift at a constant I_s=100×W/L nA at V_d= -100 mV [19]. In this work, fast pulse measurement time is t_m=5 μs to minimize the recovery. Temperature is either RT or 125 °C. The electric field over the interfacial GeO_2 layer was calculated from Eox=(Vg-Vth)×3.9/(6×EOT), where EOT is the SiO_2 capacitance equivalent thickness and the GeO_2 has a dielectric constant of 6 [20].

The defect energy distribution is measured after the stress by reducing |V*g*| gradually from |V*gstress*| to a range of lower discharge biases, |V*discharge,i*|, using the waveform in Fig. 1b. The discharging under each |V*discharge*| was monitored periodically by the measurement pulses. The Vth shift, ΔVth, was measured until the discharge completes at each bias, before |V*discharge*| is reduced further. The measured amount of

Manuscript received MM DD, 2015. This work was supported by the Engineering and Physical Science Research Council of UK under the grant no. EP/I012966/1, EP/L010607/1 and EP/M006727/1. The review of this article was arranged by Editor X.Y.

J. Ma, W. Zhang (email: W.Zhang@ljmu.ac.uk), J. F. Zhang, B. Benbakhti, Z. Ji are with the School of Engineering, John Moores University, Liverpool L3 3AF, U.K. J. Mitard and H. Arimura are with IMEC, Leuven B3001, Belgium.

effective trapping during the discharge, ΔNox=Cox×ΔVth/q, is shown in Figs. 1c against the energy levels corresponding to each V*discharge*. The energy distribution of these discharged defects is given by the differentiation of ΔNox against E, ΔDox=|*d*(ΔNox)/*d*E|, as shown in Figs. 1d. Detailed evaluation and verification of the energy distribution measurement can be found in refs. [13, 17, 21, 22]. Impact of interface states generation has been taken into account. Devices used in this work are summarized in Table 1.

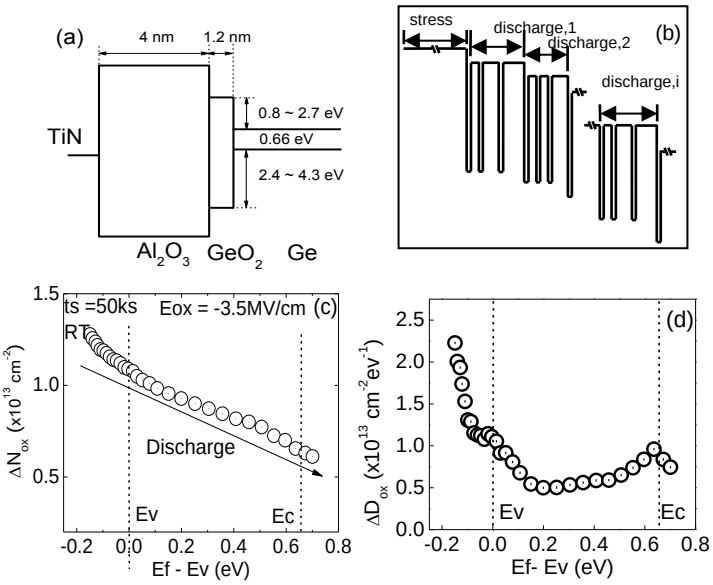

Fig. 1 (a) Schematic energy band diagram and structure of GeO_2/Ge device. (b) Typical waveform used for defect energy distribution measurement. (c) The effective density of positive charges against energy levels in GeO_2/Ge device measured during the discharge. (d) The energy distribution of positive charge density obtained from the differentiation of (c) by ΔDox=|*d*(ΔNox)/*d*E|.

TABLE 1 Gate stacks and extracted power exponents for Si and Ge Samples

(1) 2.3nm plasma-N SiON/Si (125°C: n=0.20, m=16.1, γ=3.22)
(2) 4nm Al_2O_3/1.2nm GeO_2/Ge (RT: n=0.20, m=14.4, γ=2.88; 125°C: n=0.24, m=10.9, γ=2.62)

III. RESULTS AND DISCUSSIONS

A. Differences in defect energy distribution in Ge and Si

Figs. 2a&b and c&d compare the density and energy distributions of positive charge measured after various stress levels in Ge and Si devices, respectively. At the first inspection, the shape of defect distributions in both devices appears similar, abeit the degaration is much larger in Ge devices. Significantly more defects in Ge device remain charged at the end of the measurable energy range, which are located above Ge Ec. The defect distribution below Ev in both devices hardly change with the stress level, as shown in Fig.2b&d. This suggests that the defects below Ev are as-grown hole traps (AHT) that exist in fresh device and do not increase with stress. Those defects created by stress are above Ev in both devices, as the peaks increase with stress time, and more defects cannot be discharged in Ge. More differences can be observed upon further inspection. In Fig.2d, for Si, as-grown defects are below Ev and generated defects are above Ev, indicating they are well separated in energy. In Fig.2b, for Ge, no such separation at Ev is observed, and AHTs exist above Ge Ev within the Ge band gap. It should be noted that such difference is not caused by the large difference in trapping density, as the AHT is also observed in the band gap in Si-cap Ge device, which has less defects than its Si counterpart.

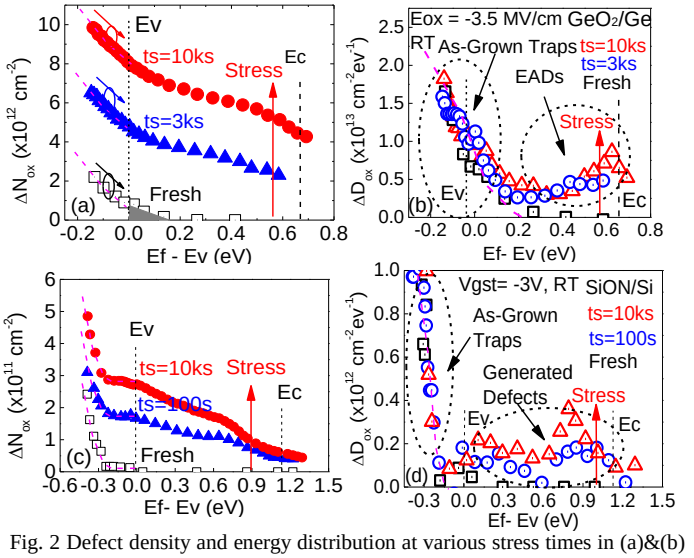

Fig. 2 Defect density and energy distribution at various stress times in (a)&(b) GeO_2/Ge device and (c)&(d) SiON/Si device. The black square symbols were obtained on a fresh device with a charging time of 5 ms for Ge and 1 sec for Si to minimize the generation.

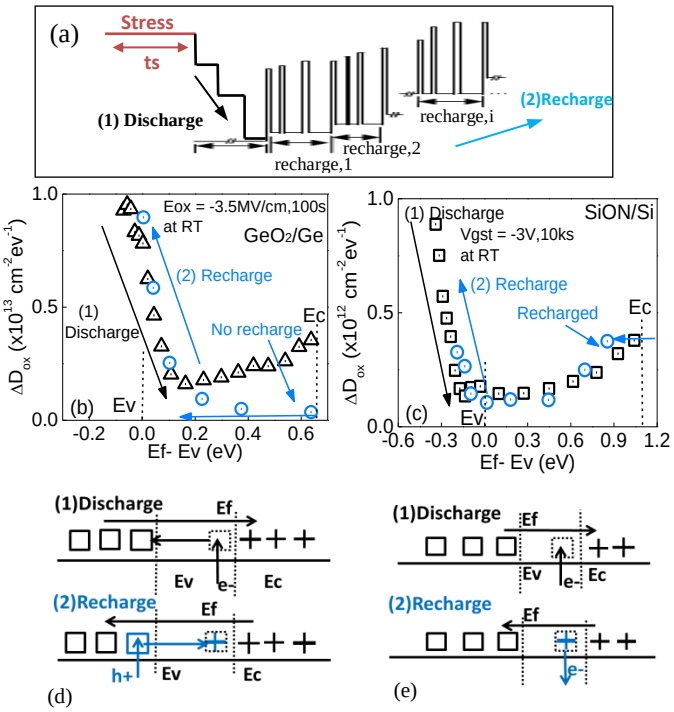

Fig. 3 Different defect behaviour during recharge: (a) Vg waveform during discharge and recharge (b) Negligible recharge in Ge when biased in the upper half of Ge bandgap. This is because (d) EADs are above Ev once positively charged, and return to fresh states below Ev after discharged, so that it can only be recharged when EL is near Ge Ev. (c) Recharge in Si starts once EL is lowered near Ec because (e) neutralized GDs in Si devices stay at high EL, allowing electrons tunnelling back from the defect to Si. The solid horizontal lines indicate the oxide/semiconductor interface. The rectangles are bulk hole traps either empty or filled with holes (+). The 'vertical arrows' indicate the capture/emission of holes (h+)/electrons (e-).

To further investigate the differences in defects, energy distributions are obtained on stressed device, first during the

defects discharge, and then recharge was conducted by sweeping the energy level backwards. Recharging time is 5k sec per bias step for both devices. The test procedure is given in Fig. 3a. As shown in Fig. 3b, traps in GeO_2/Ge device cannot be recharged until the charging energy level (EL) is near Ge Ev. In contrast, Si device in Fig. 3c shows a different behavior: defects in upper half of Si band gap can be recharged.

The above differences can be well explained by the presence of energy alternating defects (EAD) in GeO_2/Ge device, which is insignificant in Si devices. As illustrated in Fig. 3d, the energy level (EL) of EAD alternates with its charge status: it shifts back to below Ev when neutralized by an electron during the discharge, and move to above Ge Ev when it is positively re-charged. Since EADs in Ge devices will return to their fresh states after neutralization, recharging EAD only takes place when bias reaching Ev, the same as in a fresh device.

In contrast, as shown in Fig. 3e, the EL of the generated defects (GD) in Si is kept well above Ev of Si, either charged or neutral. Recharge in Si starts once EL is swept lower, as electrons tunnel back to substrate from the defect when it is above Ef.

The above analysis can be further supported by examining the effect of temperature during recharging. As shown in Fig. 4a&c, the defects were discharged at 125 ^{o}C. Temperature was then either remained at 125 ^{o}C or switched to room temperature (RT) for the recharge. In Ge devices, recharging behavior does not change with temperature, and there is no re-charge in the top half of Ge band gap. This is because the defect has returned to below Ev when it was neutralized during discharge, as illustrated in Fig. 3d. It can only be recharged when Ef is near or below Ge Ev, so that there is no re-charge when Ef is well above Ev at either 125 ^{o}C or RT, as shown in Fig. 4b.

For Si device, however, Fig. 4c shows that the positive recharging becomes higher when temperature is switched from 125 ^{o}C to RT. This is because, in contrast to Ge device, the defects neutralized at 125 ^{o}C during discharge can maintain their high EL, as shown in Fig.3e. When temperature is reduced to RT, the electrons at the high EL in Si reduce due to lower thermal energy and can no longer keep the defect neutralized, as shown in Fig. 4d, resulting in the increase in Fig. 4c [23-28].

The above model of defect energy alternating with charging status is supported by the first-principle calculation in Al_2O_3 and ab initio calculations in GeO_2 [29-31], suggesting that EADs are intrinsic in Al_2O_3/GeO_2/Ge structure.

B. Difference in the tail of as-grown hole traps (AHT) in band gap

As shown in Fig. 2b, AHTs in Si devices are typically below the Ev of Si and separated from the generated defects above the Ev. Fig. 5a shows that no tail of AHT is observed in Si bandgap, no matter which direction the energy level was swept. Since sweeping energy level from high to low was used in Si devices [12], it is referred to as 'Si-method' here. For Ge, as shown in Fig.2a, however, AHTs and EADs are not clearly separated. In order to measure the AHTs accurately, Fig. 5b compares the AHT measured in a fresh device by sweeping energy level (EL) in both directions.

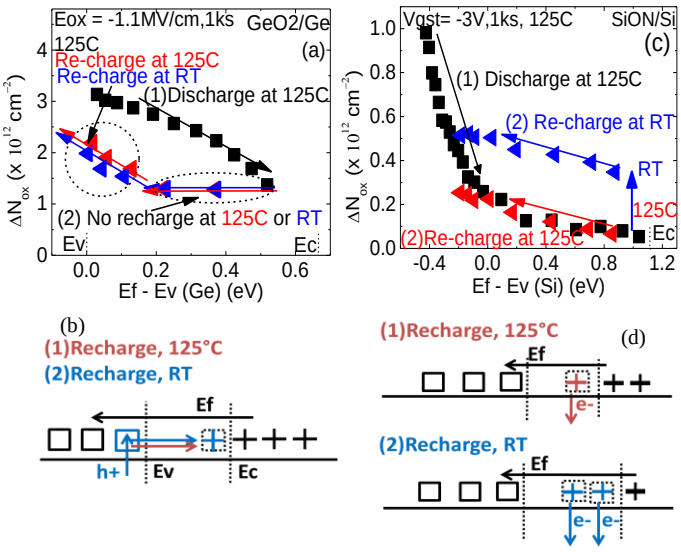

Fig. 4 Recharge under different temperatures (a) Negligible recharge in Ge when biased in the upper half of Ge bandgap at both RT and 125 ^{o}C, supporting (b) that EADs return to fresh states below Ev after discharged. (c) Recharge in Si clearly rises when lowering temperature from 125 ^{o}C to RT because (d) both changed and neutralized GDs remain at high energy level.

AHTs below Ge Ev agree when measured in both sweeping directions, but there is a 'tail' above Ge Ev, and the tail size changes when the sweeping direction is reversed. The tail is smaller when sweeping from high to low because of incomplete charging due to lower hole density above Ev and the limited charging time used during the sweeping, hence underestimate the AHTs. Sweeping energy level from low to high overcomes this artefact, therefore, and is referred to as 'Ge-method' used in this work. Fig. 5b also shows that charging and discharging of AHTs are not affected by temperatures ranging from RT to 125 ^{o}C.

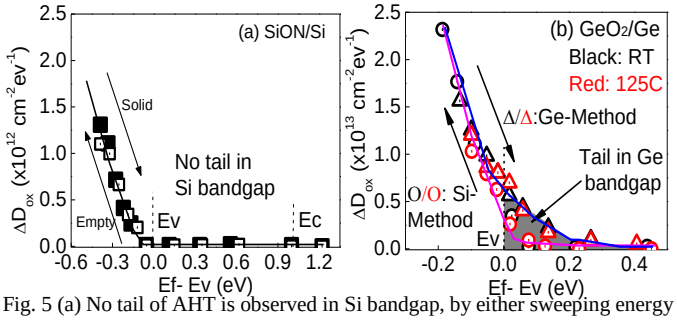

Fig. 5 (a) No tail of AHT is observed in Si bandgap, by either sweeping energy level from high to low (Si-method) or from low to high (Ge-Method). (b) A tail of AHTs in Ge band gap is observed, which is smaller when sweeping from high to low. AHTs below Ge Ev are independent of sweeping directions. AHT charging/discharging is independent of temperature. Fresh devices are used here and the charging time is 5 ms for Ge and 1 sec for Si to minimize generation.

In order to show that this tail is indeed a part of AHTs, charging and recharging the tail are carried out on a fresh device and a stressed-then-discharged device using the waveform in Fig. 3a, respectively. Fig. 6b clearly shows that the same tail above Ev is observed after the recharge reaches saturation, regardless of stress levels, supporting that the recharge is indeed due to AHT and not by the stress, and the difference in Fig. 5b is caused by incomplete recharging with the Si-method. This provides a reliable method for

extracting the accurate amount of AHTs above Ge Ev.

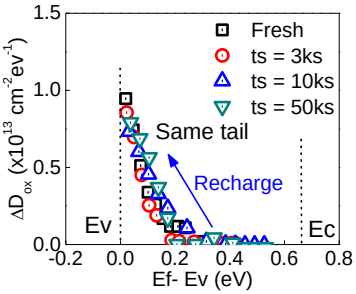

Fig.6 The same tail above Ev is recharged after different stress time, which also agrees with that in fresh device measured with the Ge-method as in Fig.5b, supporting they are AHTs.

C. Difference in energy barrier for defect generation

A further difference between the defects in Si and Ge devices can be seen in the comparison of defect energy distributions after continuous stress and stresses interrupted by recoveries. Each device is stressed either by a continuous stress of 1000 seconds, or by a short stress of 100 μs followed by a short recovery of 100 μs at Vg= 0V, which is repeated 10^7 times to give the same effective stress time of 1000 seconds as the continuous stress.

As shown in Fig. 7a, for Si devices, AHTs and GDs below the recovery EL, E(Vg_rec), can hardly be filled by the short stresses with recovery. More interestingly, the remaining GDs above the recovery EL generated under both stress conditions in Si agree well, indicating that in Si the effective defect generation depends only on the effective stress time, regardless of whether the stress being interrupted by recoveries, agreeing with previous works [26, 33]. For Ge device, as shown in Fig. 7(b), however, more defects are generated by the continuous stress even above the recovery EL. This 'additional EAD generation' cannot be explained by the generation mechanism in Si device.

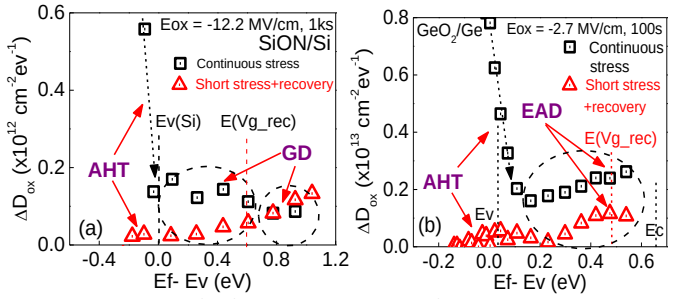

Fig.7 A comparison of defect energy distributions after a continuous stress time of 1000 sec and after 10^7 short stresses with period of 100 μs, each followed by a short recovery period of 100 μs at Vg_rec= 0 V. (a) Si device, showing good agreement when compared above the recovery EL. (b) Ge device, additional generation for continuous stress when compared after discharge at the same recovery bias.

We propose a three-well model for the energy alternation in Ge devices and then use it to explain the additional generation by continuous stress, as shown in Fig. 8. The energy level of the 2nd well is relatively shallow and below Ev, and a hole from the 1st well in Ge substrate can be injected and trapped in it. Only after this trapping, it can proceed to a relaxation process that changes its orbital configuration and forms the deep 3rd well [8]. The EADs trapped in the 3rd well is proportional to the charge density in the 2nd well, N_h. Under continuous stress, N_h is relatively high, leading to more holes trapped in the 3rd well. Under dynamic stress/recovery test, the shallow level of 2nd well means that its trapped holes during the short stress can be efficiently discharged during the subsequent recovery, so that N_h can only reach a low balanced level. The smaller N_h in turn leads to less EADs in the 3rd well. The trapping in the 3rd well is more stable due to its deep energy level. For Si devices, there is no 'additional generation' because generated defects (GD) are trapped in the 2nd well, and the charged GD does not go through further relaxation under the test conditions used here, so that the 3rd well is not developed. It has been reported that there is a GeOx layer between Ge and GeO2 [34], which can play a role in the three-well structure

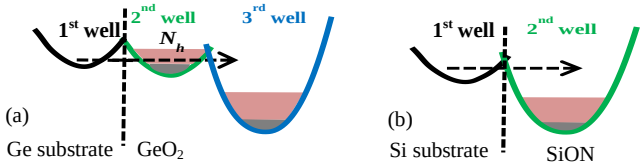

Fig.8 (a) Three-well model in Ge: generation of energy alternating defects in 3rd well with deeper energy level requires holes first being injected into 2nd well and then overcome the 2nd barrier, through a relaxation process. (b) Double-well model in Si: generated defects are at deep energy level and do not involve energy alternation.

To further support that AHTs and EADs in GeO_2/Ge devices are two different groups of defects, temperature effect is explored under different stress fields, as shown in Fig. 9. The initial degradation is dominated by filling AHTs, which is insensitive to temperature from RT to 125 °C, agreeing with Fig. 5b. In contrast, charging EADs is thermally accelerated and does not saturate, further supporting the AHT and EAD model.

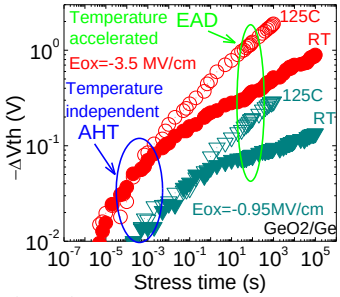

Fig.9 AHTs are filled first during stress and are temperature independent, whilst EADs are the opposite.

D. Restore power law and enable degradation extrapolation in Ge devices

When EADs were extracted by subtracting the AHTs without considering the tail in Ge band gap, power-law was restored, as shown in Fig. 10a. However, the power exponent 'n', i.e. the slope of the lines, varies substantially with Eox. The voltage power exponent, 'γ', at different stress times is also different, as shown in Fig. 10b. This prevents the reliable prediction of device lifetime when extrapolating from stress bias to the operation bias [12, 18].

To explain the reduced 'n' at lower |Eox| in Fig.10a, we investigated the impact of neglecting the AHT tail above Ge Ev on the power law. As shown in Fig.11, the tail has little effect for the EAD generation kinetics at a high stress Eox. However, at a low stress Eox, removing the tail can change the power exponent, n, significantly. This is because the amount of charges in the tail is relatively large when compared with the small EAD generation at

low Eox. Without subtracting them, they push up the apparent EAD at short time, resulting in an apparent small 'n'.

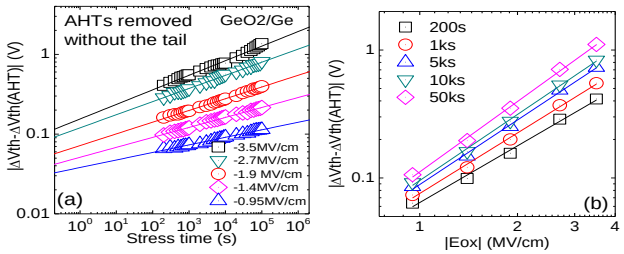

Fig.10 Removing AHT without considering the tail in Ge band gap leads to a varying slope: (a) time power exponent and (b) voltage power exponent.

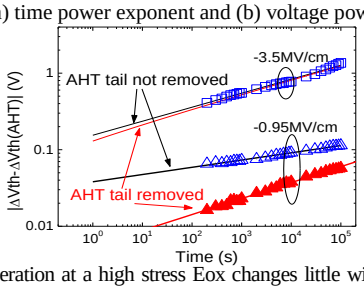

Fig.11 EAD generation at a high stress Eox changes little with or without the AHT tail above Ge Ev. At a low stress Eox, however, removing the AHT tail can increase the power exponent, n, significantly.

After subtracting all AHTs including the tail, 'n' and 'γ', become time and bias independent, as shown by the parallel lines in Figs. 12a and 12b, respectively. AHT-tail above Ev plays a crucial role for the accurate evaluation of 'n' and 'γ', therefore. This highlights the pitfall of blindly extracting 'n' by fitting the raw degradation kinetics data without separating different types of defects, and the importance of subtracting the correct amount of AHTs before fitting. A constant 'n' and 'γ' by the best-fit of the data enables lifetime prediction by extrapolating from high stress bias to low operational bias. The procedure is summarized in Table 2 and Fig. 13 below. Vg_op and Eox_op are the bias and oxide electric field at the targeted operation condition, respectively. τ is the extrapolated lifetime at a given bias.

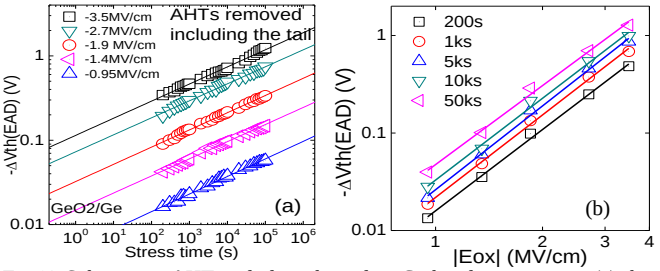

Fig.12 Subtracting AHT including the tail in Ge band gap restores (a) the constant time power exponent, and (b) the constant voltage power exponent.

TABLE 2 Procedure for lifetime prediction

i. Find the correct ΔVth(AHT) under each stress and operation bias, by using the Ge-Method, including the tail in band gap (Fig.5b)
ii. Get the ΔVth(GD or EAD, τ) = ΔVth(total, τ) - ΔVth(AHT)
iii. Extract τ from fitting ΔVth(GD or EAD) vs stress time at each bias with the power law (Fig. 13a)
iv. Estimate τ at operating condition (Vg_op=-1.5V/Eox_op=-5.2MV/cm in this example) by extrapolating τ against Vg/Eox (Fig. 13b)
v. Estimate the operation Vg/Eox for lifetime = 10 years, by using the τ in step (iv) at different operating/stress voltage/Eox (Fig.14).

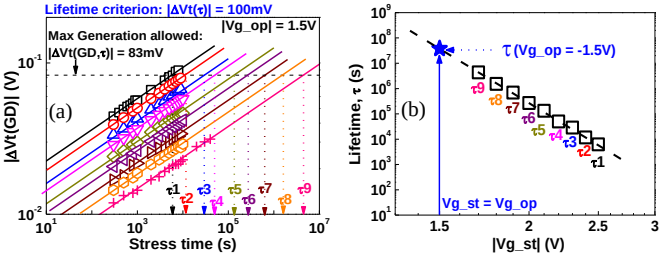

Fig.13 The lifetime prediction method procedure. A Si device is used here as a demonstrator for predicting the lifetime at a Vg_op= -1.5 V. The lifetime criterion is in total |ΔVt(τ)| =100 mV, giving a corresponding GD: ΔVth(GD,τ)= ΔVth(τ)-Δ(AHT) =100-17=83 mV [33].

Fig.14 compares the lifetime extrapolation of different devices/processes at 125 °C using the above procedure. Power law based degradation extrapolation is restored for both Si and Ge technologies. Optimization is clearly needed for GeO_2/Ge, agreeing with the observation in ref. [8]. The method works for both 125 °C and RT (not shown). The extracted exponent values for both SiON/Si and GeO_2/Ge samples are summarized in table 1.

It has been shown in previous Sections that Ge sample behaves differently from that in Si samples. For Si devices, recent studies show that the defects in oxides have a complex behaviour, involving defect-hydrogen interaction [35]. The detailed mechanisms are not known. Our speculation is that defect generation [36] is a process of converting a hydrogen-related precursor into a defect in SiON [37, 38] and the structure becomes permanently different from that of the precursor. After neutralization, the GD structure remains different and will not return to that of its precursor.

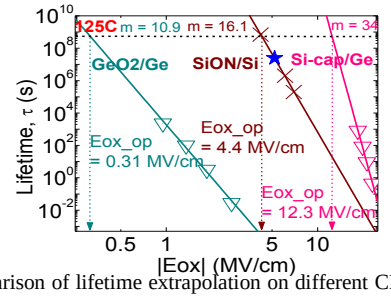

Fig.14 A comparison of lifetime extrapolation on different CMOS processes by the new method in this work at 125 °C. Power law is restored in all cases, enabling process evaluation and comparison. The blue star in Si/ SiON corresponds to the τ at Vg_op= -1.5 V extracted in Fig. 13b.

For Ge, this work demonstrated that EADs in Ge device are clearly different from the generated defects (GD) in Si device, yet both follow the power law. Our speculation is that the charging of EAD also involves some kinds of structure relaxation [39]. The power law could originate from a distribution of the barriers between energy wells [40]. The relaxed-structure, however, is not permanent [15]. Following neutralization, it returns to its original precursor, so that its energy level also reverts to its original one. Further evidences are needed to verify the above speculations.

GeO_2/Ge clearly needs further optimization for being used in commercial product, because of its poor performance caused by the very high defect density of the GeO_2/Ge structure when compared to that of SiO_2/Si. It should be noted that the phenomenon of energy alternation is also observed in Si-cap Ge devices, which has a better reliability than not only GeO_2/Ge

devices, but also SiON/Si devices, as shown in Fig. 14. The detailed analysis on Si-cap devices is not given in this work due to space limitation. The technique developed in this work is therefore applicable to a variety of Ge and Si technologies, regardless the amount of degradation. It allows restoring the power law and enabling the lifetime evaluation and, in turn, assisting Ge CMOS process development. The quality of Ge-based or other channel/ gate interfacial structures that are yet to be integrated in future device can be tested and subsequently improved by using the proposed methodology.

IV. Conclusions

This work compares the defect energy distributions in Ge and Si devices and demonstrated that their defect properties are different. The energy alternating defects (EAD) are generated in Ge, but insignificant in Si devices. The as-grown hole traps have a tail above Ev for Ge, but not Si devices. The generation of EAD in Ge requires the injected charge carriers to overcome a 2nd energy barrier, which results in additional generation under uninterrupted stress conditions.

Based on the above detailed study on defect differences, EADs can be experimentally separated from AHTs. The importance of removing the AHT tail is demonstrated for restoring power law degradation kinetics with constant time/Eox power exponents. This method enables the prediction of lifetime and the maximum operation bias for Ge devices, and the direct comparison among different CMOS technologies and, in turn, assisting in process/device development and optimization.

References

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, T. Yuan, and W. Hen-Sum Philip, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259-288, 2001.

[2] M. Caymax, G. Eneman, F. Bellenger, C. Merckling, A. Delabie, G. Wang, R. Loo, E. Simoen, J. Mitard, B. De Jaeger, G. Hellings, K. De Meyer, M. Meuris, and M. Heyns, "Germanium for advanced CMOS anno 2009: a SWOT analysis," in *IEDM Tech. Dig.*, 2009, pp. 1-4.

[3] C. Chi On, and K. C. Saraswat, "Advanced germanium MOSFET technologies with high-k gate dielectrics and shallow junctions," in *ICICDT*, 2004, pp. 245-252.

[4] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L. A. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEDM Tech. Dig.*, 2006, pp. 1-4.

[5] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High performance GeO_2/Ge nMOSFETs with source/drain junctions formed by gas phase doping," in *IEDM Tech. Dig.*, 2009, pp. 1-4.

[6] B. Kaczer, J. Franco, J. Mitard, P. J. Roussel, A. Veloso, and G. Groeseneken, "Improvement in NBTI reliability of Si-passivated Ge/high-k/metal-gate pFETs," *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1582-1584, 2009.

[7] R. Zhang, P. C. Huang, N. Taoka, M. Takenaka, and S. Takagi, "High mobility Ge pMOSFETs with 0.7 nm ultrathin EOT using HfO_2/Al_2O_3/GeO_x/Ge gate stacks fabricated by plasma post oxidation," in *VLSI Symp. Tech. Dig.*, 2012, pp. 161-162.

[8] J. Franco, B. Kaczer, P. J. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser, and G. Groeseneken, "Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO_2/HfO_2 pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks," in *IEDM Tech. Dig.*, 2013, pp. 15.12.11-15.12.14.

[9] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High performance GeO2/Ge nMOSFETs with source/drain junctions formed by gas phase doping," in IEDM Tech. Dig., 2009, pp. 1-4.

[10] G. Groeseneken, M. Aoulaiche, M. Cho, J. Franco, B. Kaczer, T. Kauerauf, J. Mitard, L. A. Ragnarsson, P. Roussel, and M. Toledano-Luque, "Bias-temperature instability of Si and Si(Ge)-channel sub-1nm EOT p-MOS devices: Challenges and solutions," in *Proc. IPFA*, 2013, pp. 41-50.

[11] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, X. F. Zheng, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. R. Chalker, "Characterization of Negative-Bias Temperature Instability of Ge MOSFETs With GeO_2/Al_2O_3 Stack," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1307-1315, 2014.

[12] Z. Ji, S. F. W. M. Hatta, J. F. Zhang, J. G. Ma, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, "Negative bias temperature instability lifetime prediction: Problems and solutions," in *IEDM Tech. Dig.*, 2013, pp. 15.16.11-15.16.14.

[13] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, "Energy Distribution of Positive Charges in Al_2O_3/GeO_2/Ge pMOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 160-162, 2014.

[14] F. Bellenger, B. De Jaeger, C. Merckling, M. Houssa, J. Penaud, L. Nyns, E. Vrancken, M. Caymax, M. Meuris, T. Hoffmann, K. De Meyer, and M. Heyns, "High FET Performance for a Future CMOS GeO_2-Based Technology," *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 402-404, 2010.

[15] K. Kita, S. K. Wang, M. Yoshida, C. H. Lee, K. Nagashio, T. Nishimura, and A. Toriumi, "Comprehensive study of GeO_2 oxidation, GeO desorption and -metal interaction GeO_2-understanding of Ge processing kinetics for perfect interface control," in *IEDM Tech. Dig.*, 2009, pp. 1-4.

[16] R. Zhang, P. C. Huang, J. C. Lin, N. Taoka, M. Takenaka, and S. Takagi, "High-Mobility Ge p- and n-MOSFETs With 0.7-nm EOT Using HfO_2/Al_2O_3/GeO_x/Ge Gate Stacks Fabricated by Plasma Postoxidation," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 927-934, 2013.

[17] X.F.Zheng, W.D.Zhang, B.Govoreanu, J.F. Zhang, J. van Houdt. "A discharge-based multi-pulse technique (DMP) for probing electron trap energy distribution in high-k materials for Flash memory application, IEEE International Electron Devices Meeting (IEDM), pp.127-130, 2009.

[18] Z. Ji, L. Lin, J. F. Zhang, B. Kaczer, and G. Groeseneken, "NBTI Lifetime Prediction and Kinetics at Operation Bias Based on Ultrafast Pulse Measurement," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 228-237, 2010.

[19] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast VT-Measurements," in *Proc. IRPS*, 2006, pp. 448-453.

[20] J. Mitard, F. Bellenger, L. Witters, D. J. B., V. B., L. Nyns, K. Martens, E. Vrancken, G. Wang, D. Lin, R. Loo, M. Caymax, K. De Meyer, M. Heyns, and N. Horiguchi, "Investigation of the electrical properties of Ge/high-k gate stack: GeO_2 VS Si-cap," *in Proc. ICSSDM*, 2011.

[21] X. F. Zheng, W. D. Zhang, B. Govoreanu, D. R. Aguado, J. F. Zhang, J. Van Houdt, "Energy and Spatial Distributions of Electron Traps Throughout SiO_2/Al_2O_3 Stacks as the IPD in Flash Memory Application", *IEEE Trans. Electron Devices*, vol. 5, No. 1, pp.288-296, 2010.

[22] S. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. Zhang, N. Soin, B. Kaczer, S. D. Gendt, and G. Groeseneken, "Energy Distribution of Positive Charges in Gate Dielectric: Probing Technique and Impacts of Different Defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745-1753, 2013.

[23] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper)," *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1883-1887, 2009.

[24] J. F. Zhang, Z. Ji, M. H. Chang, B. Kaczer, and G. Groeseneken, "Real Vth instability of pMOSFETs under practical operation conditions," in *IEDM Tech. Dig.*, 2007, pp. 817-820.

[25] J. F. Zhang, C. Z. Zhao, A. H. Chen, G. Groeseneken, and R. Degraeve, "Hole traps in silicon dioxides. Part I. Properties," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1267-1273, 2004.

[26] C. Z. Zhao, J. F. Zhang, G. Groeseneken, and R. Degraeve, "Hole-traps in silicon dioxides. Part II. Generation mechanism," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1274-1280, 2004.

[27] J. F. Zhang, M. H. Chang, and G. Groeseneken, "Effects of Measurement Temperature on NBTI," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 298-300, 2007.

[28] L. Lin, K. Xiong, and J. Robertson, "Atomic structure, electronic

structure, and band offsets at Ge:GeO:GeO_2 interfaces," *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 242902-1-242902-3, 2010.
[29] J. R. Weber, A. Janotti, and C. G. Van de Walle, "Native defects in Al_2O_3 and their impact on III-V/Al_2O_3 metal-oxide-semiconductor-based devices," *J. Appl. Phys.*, vol. 109, no. 3, pp. 033715-1-033715-7, 2011.
[30] D. Liu, Y. Guo, L. Lin, and J. Robertson, "First-principles calculations of the electronic structure and defects of Al_2O_3," *J. Appl. Phys.*, vol. 114, no. 8, pp. 083704-1-083704-5, 2013.
[31] J. F. Binder, P. Broqvist, and A. Pasquarello, "Charge trapping in substoichiometric germanium oxide," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1428-1431, 2011.
[32] L. Lin, Z. Ji, J. F. Zhang, W. Zhang, B. Kaczer, S. De Gendt, and G. Groeseneken, "A Single Pulse Charge Pumping Technique for Fast Measurements of Interface States," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1490-1498, 2011.
[33] Z. Ji, S. F. W. M. Hatta, J. F. Zhang, J. G. Ma, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, G. Groeseneken, 'Negative Bias Temperature Instability Lifetime Prediction: Problems and Solutions', International Electron Device Meeting (IEDM) 2013. Washington DC, USA, December 8–10.
[34] Molle, Alessandro, et al. "High permittivity materials for oxide gate stack in Ge-based metal oxide semiconductor capacitors." Thin solid films 518.6 (2010): S96-S103.
[35] T. Grasser, et al. "On the volatility of oxide defects: Activation, deactivation, and transformation." *Reliability Physics Symposium (IRPS), 2015 IEEE International*. IEEE, 2015.
[36] J. F. Zhang, H. K. Sii, G. Groeseneken, and R. Degraeve. "Hole trapping and trap generation in the gate silicon dioxide." *IEEE Trans. Electron Devices, vol.* 48, no. 6, pp. 1127-1135, 2001.
[37] T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *Proc. IRPS*, 2010, pp. 16-25.
[38] T. Grasser, et al. "Gate-sided hydrogen release as the origin of" permanent" NBTI degradation: From single defects to lifetimes." 2015 IEEE International Electron Devices Meeting (IEDM). IEEE, 2015.
[39] S. Baldovino, A. Molle, and M. Fanciulli, "Evidence of dangling bond electrical activity at the Ge/oxide interface," *Appl. Phys. Lett.*, vol. 93, no. 24, pp. 242105, 2008.
[40] J. S. Lee, S. R. Bishop, T. Kaufman-Osborn, E. Chagarov, and A. C. Kummel, "Monolayer Passivation of Ge(100) Surface via Nitridation and Oxidation," *ECS Trans.*, vol. 33, no. 6, pp. 447-454, 2010.

Jigang Ma received the B.Eng. and M.Eng. degrees from Xidian University, Xi'an, China, in 2009 and 2012, respectively, and the PhD Degree in microelectronics from Liverpool John Moores University (LJMU), UK in 2015. He is currently a postdoctoral research associate at LJMU and a visiting researcher at imec, Belgium. His current research interests include modelling and characterization of Emerging (resistive switching) memory devices, CMOS devices, and GaN HEMT devices.

Wei Dong Zhang received the Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2003. He is a professor of Nanoelectronics at LJMU. His current research interests include characterization and quality assessment of resistive switching and flash memory devices, CMOS devices based on Si, Ge and III-V materials, and GaN HEMT devices.

Jian Fu Zhang received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1982 and 1987, respectively. He has been a Professor of Microelectronics with Liverpool John Moores University, Liverpool, since 2001. His current research interests include the aging, variability, characterization, and modelling of nanometer-size devices.

Brahim Benbakhti received the M.Sc. and Ph.D. degrees in microwave and microtechnology from Lille University, Lille, France, in 2003 and 2007, respectively. He is currently with the Electronics and Electrical Engineering Department, Liverpool JMU. His current research interests include the reliability characterization and simulation of III-nitrides-based devices, transistor structure engineering, nanoscale III-V and Ge channel MOSFETs.

Zhigang Ji (M'04) received the Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2010. He has been a Lecturer with LJMU since 2011. His current research interests include defect characterization of CMOS devices.

Jerome Mitard After a Ph.D. in microelectronics performed at LETI/ Grenoble together with STMicroelectronics/Grenoble/France, Jérôme Mitard joined IMEC/Leuven/ Belgium, in 2007 as a device researcher working on high-mobility channel MOSFETs. He is currently team leader of the 300mm Platform Device Research team.

Hiroaki Arimura received the M.S. and Ph.D. degrees in material science and engineering from Osaka University, Japan, in 2009 and 2011, respectively. He joined imec, Belgium, as a postdoctoral researcher in 2011, and has been a senior researcher since 2013. His current research is on Ge channel devices.