

LCL Grid Filter Design of a Multi-Megawatt Medium-Voltage Converter for Offshore Wind Turbine using SHEPWM Modulation

Mikel Zabaleta, Eduardo Burguete, Danel Madariaga, Ignacio Zubimendi, Markel Zubiaga, Igor Larrazabal.

Abstract—The switching frequency of medium-voltage high power converters is limited to about 1 kHz due to semiconductor junction temperature constraint. The frequency band between the fundamental and carrier frequency is limited to a little more than one decade and the LCL filter design is usually a challenge to meet grid codes for grid connected applications. Traditional designs focus on the optimization of the filter parameters and different damping circuits. However, this design is very influenced by the modulation technique and produced low order harmonics. Widely used pulse width modulations (PWM), such as phase disposition PWM (PDPWM), produce low order harmonics that constraint the design of the filter. Selective harmonic elimination PWM (SHEPWM) can eliminate these low order harmonics, enabling a more efficient design of the LCL filter. In this paper, the LCL grid filter of a Multi-Megawatt Medium-Voltage neutral point clamped (NPC) converter for a wind turbine is redesigned using SHEPWM modulation. Experimental results demonstrate that the efficiency of the converter, filter and overall efficiency are increased compared to that obtained with PDPWM.

Index Terms—LCL filter, medium-voltage converter, selective harmonic elimination, SHE.

I. INTRODUCTION

MEDIUM voltage high power converters have usually a limited switching frequency due to semiconductor maximum junction temperature constraints. The maximum switching frequency for these converters is usually set around 1 kHz [1]. In grid connected applications, this constraint has an important influence on the design of the grid filter, which has to be optimized to meet grid codes restrictions.

LCL filter is one of the most adopted filters to be used in grid connected filters [2]. They have a resonance frequency and they provide good attenuation ratio above it. For low power converters the carrier frequency is set quite above 1 kHz, and the resonance frequency of the filter needs to be placed within a band with a lower bound set by the control

bandwidth frequency (CBWF) and an upper bound set by the first significant switching harmonics. However, for medium-voltage high power converters, this frequency band is narrow (as the CBWF and the switching frequency are relatively close), so it is hard to place the resonance frequency according to such criteria [1],[3]. Therefore, LCL filters usually require damping circuits to reduce the resonance amplifications that become more easily excited as the CBWF gets close to the switching frequency. The losses on the damping resistance of the grid filter reduce the overall efficiency of the converter.

Many papers focus on the design of the LCL filter, proposing different methods and algorithms to determine the optimal values of the components of the filter or proposing different damping circuits, to get the desired attenuation [1]-[15]. However, these proposals do not take into account the modulation technique and hence, the solution may remain suboptimal in terms of overall efficiency of the converter.

Power converters are usually controlled using pulse width modulation (PWM) techniques. Many different techniques have been proposed in the literature for multilevel converters, such as, phase shifted PWM (PSPWM), phase disposition PWM (PDPWM), phase opposite disposition PWM (PODPWM) or centered space vector PWM (CSVPWM). These techniques try to reduce the total harmonic distortion (THD) for a given switching frequency [16],[17]. Nevertheless, they produce low order harmonics, which require to be damped to meet the grid codes. As a result, the losses in the damping resistor of the filter increase, reducing the efficiency of the filter and of the whole system.

The selective harmonic elimination PWM (SHEPWM) modulation technique allows eliminating some harmonics [18]-[21], which can be selected to be the harmonics around the resonance frequency of the LCL filter to reduce the damping requirements, and hence, the losses in the damping resistor of the filter.

In this paper a LCL grid filter for a medium-voltage high power converter is redesigned using SHEPWM modulation technique (the conventional design was based on PDPWM modulation). SHEPWM is used to eliminate some undesired low order harmonics near the resonance frequency of the LCL filter. The lower damping requirements of the produced harmonics by the SHEPWM modulation lead to a more efficient design of the LCL filter. In addition, the

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The authors are with the Wind R&D Department of Ingeteam Power Technology S.A., Spain (e-mail: mikel.zabaleta@ingetteam.com; eduardo.burguete@ingetteam.com; danel.madariaga@ingetteam.com; ignacio.zubimendi@ingetteam.com; markel.zubiaga@ingetteam.com; igor.larrazabal@ingetteam.com)

switching frequency is reduced, and therefore, the switching losses of the semiconductors. As a consequence, the overall efficiency of the conversion stage will be increased, while still meeting the grid codes requirements.

In section II the converter with its parameters is described. Section III describes the previous design using PDPWM modulation technique and section IV presents the optimized new design using SHEPWM. Section V shows experimental results for both designs, which prove that the theoretical analysis is adequate.

II. CONVERTER STRUCTURE, PARAMETERS AND SPECIFICATIONS

The studied converter in this paper is a NPC three phase converter in a back to back configuration. The study of this paper is focused on the grid side converter and its scheme is shown in Fig. 1.

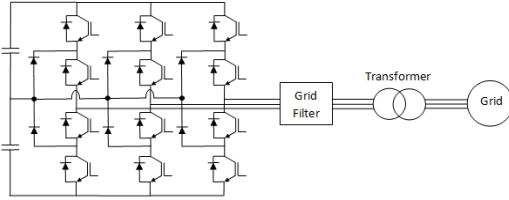


Fig. 1. Grid connected 3L-NPC converter.

The converter output is rated at 5MVA, 3.3 kV line to line at 50/60 Hz and is aimed to be used in full-conversion stages in offshore wind turbines rated 5+ MVAs. It must be able to operate at full rated power for a power factor range of (-0.9, 0.9). Table I shows the main parameters of the NPC grid side converter.

TABLE I
NPC CONVERTER SPECIFICATIONS

Parameter	Value
Line to Line Grid Voltage	3.3 kV
Grid current	875 A
Fundamental frequency	50/60 Hz
Output Power	5 MVA
Power factor	± 0.9

The LCL damping circuit can have different configurations [2],[7-9]. LCL filter with a damping resistor in series with the capacitor involves high losses in the resistor, mainly caused by the fundamental component. A damping circuit formed by a resistor (R_d) and an inductor (L_d) in parallel reduces the losses in the damping resistor, because the L_d inductor provides a new path without losses to the fundamental current component of the filter. Thus, the solution with a resistor and an inductor in parallel for the damping circuit was selected for the converter. Other configurations with more components may introduce additional benefits but the limited available footprint usually found on wind turbine applications discarded them. Fig. 2 depicts this filter, where v_c and v_g are the converter and grid voltages respectively, L_c is the inductance of the converter side of the LCL filter, C_f is the capacitor of the LCL filter and L_g is the grid side inductance of the filter, that

comprises both the short-circuit impedance of the grid and that of the transformer. The LCL filter with R_d and L_d damping circuit will be denoted as LCL-RL filter throughout this paper.

The converter is required to fulfill the German technical guideline for “Generating plants connected to the medium-voltage network” [22] (usually referred to as VDEW in papers, for example in [1]). The requirements for the grid current harmonics defined by VDEW for a 10 kV grid are summarized in Table II.

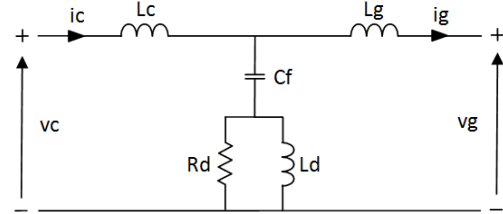


Fig. 2. Grid per-phase LCL filter with RL damping circuit.

TABLE II
GRID CURRENT DISTORTION LIMITS ACCORDING TO VDEW

Harmonic order v (odd), μ (even)	$i_{\mu,v \text{ zul}}$
5	0.058
7	0.082
11	0.052
13	0.038
17	0.022
19	0.018
23	0.012
25	0.010
$25 < v < 40$	$0.01 \cdot 25/v$
$\mu < 40$	$0.06/\mu$
$\mu, v > 40$	$0.18/\mu$

The values of the Table II were interpreted as described by (1) in accordance to some medium-voltage converters leader manufacturers, where i_k is the maximum permissible current harmonic expressed as a percentage of rated current and SCR is the grid's short circuit ratio (the ratio of grid's shortcircuit current to the generator's rated current). For this paper, SCR is assumed to be 40.

$$i_k = i_{\mu,v \text{ zul}} \text{ SCR} \sqrt{3} \quad (1)$$

III. PDPWM CONVERTER DESIGN

In a first step the converter was designed with PDPWM modulation technique, which presents good THD values [17] and is commonly adopted by the industry in grid connected applications. The LCL-RL filter was designed in order to meet VDEW requirements.

A. PDPWM Generated Harmonic Distortion

The PDPWM modulation disposes $n-1$ carriers one above the other, being n the number of voltage levels of the converter. For the NPC $n=3$, and so, PDPWM technique uses two carriers, one above the other. Like in a two level converter, a third order harmonic can be injected (for example adding $-(\max+\min)/2$ [16]-[17]) to increase the linear

operation of the modulation index.

The harmonic spectrum created by the converter is analyzed using the virtual voltage harmonic spectrum (VVHS) concept [1]. The VVHS spectrum is formed by the largest harmonics of the considered modulation index range. Due to the permissible grid voltage variation, a modulation index range of $m \in [0.9, 1]$ is assumed (with $m_{\max}=1.15$). Designing the LCL filter with VVHS to meet the VDEW requirements assures that no harmonic will surpass the defined limit for any modulation index.

Fig. 3 shows the described PDPWM modulation for $m=1$ and $f_{\text{sw}}=1140\text{Hz}$ and the VVHS that this PDPWM modulation produces for a modulation index range of $m \in [0.9, 1]$.

The largest harmonics produced by this PDPWM modulation are located around twice the frequency of the carriers (20% of the fundamental). However, lower order harmonics are also produced. The harmonics around the carrier frequency have a magnitude around 5-7% of the fundamental. Furthermore, even lower order harmonics are produced, such as, the 11th harmonic, whose magnitude is around 5% of the fundamental. These low order harmonics, such as 11th, are located between the switching frequency and CBWF, where the LCL filter resonance frequency usually lays.

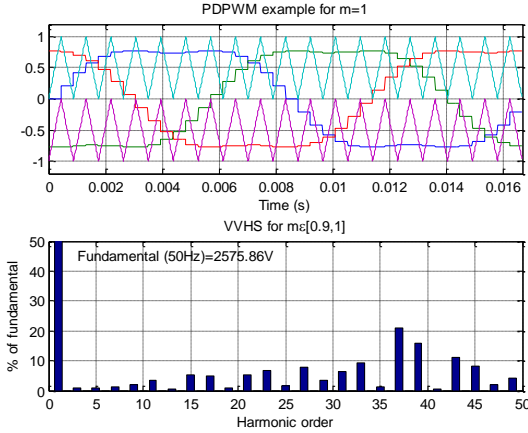


Fig. 3. PDPWM modulation technique and the produced VVHS.

B. Filter characteristics

The aim of the design of the filter is to meet the requirements for the grid current. The transfer function that relates the grid current (ig) with the voltage produced by the modulation (vc), is the ig/vc transfer function, which is developed in (2) and (3) for LCL and LCL-RL filters respectively.

Fig. 4 illustrates an example of the previous transfer functions (the parameters of the filters are those from Table V, but the damping resistance of the LCL-RL filter is assumed to be ∞). The LCL has one resonance frequency (ω_r), whereas the LCL-RL filter has one resonance frequency (ω_r) and one anti-resonance frequency (ω_{ar}).

The anti-resonance frequency of the LCL-RL filter is determined by (4),

$$\omega_{ar} = \sqrt{\frac{Ld - 4 Rd^2 Cf}{4 Rd^2 Cf^2 Ld}} \quad (4)$$

The resonance frequency of the LCL filter is determined by (5),

$$\omega_r = \sqrt{\frac{Lc + Lg}{Lc Lg Cf}} \quad (5)$$

The calculation of the resonance frequency of the LCL-RL filter is more complex. The upper and lower bounds for this frequency can be obtained considering zero the damping resistor (using (5)) and considering an infinite damping resistor (using (6)) as depicted in Fig. 4. So, the resonance frequency will be located between these two values depending on the actual value of the damping resistor.

$$\omega_{r_o} = \sqrt{\frac{1}{\left(\frac{Lc Lg}{Lc + Lg} + Ld\right) Cf}} \quad (6)$$

The gain at the resonance frequency of the LCL-RL filter decreases when the value of the damping resistor of the filter is reduced (increasing the damping).

The low order harmonics such as the 11th, are highly increased by the resonance if it is not properly damped. In order to meet the VDEW code, the VVHS produced by the PDPWM requires a low damping resistor to reduce the gain of the ig/vc transfer function around the resonance frequency.

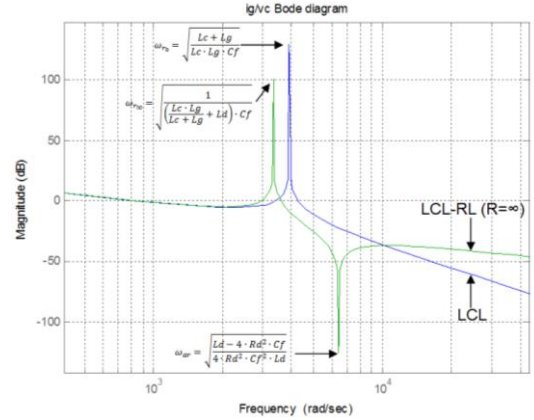


Fig. 4. $ig/vc(s)$ transfer function Bode diagram (magnitude).

C. Filter Design

The filter design is restricted by the VVHS created by the modulation and the VDEW grid code. The filter must provide enough attenuation to reduce the VVHS to acceptable values in concordance to the VDEW grid code limits. Thus, the virtual attenuation required to meet a grid code can be defined as the attenuation required by the filter to meet said grid code for the VVHS. That is, the attenuation required for the ig/vc transfer function can be calculated and compared with the ig/vc transfer function parameters of the filter. As an example, the Fig. 5 depicts the ig/vc transfer function of a LCL-RL filter (specifically, the filter of Table III) and the virtual attenuation required by the filter to meet the VDEW code.

$$\frac{ig}{vc}(s) = \frac{1}{Lc Lg Cf s^3 + (Lc + Lg) s} \quad (2)$$

$$\frac{ig}{vc}(s) = \frac{Rd Cf Ld s^2 + Ld s + Rd}{Lc Lg Ld Cf s^4 + Rd Cf (Lc Ld + Lc Lg + Lg Ld) s^3 + (Lc Ld + Lg Ld) s^2 + Rd (Lc + Lg) s} \quad (3)$$

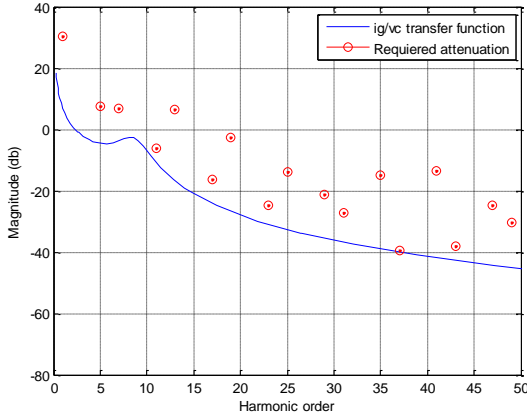


Fig. 5. $ig(s)/vc(s)$ transfer function and virtual attenuation required.

Fig. 6 shows the design process of the filter. With VVHS and VDEW restrictions, the virtual harmonic attenuation is calculated. An optimization algorithm calculates the filter parameters. This algorithm includes some design criteria like limiting the maximum switching current in the IGBTs, minimizing the energy stored in the filter and/or limiting the value of the converter side inductance (Lc) due to space constraints. Furthermore, the optimized filter has to provide the required attenuation to meet the grid code requirements.

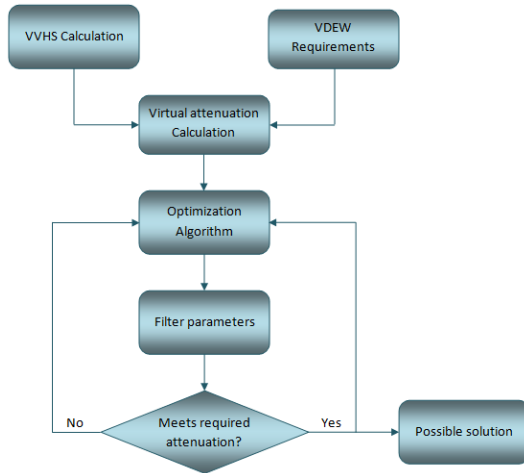


Fig. 6. Filter design flow chart.

The design process yielded to the filter values shown on Table III.

Lc	Lg	Cf	Rd	Ld
0.11 p.u.	0.059 p.u.	0.16 p.u.	0.27 p.u.	0.031 p.u.

Fig. 7 depicts the VDEW limits for the grid current and the harmonics of the grid current produced by the PDPWM

modulation with the filter calculated in Table III. It can be seen that all the maximum harmonics produced by the PDPWM modulation along the modulation range satisfy the restrictions of the VDEW grid code.

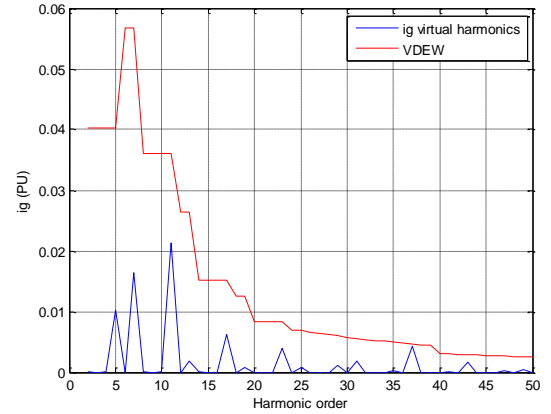


Fig. 7. Produced grid current harmonics by VVHS and VDEW limit.

Table IV lists some calculated results obtained at rated power. P_{Rd} are the losses on the damping resistor, THD is the THD of the grid current, f_{sw} is the switching frequency and ig_{max} is the peak value of the grid current including the current ripple. The losses on the damping resistor include the Ohmic losses due to the fundamental current and current harmonics. The values of the losses and the THD of Table IV are the maximum values obtained for the entire modulation index range. The peak value of the current of Table IV is the maximum value taking into account the entire modulation index range and power factor range.

P_{Rd}	THD	f_{sw}	ig_{max}
5262 W	0.96 %	1140 Hz	1346 A

IV. SHEPWM CONVERTER DESIGN

This section describes the LCL-RL filter design using SHEPWM modulation. This modulation allows using a lower damping on the filter while reducing the switching frequency. Consequently, the losses on the filter and on semiconductors are reduced, and thus, the overall efficiency of the conversion stage is increased.

There are several solutions (different switching angles that eliminate the same harmonics) for a SHEPWM once the harmonics to be eliminated are chosen [19]-[21]. The proper selection of the solutions is of vital importance to provide a smooth operation across the entire modulation index range. The procedure to select the most adequate solutions for the SHEPWM is considered out of the scope of the present paper.

A. SHEPWM Generated Harmonic Distortion

The SHEPWM modulation technique calculates the optimum switching angles along a fundamental period in order to eliminate some harmonics. The number of harmonics that this modulation can eliminate depends on the number of edges (or commutations) along the period. Different symmetries can also be used but in this paper, quarter wave symmetry is used as it allows for a faster response and a 5 edges along a quarter of period modulation is considered, yielding to 4 eliminated harmonics.

The modulation with 5 edges allows eliminating for example the 5th, 7th, 11th and 13th harmonics. Furthermore, the LCL-RL filter can be designed so that the anti-resonant frequency lays on the 17th harmonic which is the first non-eliminated harmonic that will appear in the current. Therefore, the first non triple odd harmonic that is not eliminated and does not lay on the anti-resonance frequency of the filter is the 19th harmonic.

In addition, the equivalent switching frequency of the SHEPWM modulation with 5 edges is 600 Hz (lower than the 1140 Hz of the PDPWM modulation), reducing the switching losses.

A SHEPWM modulation with more edges per period can eliminate more harmonics, but at the same time, the switching losses increase, reducing the efficiency.

The LCL-RL filter is designed so that the resonance frequency lays on the 9th harmonic (540 Hz), to ensure that no excitation is possible as the modulation eliminates all the surrounding harmonics.

Fig. 8 depicts the converter output voltage waveform of the SHEPWM defined to eliminate the desired harmonics and VVHS produced by this modulation technique for a modulation index range of $m \in [0.9, 1.0]$.

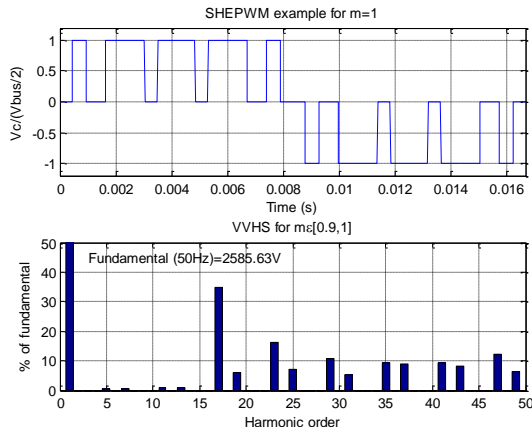


Fig. 8. Converter output waveform produced by SHEPWM modulation and the VVHS.

As Fig. 8 illustrates, the 5th, 7th, 11th and 13th harmonics have been almost eliminated. The resonance frequency of the filter will be designed to lay on the 9th harmonic and due to the previous harmonics being very small, the damping requirements of the filter can be lowered. Therefore, the damping resistor can be larger, reducing the losses on the filter. The first harmonic that appears is the 17th and it can be

seen that it is the largest harmonic, so increased attenuation at such frequency will be required.

B. Filter Design

The design process of the filter for SHEPWM modulation has two additional constraints compared to the design of the filter for PDPWM modulation. The goal behind using the SHEPWM modulation is to increase the damping resistor of the filter (lower damping) to reduce the losses on it and increase the efficiency. Due to the low damping at the resonance frequency, this has to be placed at a frequency where no harmonics are emitted by the converter, such as, 9th. For this purpose the optimization algorithm varies the parameters of the filter with the restriction that the resonance frequency is set to 9th harmonic. Furthermore, the 17th harmonic of the SHEPWM is higher than any other harmonic present both in the SHEPWM modulation and in the PDPWM modulation, so an unusually large attenuation is required. As the damping resistor has been increased, the anti-resonance frequency is mildly damped, and therefore, the anti-resonance frequency can provide the required big attenuation at the 17th harmonic.

The optimization algorithm then looks for filters that provide the required virtual attenuation and have the resonance and anti-resonance frequencies at 9th and 17th harmonics. The result of the process yielded to the filter of Table V, which has a larger damping resistance and a smaller damping inductance compared with the PDPWM filter.

TABLE V
LCL-RL FILTER FOR SHEPWM MODULATION

L_c	L_g	C_f	R_d	L_d
0.11 p.u.	0.059 p.u.	0.16 p.u.	26 p.u.	0.014 p.u.

Fig. 9 illustrates the ig/vc transfer function of the filter of Table V and the virtual attenuation required. It can be seen that the filter provides the required attenuation for all the harmonics. Fig. 10 shows the harmonics of the grid current created by the VVHS and the maximum harmonics allowed by VDEW grid code. All the harmonics created by the VVHS are smaller than the maximum allowed by the VDEW.

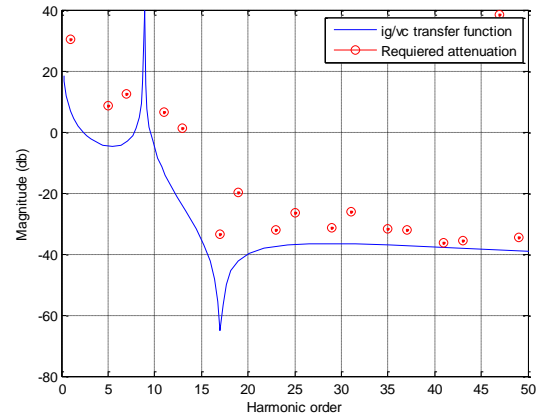


Fig. 9. $ig(s)/vc(s)$ transfer function and virtual attenuation required.

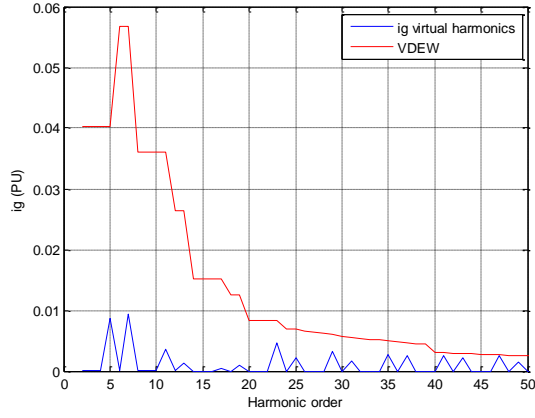


Fig. 10. Produced grid current harmonics by VVHS and VDEW limit.

Fig. 11 shows the ig/vc transfer function and the required attenuation for the SHEPWM and PDPWM. The PDPWM modulation has some low order harmonics, such as the 11th, that require attenuation due to its proximity to the resonance frequency. Even more, the neutral point control and the dead time can also produce low order harmonics [23]. If the resonance is not properly damped, these low order harmonics that are located around the resonance frequency may excite it causing over-currents in the filter components and not satisfying the grid code's requirements.

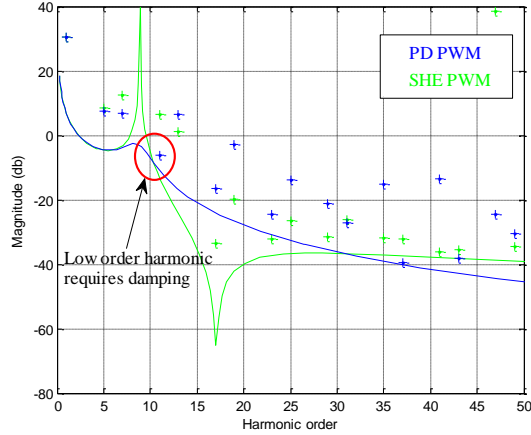


Fig. 11. $ig(s)/vc(s)$ transfer function and virtual attenuation required.

Table VI shows some calculated results obtained at rated power. The procedure to calculate them was analog to the procedure used to obtain the values of Table IV. Comparing the results from Table VI with the results from Table IV, it can be concluded that the losses in the damping resistance of the filter have been significantly reduced (from 5262 W to 429 W). In addition, the switching frequency of the SHEPWM is almost half the switching frequency of the PDPWM (from 1140 to 600 Hz), which will reduce the switching losses of the semiconductors. Additionally, the THD value has been kept similar and with good value (1.44 with SHEPWM and 0.96 with PDPWM) and the converter's peak current has been slightly increased from 1346 to 1442 A.

P_{Rd}	THD	f_{sw}	ig_{max}
429 W	1.44 %	600 Hz	1442 A

V. EXPERIMENTAL RESULTS

A medium voltage converter of Ingeteam's MV100 family was used in the experimental setup. Some characteristics of the MV100 are: 3.3 kV, 5.6kV DC-link, water-cooled, employs 3L-NPC topology and uses 4.5 kV IGBTs. The technical data of the converter can be consulted in [24].



Fig. 12. Picture of filter design for the MV100 converter: a) PDPWM and b) SHEPWM.

The converter has been tested using the two modulations, PDPWM and SHEPWM, each one with its designed filter (see Fig. 12). Fig. 13 and Fig. 14 depict voltage and current experimental waveforms on the grid side for PDPWM and SHEPWM modulations respectively when the converter delivers 5MW.

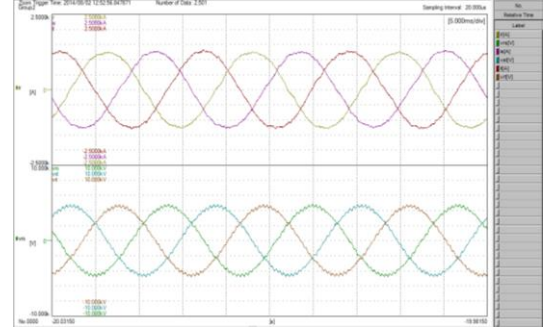


Fig. 13. Current (top) and voltage (bottom) experimental waveforms on the grid side for PDPWM modulation.

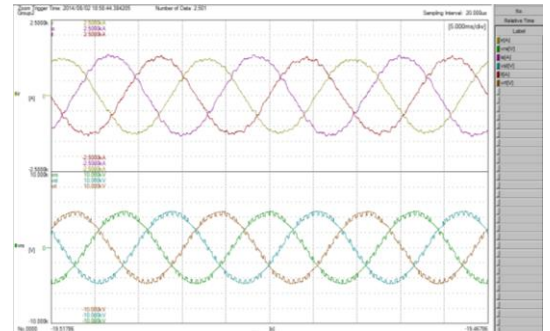


Fig. 14. Current (top) and voltage (bottom) experimental waveforms on the grid side for SHEPWM modulation.

Fig. 15 and Fig. 16 show the harmonics of the grid current of the previous experimental results and the maximum

harmonics allowed by the VDEW grid code for PDPWM and SHEPWM modulations respectively. Both configurations meet the requirements of the VDEW, as expected.

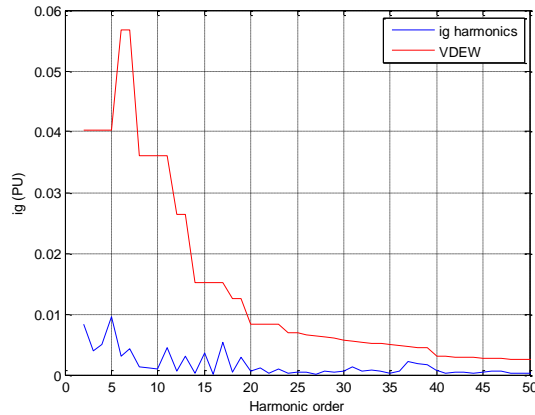


Fig. 15. Grid current harmonics and the VDEW limit for PDPWM modulation.

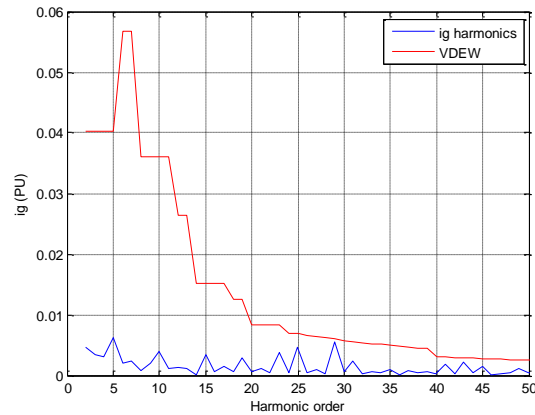


Fig. 16. Grid current harmonics and the VDEW limit for SHEPWM modulation.

Table VII shows the power losses (difference between input power and output power of each stage) measured for different output power operating points (power factor set to 1, only delivering active power) for both modulations with their filters. The losses on the converter and on the filter decrease with SHEPWM modulation.

TABLE VII
LOSSES AND EFFICIENCY MEASURED

Output power (kW)	Power Losses (%)				Grid side efficiency η (%)	
	PDPWM		SHEPWM		PDPWM	SHEPWM
	Grid converter	Grid filter	Grid converter	Grid filter		
320	0.218	0.261	0.118	0.058	91.01	96.68
685	0.268	0.263	0.124	0.062	95.34	98.37
1200	0.324	0.271	0.152	0.069	97.03	98.89
2692	0.518	0.3	0.291	0.103	98.17	99.12
4800	0.789	0.346	0.508	0.159	98.58	99.17
5100	0.832	0.352	0.527	0.167	98.60	99.18

Fig. 17 illustrates the efficiency of the grid side (grid side converter and grid filter). The figure shows that the converter efficiency and the filter efficiency are increased with

SHEPWM modulation, and hence, the overall efficiency.

Fig. 18 shows that the overall efficiency is increased when using SHEPWM modulation especially at low and medium loads where efficiency is a key factor in wind turbine applications. The increase on the efficiency is between 0.6 % and 2 %, for a power range of 1000-5000 kW.

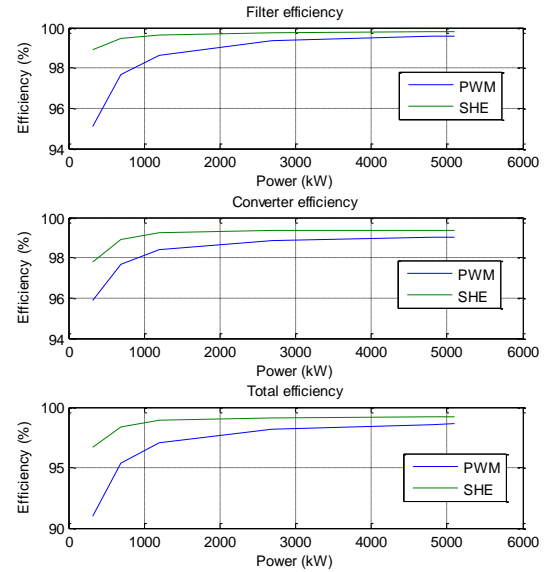


Fig. 17. Grid side efficiency for PDPWM modulation and SHEPWM modulation.

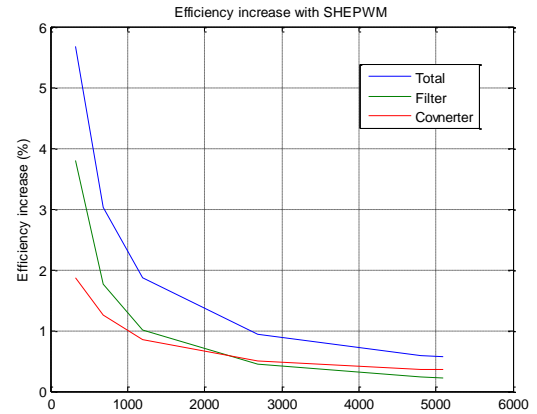


Fig. 18. Grid side efficiency increase.

Last, Table VIII resumes some THD values of the grid current for different output powers (the power factor was 1). The THD remains under the 3% for all the operating points.

TABLE VIII
GRID CURRENT THD

Output power (kW)	THD (%)	
	PDPWM	SHEPWM
1000	2.85	1.98
2000	1.42	1.29
3000	0.82	1.09
4000	1.01	0.65
5000	0.82	0.53

VI. CONCLUSIONS

An efficiency enhancement of 0.6-2 % on a multi-Megawatt medium-voltage NPC for a wind power application has been achieved especially at low and medium loads using SHEPWM modulation.

The low switching frequency of the IGBTs for the medium-voltage applications requires high damping at the resonance frequency of the LCL filter for a PDPWM modulation. This modulation has shown to be suboptimal in terms of efficiency on the filter.

The SHEPWM modulation provides some degrees of freedom and the produced harmonics can be altered. The low order harmonics near the resonance frequency of the LCL filter can be eliminated, reducing the passive damping requirements to meet the grid codes. This leads to a higher damping resistance, and hence, to lower the damping losses.

Comparing the simulation and experimental results of the SHEPWM modulation with the previously used PDPWM modulation, the losses on the damping resistor and the switching losses have been decreased. Additionally, the harmonic emission also fulfills the requirements of the VDEW grid code and the THD remains similar.

REFERENCES

- [1] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter", *IEEE Trans. on Industrial Electronics*, vol. 58, pp. 1205-1217, 2011.
- [2] C. Zhang, T. Dragicevic, J.C. Vasquez, J.M. Guerrero, "Resonance damping techniques for grid-connected voltage source converters with LCL filters — A review", in *Proc. IEEE International Energy Conference (ENERGYCON)*, Dubrovnik, Croatia, 2014, pp. 169 - 176.
- [3] J. San-Sebastian, I. Etxeberria-Otadui, A. Rujas, J.A. Barrena, P. Rodriguez, "Optimized LCL filter design methodology applied to MV grid-connected multimegawatt VSC", in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, USA, 2012, pp. 2506-2512.
- [4] S. V. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines", in *Proc. International Conf. Power Electronics ICPE*, Daegu, South Korea, 2007, pp. 1133-1138.
- [5] T. C. Y. Wang, Z. Ye, G. Sinha, and X. Yuan, "Output filter design for a grid-interconnected three-phase inverter," in *Proc. IEEE Annual Power Electronics Specialist Conf. (PESC)*, Acapulco, Mexico, 2003, pp. 779-784.
- [6] M. Liserre, F. Blaabjerg and S. Hansen "Design and control of an LCL-filter-based three-phase active rectifier", *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp.1281 -1291, 2005.
- [7] W. Wu, Y. He and F. Blaabjerg "A new design method for the passive damped LCL- and LLCL-filter based single-phase grid-tied inverter", *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp.4339 -4350, 2013.
- [8] M. Huang, W. Wu, F. Blaabjerg, Y. Yang, "Step by step design of a high order power filter for three-phase three-wire grid-connected inverter in renewable energy system", in *Proc. IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Rogers, AR, USA, 2013, pp. 1-8.
- [9] R. Pena Alzola, M. Liserre, F. Blaabjerg, R. Sebastian, J. Dannehl, and F. Fuchs, "Analysis of the passive damping losses in LCL-filter-based grid converters", *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2642–2646, Jun. 2013.
- [10] P. Channegowda and V. John "Filter optimization for grid interactive voltage source inverters", *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp.4106 -4114, 2010.
- [11] Z. Shao, X. Zhang, F. Wang, F. Li, and R. Cao, "A novel design method of LCL filter for a grid-interconnected three-level voltage source inverter", in *International Power Electronics and Motion Control Conference (IPEMC)*, Harbin, China, 2012, vol. 4, pp. 2873-2876.
- [12] J. Muehlethaler, M. Schwewizer, R. Blattmann, J.W. Kolar, A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers", *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, Jul. 2006.
- [13] A. Reznik, M.G. Simoes, A. Al-Durra, S.m. Mueyen, "LCL filter design and performance analysis for grid-interconnected systems", *IEEE Trans. Ind. Applications.*, vol. 50, no. 2, pp. 1225–1232, Jul. 2013.
- [14] W. Wu, M. Huang, X. Wang, H. Wang, F. Blaabjerg, M. Liserre and H.S. Chung, "A Robust Passive Damping Method for LLCL-Filter-Based Grid-Tied Inverters to Minimize the Effect of Grid Harmonic Voltages", *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3279–3289, Jul. 2014.
- [15] J. Muehlethaler, M. Schweier, R. Blattmann, J.W. Kolar and A. Ecklebe, "A Robust Passive Damping Method for LLCL-Filter-Based Grid-Tied Inverters to Minimize the Effect of Grid Harmonic Voltages", *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3279–3289, Jul. 2014.
- [16] B.P. McGrath, D.G. Holmes, T. Lipo, "Optimized space vector switching sequences for multilevel inverters", *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.
- [17] B.P. McGrath, D.G. Holmes, T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range", *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 941–948, Jul. 2006.
- [18] H.S. Patel, R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: part I - harmonic elimination", *IEEE Trans. Ind. Applications.*, vol. IA-9, no. 3, May/Jun. 1973.
- [19] . Fei, X. Ruan and B. Wu, "A Generalized Formulation of Quarter Wave Symmetry SHE-PWM Problems for Multilevel Inverters", *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1758–1766, Jul. 2009.
- [20] M.S.A. Dahidah, G. Konstantinou and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications", *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1, 2014.
- [21] K. Yang, Z. Yuan, R. Yuan, W. Yu, J. Yuan and J. Wang, "A Groebner Bases Theory Based Method for Selective Harmonic Elimination", *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1, 2015.
- [22] BDEW "Technische Richtlinie Erzeugungsanlagen am Mittelspannungsnetz", Berlin, Germany, Jun. 2008.
- [23] J. Xu, T. Tang, S. Xie, "Research on low-order current harmonics rejections for grid-connected LCL-filtered inverters", *International Conference on Power Electronics, IET*, Manchester, United Kingdom, 2014, vol. 7, no. 5, pp. 1227-1234.
- [24] Ingeteam Power Technology (2015), Available: <http://www.ingeteam.com>