MODULATION AND CONTROL STRATEGIES FOR MULTILEVEL FIVE-PHASE OPEN-END WINDING DRIVES

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ABSTRACT

Industrial and automotive trends clearly demonstrate an increased interest in medium- and high-power variable speed drives. Despite constant progress in the technology, the semiconductor characteristics are still the bottleneck in drive designs, due to their limitations to block high voltage (several kilovolts) and conduct high current (several hundreds of amperes per-phase). For this reason and numerous other advantages, solutions based on multilevel inverters and multiphase machines are considered in recent years.

The open-end winding drives are an alternative approach for drives construction. This thesis investigates carrier based pulse width modulation schemes for five-phase open-end winding drives. Two drive topologies, with isolated dc-links of two inverters, are considered. The first one consists of two two-level inverters and a five-phase machine. The second topology utilises one three- and one two-level five-phase inverter. It is shown that the same drive structure can produce a different number of phase voltage levels, when different dc-link voltages of two inverters are in use. Hence, dc-link voltage ratio is considered as an additional degree of freedom. An open-end winding structure that comprises of two two-level inverters offers harmonic performance equivalent to three- and four-level single-sided supply. The second drive structure under analysis is able to produce four, five and six voltage levels, depending on utilised dc-link voltage ratio.

Modulation schemes are classified in two categories. So-called coupled modulation schemes are developed under the assumption that open-end winding drives are equivalent to certain single-sided multilevel solutions. This enables the application of slightly modified modulation methods for multilevel inverters, to the open-end winding configurations. As a consequence, number of utilised voltage levels can be higher than the sum of two inverters' number of levels. However, this boost in number of levels relies on simultaneous switching in two inverters' legs connected to the same drive phase, which causes so-called dead-time spikes. The second group, referred to in this thesis as decoupled modulation schemes, rely on the separate modulation of two inverters, using voltage references obtained by splitting the overall phase voltage reference, proportionally to inverters' dc-link voltages. Hence, this kind of modulation offers somewhat worse harmonic performance, when compared to coupled modulation schemes.

Special attention is paid to the stability of dc-link voltage levels, which is one of the most important figures of merits of quality for multilevel drives. Using a novel analysis approach, it is demonstrated that utilisation of optimal harmonic performance offered by coupled modulation methods leads to unstable dc-link voltages, but only in the cases where dc-link voltage ratio is used for increment of available number of voltage levels. Decoupled modulation methods offer stable dc-link voltages, regardless of drive configuration.

One of the drawbacks of the analysed open-end winding drives is the need for two isolated dc sources, which form dc-link voltages of two inverters. For that reason, a possibility to use only one dc-source in open-end winding drives with isolated inverters is considered. Analysis shows that both drive topologies can be operated using so-called bulk and conditioning inverter control, where bulk inverter is supplied from an active dc source, but operates in staircase mode, while conditioning inverter performs high-frequency pulse width modulation, in order to suppress low-order harmonic content. This kind of operation is investigated in details for two specific configurations in which two inverters never operate at the same time in PWM mode, when coupled modulation methods are used. Comparison of the results shows that topology which comprises from one three- and one two-level inverter is more suitable for this kind of control. Together with previously analysed configurations and modulation strategies, dynamic performance of this novel drive is tested under the closed-loop speed control. Experimental results show that open-end winding drives are suitable for a wide range of applications.

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Firstly, my deepest gratitude goes to my supervisors Dr. Martin Jones (director of studies) and Prof. Dr. Emil Levi, who gave the chance to work in this, for me the most interesting research field, and who were actively mentoring my work and progress in last three and a half years. Their patience, support and advice were essential during my PhD studies.

Probably the biggest influence on my research comes from two of my colleagues, Dr. Nandor Bodo and Dr. Obrad Djordjević, who were always available for a discussion. Since my research is in a way continuation of their work, support that they provided during my first research steps in the field of multiphase open-end winding drives was crucial for further progress. I leaned from them many practical things related to the multiphase drives and rapid prototyping systems that were used for experimental verification. I would also like to thank to the former and current members of LJMU EMD group, particularly to Dr. Ivan Subotić, Dr. Hang Seng Che, Dr. Chee Shen Lim and Ivan Zorić for their support and valuable advice. Discussions with them broadened my knowledge in various fields related to my PhD studies. The most beautiful memories I have from last three years are related to our friendship and frequent gatherings. It was a privilege to spend this time with all of you!

I wish also to express my special gratitude to Prof. Dr. Predrag Pejović, for very interesting lectures about power electronics, which undoubtedly awaked my interest in this field. Prior to my PhD studies, I had a chance to work more closely with him, on research projects related to the current injection principle applied to three-phase diode rectifiers. He introduced me to the specific research approach and application of mathematical models in power electronics, skills I often relied on during my PhD studies. Another professor from the University of Belgrade, Dr. Slobodan Vukosavić has broadened my interest in electrical machines and drives, thanks to his very practical approach to the topic.

My personality and research skills are highly influenced by the people in Petnica Research Centre, Serbia. During my last two years of high school I was a participant, and during my studies, a research assistant in astronomy section, which provided me a chance to work with probably the most talented and perspective people from my country, that share the same passion for science and research. There I learned the difference between learning and research, and realised that true scientific engagement relies on questioning everything, from scientific “facts”, to the authorities and established opinions how things work and how research should be performed. Although only a few aspects of practical knowledge I gained in Petnica Science Centre are relevant to my field of interest, that experience helped me develop probably the most important skills for any research – to constantly ask questions and doubt everything, including my work, research methods and findings. This unique experience also helped me understand that curiosity and open-mindless are more important for science, then starting knowledge or talents.

The biggest influence on my development, as a researcher, and more importantly, as a person, definitely comes from my girlfriend Marija Janković. This thesis is dedicated to Marija. I would like to thank her for constant and wholehearted support. More than four years ago, we decided together to go abroad and look for a chance to do the research in our common field of interest, power electronics. Being a PhD student in the same area of research, Marija was able to provide a different view on certain topics and actively support my efforts thought long discussions and analysis. Work with her in the last six years had a strong and very positive influence on my research skills.

At the end, I would like to thank my mother Ljiljana Jeneckov, for her love and care. Without her constant support and encouragement this thesis wouldn’t have been completed.

CONTENTS

LIST OF USED ABBREVIATIONS

ac	Alternating current.
APOD PWM	Alternate phase opposite disposition carrier based pulse width modulation.
ANPC	Active neutral point clamped inverter.
B&C	Bulk and conditioning (control).
CB PWM	Carrier based pulse width modulation.
CMV	Common mode voltage.
CHB	Cascaded H-bridge inverter.
dc	Direct current.
div	Division unit for oscilloscope screenshots.
DSP	Digital signal processor.
DTC	Direct torque control.
EMD	Electric machines and drives (research group at LJMU).
emf	Electro motive force.
ERS	Equal reference sharing.
FFT	Fast Fourier transformation.
FC	Flying capacitor inverter.
FOC	Field oriented control.
GaN	Gallium nitride (semiconductor compound/technology).
GTO	Gate turn-off thyristors.
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated gate bipolar transistor.
IGBT+D	Power module that contains one IGBT and its antiparallel diode.
IGCT	Integrated gate commutated thyristor.
LJMU	Liverpool John Moores University.
LS PWM	Level shifted pulse width modulation.
MMF	Magneto-motive force.
MOSFET	Metal oxide semiconductor field effect transistor.
MMC	Modular multilevel converter.
NPC	Neutral point clamped inverter.
NPN	N-type bipolar junction transistor.
NPP	Neutral point piloted inverter.
OeW	Open-end winding.
PEBB	Power electronics building block.
PD PWM	Phase disposition carrier based pulse width modulation.
PI	Controller with proportional and integral gain.
POD PWM	Phase opposition disposition pulse width modulation.
PRS	Proportional reference sharing.
PS PWM	Phase shifted pulse width modulation.
PWM	Pulse width modulation.
p.u.	Per unit.
rms	Root mean square value.
SAR	Switching action reduction (part of PWM scheme).
SAT	Saturation block of PI controller.
SiC	Silicon carbide (semiconductor compound/technology).
SV PWM	Space vector pulse width modulation.
SRA	Spike removal algorithm (dead-time spike elimination method).
THD	Total harmonic distortion.
URS PWM	Unequal reference sharing PWM scheme.
URS1 PWM	URS PWM with carriers in phase disposition.
URS2 PWM	URS PWM with carriers in alternate phase disposition.
VSD	Vector space decomposition.
VSI	Voltage source inverter.

LIST OF PRINCIPAL SYMBOLS

a	Superscript label for the first complementary IGBT+D pair in three-level NPC inverter.
A_{ki}	Logical variables, used in algorithm for PWM gating signal generation.
b	Superscript label for second complementary IGBT+D pair in three-level NPC inverter.
C_i	The i^{th} carrier signal.
CH1..4	Oscilloscope channel (1, 2, 3 or 4).
C_{dc1}, C_{dc2}	Capacitor in dc-link of two-level inverter VSI_1 and VSI_2, respectively.
C_{dc11}, C_{dc12}	Capacitors in dc-link of three-level inverter.
dx/dt	The first derivative of signal x over time.
D^x_{upjk}, D^x_{dnjk}	Antiparallel diode in j^{th} VSI and k^{th} drive phase, x stands for switching pair a or b in the case of NPC converter.
d^x_{jk}	Duty ratio that corresponds to complementary IGBT+D pair labelled with x (if any), in j^{th} VSI and k^{th} leg.
e	Error signal in closed-loop control (input of PI control).
f_q	Grid voltage fundamental frequency.
f_n	Rated frequency.
f_S	PWM switching frequency.
g^x_{upjk}, g^x_{dnjk}	Gating signal for the switch in the pair x (if any) in j^{th} VSI and k^{th} leg (dn – down, up - upper).
$i_{dclink1k}$, $i_{dclink2k}$	The k^{th} drive phase contribution to dc-link current of VSI_1 and VSI_2, respectively.
$i_{dclink1}$, $i_{dclink2}$	VSI_1 and VSI_2 dc-link currents, respectively.
i_d, i_q	Phase current components in the first (d-q) plane.
i^*_d	Reference for i_d current component.
i_k	The k^{th} phase stator current.
I_m	Phase current amplitude.
i^*_q	Reference for i_q current component.
i_x, i_y	Phase current components in the second (x-y) plane.
i_{x3}, i_{y3}	Phase current 3^{rd} harmonic x and y components, respectively.
i_{x7} i_{y7}	Phase current 7^{th} harmonic x and y components, respectively.
J	Rotor inertia.
K_{aw}	PI controller anti-windup constant.
K_P	PI controller proportional gain.
K_I	PI controller integral gain.
L_m	Magnetising inductance.
l_k	The k^{th} normalised voltage level.
$L_{\gamma r}$	Rotor leakage inductance.
$L_{\gamma s}$	Stator leakage inductance.
M_b	Modulation index (border) value that corresponds to the dc-link current mean value sign change.
M_{max}	Maximal value of modulation index considered in this research.
M_{min}	Minimal value of modulation index considered in this research.
N	Switching state number in equivalent models analysis.
M_{start}	Modulation index value for which dc-link capacitor voltage balancing algorithm starts to work.
p	Number of machine pole pairs.
r	The dc-link voltage ratio, i.e. V_{dc1}/V_{dc2}.
r_{max}	Maximal value of dc-link voltage ratio considered in simulations.
r_{min}	Minimal value of dc-link voltage ratio considered in simulations.
R_r	Rotor resistance.
R_s	Stator resistance.
R_{offset}	Phase voltage reference offset.
s	Laplace operator.
S_{jk}	The j^{th} VSI and i^{th} leg state, logical representation of leg voltage (1 or 0).
S^x_{upjk}, S^x_{dnjk}	Upper switch state in the j^{th} VSI and k^{th} leg.
T	Fundamental period.
TD_k	The k^{th} normalised time delay signal.
$t_{d\text{-}t}$	Dead-time interval.
TL	Machine load.
T_S	Switching period.
T_{stop}	Simulation end time.
T_r	Rotor time constant.
t_{rr}	Reverse recovery time
v_{ac1k}	The k^{th} ac voltage source of three-phase supply system that is isolated from the mains.

v_{ac2k}	The k^{th} ac voltage source of three-phase supply system that is isolated from the mains and v_{ac1k} sources.
v_{cdc2}	Voltage across capacitor C_{dc2}.
V^{*}_{cdc2}	Reference for closed-loop control of C_{dc2} voltage.
v_{cdc21}	Voltage across capacitor C_{dc21}.
V_{dc}	The overall dc-link voltage of open-end drive. Normalisation factor in equivalent models.
V_{dc1}, V_{dc2}	The dc-link voltage, of VSI_1 and VSI_2, respectively.
v_{inj}	Min-max injection term, used in phase voltage reference expression.
v_{jk}	The j^{th} VSI leg voltage in k^{th} phase.
v^{*}_{jk}	Voltage reference for j^{th} VSI k^{th} phase in the case of URS PWM.
v_k	The k^{th} phase voltage.
v^{*}_k	The k^{th} phase voltage reference.
v_{mp}	Mid-point voltage of NPC converter.
$v_{n1,}$ v_{n2}	Potential of the lower dc-link rails of VSI_1 and VSI_2, respectively.
v_{n2n1}	Common mode voltage.
V_{n2n1}	Common mode voltage dc component.
v_n	Rated phase voltage peak value.
$v_{out\text{-}rect\text{-}j}$	Output voltage of three-phase diode rectifier, used for dc-link voltage formation for j^{th} VSI.
v_{p1}, v_{p2}	Voltage potentials of the upper dc-link voltage rails of VSI_1 and VSI_2, respectively.
VSI_1, VSI_2	VSIs in OeW drive topology, supplied from V_{dc1} and V_{dc2}, respectively.
$v_{x\text{-}y}$	Voltage space vector in the second plane (one with non-torque-producing quantities).
$v_{\alpha\text{-}\beta}$	Voltage space vector in the first plane (one with torque-producing quantities).
X	Don't care state in truth tables.
X_i	The rms value of a harmonic.
$\underline{X}_n$,	Phase voltage n^{th} harmonic component.
$\underline{X}_{nj}$	The j^{th} VSI contribution to the phase voltage n^{th} harmonic component.
x-y	2D plane with non-torque-producing quantities.
Z	High impedance state of VSI leg output.
α	Conduction angle for staircase operation in the case of B&C control.
α-β	2D plane with torque-producing quantities.
γ	Phase angle between stator windings ($2\cdot\pi/5$ in the five-phase case).
ΔM	Modulation index step increment in simulations and experiments.
Δr	The dc-link voltage ratio step increment in simulations.
Δt	Simulation time step.
Δv, Δv', Δv"	Reference offsets, used for dead-time spike elimination, SRA outputs.
Δv_{1k}, Δv_{2k}	The final Δv value that is applied to VSI_1 and VSI_2, respectively, in k^{th} drive phase.
θ_e	Estimated rotor position.
θ	Measured rotor position.
θ_{slip}	Slip estimation.
σ	Output of PI controller in dc-link voltage stability closed-loop control (within B&C control scheme).
τ_{jk}	Time instants that correspond to the k^{th} phase voltage reference j^{th} crossing with equivalent voltage levels.
ϕ	Phase angle between stator phase voltage and stator phase current.
ω	Measured rotor speed.
ω^{*}	Rotor speed reference.

Chapter 1

INTRODUCTION

1.1. PRELIMINARY REMARKS

At the beginning of the electrical ac machines era, the number of machine phases was chosen to match with the three-phase grid, since induction machines were directly supplied from the mains. Later on, power electronic converters were introduced in order to allow easier speed and position control in industrial applications. In essence, the power electronic converter can be viewed as an interface that decouples the three-phase mains from the machine. Nowadays, there are many different types of power electronic converters, which can serve this purpose. A simplified diagram classifying the different types is shown in Fig. 1.1. The great variety of solutions visible in Fig. 1.1 underlines the importance of this research field for industrial applications, but also suggests that there is no universal solution that can meet the demands of a wider range of applications. More details about various drive structures and comparison of their performance and application areas can be found in [Rodriguez et al. (2009), Wilamowski and Irwin (2011), Kouro et al. (2012)]. One of the common benefits of all converter structures shown in Fig. 1.1 is that the number of machine's phases is not limited to three. However, three-phase machines are still customarily adopted for variable speed drives.

In low- and medium-voltage (below 10 kV) high-power drives, the most frequently used concept is based on voltage source inverters (VSI). Here, drives with the overall power consumption higher than 100 kW are considered as high-power applications. The general structure of a modern variable-speed electric drive is depicted in Fig. 1.2, referred to in this thesis as single-sided machine supply.

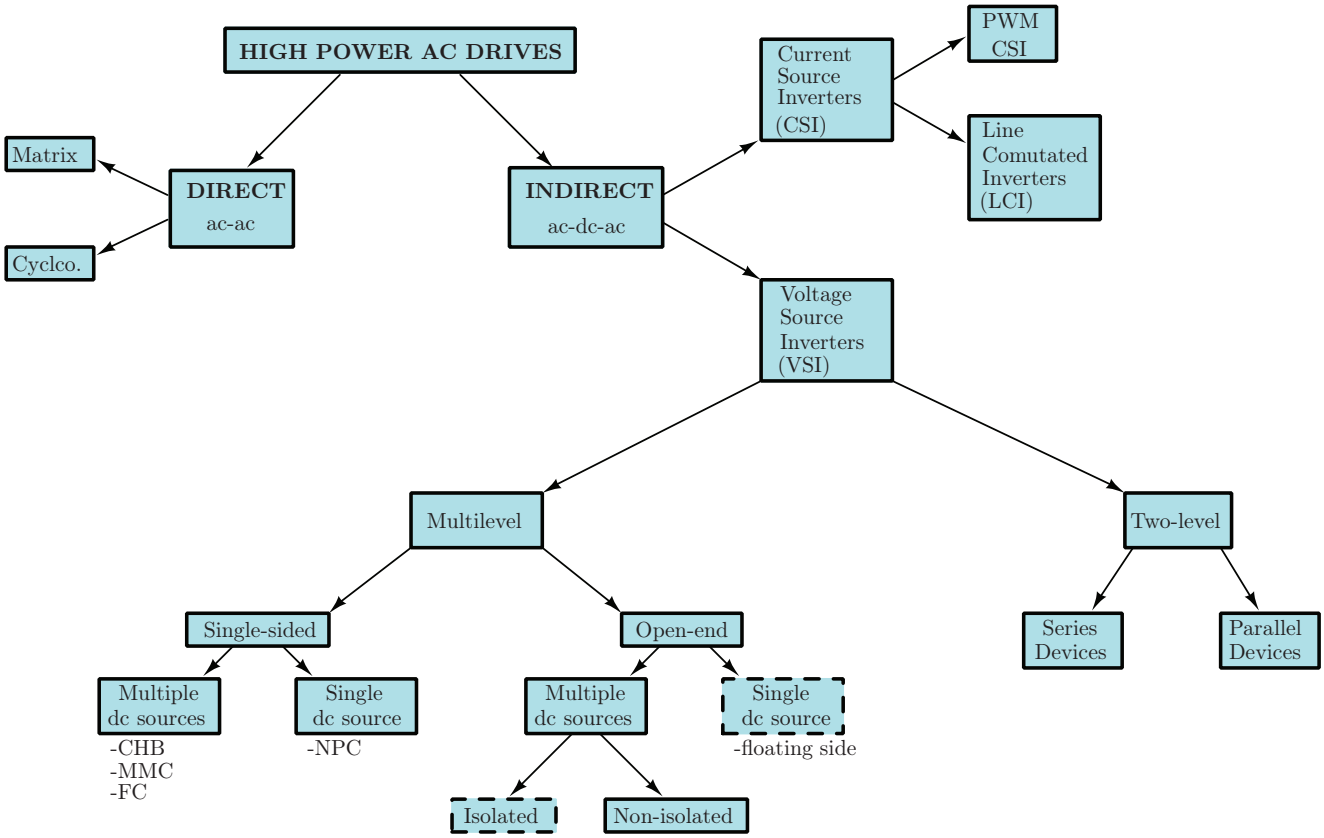


Fig. 1.1. High-power ac drives classification, in terms of power electronics converter structure.

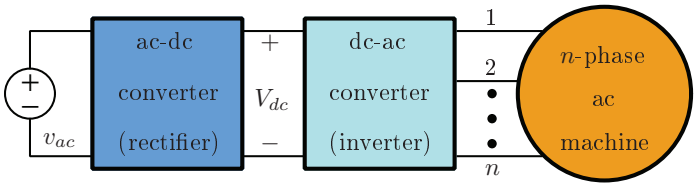


Fig. 1.2. Multiphase multilevel drive, with neutral point connected windings (single-sided supply).

The first stage of the drive is an ac-dc converter that rectifies the ac voltages from the mains to form a dc-link voltage V_{dc}. Alternatively, this stage can be replaced with a battery pack, which is of interest for automotive applications. In industrial drives, this stage usually employs a three-phase diode rectifier, which has a capacitor bank at its output. The second stage, dc-ac converter, performs the inverse process, i.e. formation of ac phase voltages from dc-link voltage. Hence, the power electronics converter connected to the machine is known as an inverter, and its main purpose is to produce a fully controllable (amplitude, phase shift and frequency) set of voltages.

Clearly, this approach opens the possibility of using the number of machine phases as a design parameter. So-called multiphase machines have been reported to offer numerous advantages over the three-phase counterparts [Levi et al. (2007)]. These advantages are especially important for high-power drives. The most important benefits of multiphase machines are:

- Possibility of splitting the required overall power across more than three phases. In the case of high-power applications, reducing the current rating of the semiconductor components is of exceptional importance, and therefore multiphase drives are increasingly used.
- A significant improvement in fault tolerance of the drive. Namely, any ac machine, regardless of the number of phases, requires only two independent stator currents for independent flux and torque control. In a three-phase single-sided machine supply, a fault in one phase means that there are no longer two independent currents. However, a multiphase machine can continue to operate with a rotating field in post-fault operation as long as at least three phases are healthy.
- A potentially better efficiency due to reduced space harmonic content of the magneto-motive force [Levi et al. (2007)].
- Possible exploitation of different stator windings interconnections, which affect the speed-torque drive characteristics. By using small amount of additional hardware, those can be combined during drive operation, in order to meet application requirements in various operating conditions [Sadeghi et al. (2012), Nguyen et al. (2013)].

Although multiphase variable-speed drive systems have been a subject of research for the last 50 years, it is the last fifteen years that have seen an enormous growth of the quantum of knowledge in the area. This has been motivated by numerous specific application areas, such as electric ship propulsion, locomotive traction, electric and hybrid electric vehicles [Levi et al. (2007), Levi (2008)], where the advantages of multiphase systems outweigh the initial higher cost of the development. Various pulse width modulation (PWM) techniques have been developed for various phase numbers (including both odd and even numbers), which take into account the nature of the multiphase system and enable realisation of desired reference voltage on average in a switching period. The most relevant past research efforts are addressed in the literature review, provided in Chapter 2.

Voltage source inverters are nowadays the most common solution for variable speed drives. Among them, the most frequently used are two-level inverters. Despite the most recent progress in semiconductor industry, limited ability of semiconductor devices to block high-voltages makes two-level inverters less suitable for high-power industrial

applications where high-voltage drives are required. This problem can be overcome with so-called multilevel inverters. They are made as a series connection of semiconductor switches, therefore circumventing some of the limitations set by semiconductor technology. Contrary to the solutions based on parallel and series connected semiconductor devices (Fig. 1.1) multilevel inverters do not require simultaneous switching, thanks to their specific structures. This eliminates the issues related to current and voltage sharing, which still limits the usage of two-level inverters based on parallel and series semiconductor connections, for high-power applications, with regard to current semiconductor technology.

Three-phase multilevel topologies have been drawing an increased attention in the last two decades. The numerous advantages of multilevel supply include: good power quality (lower voltage distortion and dv/dt in comparison with two-level inverters), improved electromagnetic compatibility, operation with a lower switching frequency (lower switching losses), capability to utilise high dc-link voltage, smaller common mode voltage (CMV) which leads to reduction of the stress in the machine bearings, and the possibility for fault tolerant operation in some, modular configurations. There are various topologies of multilevel converters. The main ones are the neutral point clamped (NPC), the flying capacitor (FC) and cascaded converters. More details can be found in Chapter 2, where a literature survey of multilevel topologies and their application to the three-phase (Section 2.2) and multiphase drives (Section 2.4) is given. Surprisingly, it can be concluded that the multilevel inverter supply is well-established for three-phase drives, while that does not apply to multiphase drive systems. The most of the initial attempts, surveyed in [Levi et al. (2007), Levi et al. (2008)], are characterized with inappropriately defined requirements in the development of the PWM algorithms and are therefore ill-suited for industrial applications.

From the previous research results, it is obvious that inverters with greater number of voltage levels are able to produce finer, more sinusoidal ac voltages, while higher dc-link voltage can be utilised. This leads to better performance and increased application power rating, with the same semiconductor technology. However, increased number of voltage levels leads to more complex control (regarding both software and hardware). Furthermore, the overall number of components rapidly increases with the increment of number of voltage levels, including not only power switches (IGBTs, or power MOSFETs) but also additional diodes and/or capacitors [Kouro et al. (2012)].

Another way to construct a multilevel drive is to use an open-end winding (OeW) machine. Instead of forming an isolated neutral point or using any other configuration that is based on stator windings interconnections, in the case of OeW machine all stator phase windings are left open on both ends. Therefore, this type of machine is supplied from two inverters as shown in Fig. 1.3. Clearly, stator phase voltage is in this case formed as a combination of two inverters' leg voltages. Earlier research efforts related to OeW drives showed that multilevel performance could be achieved with two two-level inverters [Lega (2007), Satiawan (2012)]. Also, OeW drives offer some further advantages which are discussed later in the thesis. So far, relatively few research efforts have been directed towards the multiphase open-end winding multilevel topology, as shown in Section 2.5. The majority of this work is undertaken at Liverpool John Moore's University (LJMU) in Electric Machines and Drives (EMD) group.

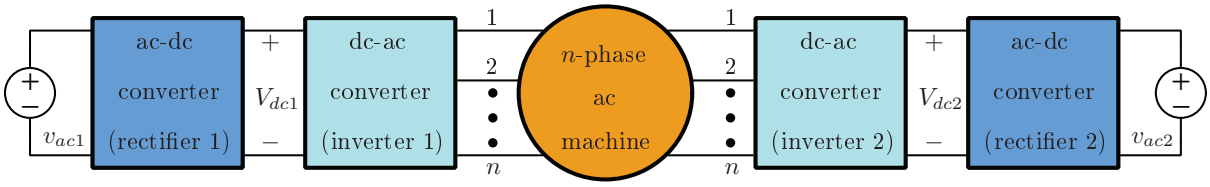


Fig. 1.3. Principal scheme of multilevel multiphase open-end drive structure.

This thesis represents an attempt to extend the previous work in this research area, with the emphasis on developing suitable control algorithms for five-phase open-end winding drives. Drive groups under analysis are boxed in Fig. 1.1 with dashed lines. In particular, two different drive structures are analysed. The first one utilises two two-level inverters that are supplied with different dc-link voltage levels. The second topology utilises one three- and one two-level inverter to supply a five-phase OeW machine. This structure is analysed for several different cases as well, with regard to utilised dc-link voltage levels of two inverters. Combination of different dc-link voltage levels of two inverters in both topologies leads to utilisation of different number of voltage levels in the phase voltage.

In particular, topology with two two-level inverters can be controlled in such a way that the final phase voltage waveform is equivalent to those produced by three- and four-level single-sided multilevel drives. The topology that utilises three- and two-level inverters in OeW structure is able to produce phase voltage waveforms equivalent to those obtained with four-, five- and six-level single-sided machine supplies. This clearly shows that the ratio between dc-link voltages of two inverters can be used as an additional degree of freedom in drive design, offered by open-end winding drive concept. A special type of OeW drive, which employs two isolated inverters but only one dc voltage source, is analysed. All mentioned OeW configurations are firstly analysed in terms of drive harmonic performance and other important figures of merit related to multilevel drives. Finally, selected topologies and developed modulation strategies are tested within closed-loop field oriented control.

This thesis is written with the aim to provide sufficient material for future research efforts related not only to modulation strategies for multilevel multiphase open-end winding drives, but for modulation strategies for drive applications in general. Although probably the most apparent and obvious contribution of this thesis is in the developed modulation strategies, the author would like to emphasise that some important contributions might be in the developed analysis methods, which can be applied in many other cases, i.e. for different drive configurations.

1.2. RESEARCH AIM, OBJECTIVES AND NOVELTY

The mentioned topologies offer more degrees of freedom for development of modulation strategies, higher reliability, possibilities for development of post-fault modulation schemes, and other advantages, but they have not been considered before as a viable solution for industrial high-power applications. The literature survey provided in Chapter 2, shows that this research is novel, since no similar research has been conducted so far. Hence, it seems reasonable to believe that the results presented in this thesis can lead to further progress in the development of these drive types.

Analysis of drives structures and development of modulation strategies in this thesis, together with simulation and experimental verification, enable easier drive topology selection for future applications, with specific requirements. Possible disadvantages of the drives (usually specific for each of the topologies) are analysed as well, in order to provide a clear picture about the validity of the proposed solutions and to make a useful contribution to the engineering and scientific communities in general.

Results from [Satiawan (2012), Bodo (2013)] where multiphase OeW topology with two two-level inverters (2L-OeW-2L) is analysed are taken as a starting point for this research. Extension of that work for the unequal dc-link voltage case is presented in Chapter 3, where a novel analysis method for OeW drives is proposed, based on equivalent drive model. This approach unifies the analysis of the proposed drive for an arbitrary dc-link voltage ratio. The first results of this work are presented in three conference papers [Darijevic et al. (2013a), Darijevic et al. (2013b), Jones et al. (2014)]

and later used for comparison with other drive structures in other conference papers [Darijevic et al. (2015a), Darijevic et al. (2015c)], as well as in an IEEE journal publication [Darijevic et al. (2016)].

Open-end drives, supplied with one three-level and one two-level inverter (3L-OeW-2L), used to supply a five-phase machine are considered as the second research topic. In Chapter 4, modulation strategies for this topology are derived, using the same equivalent model approach. Preliminary results for this topology are presented in [Darijevic et al. (2015a), Darijevic et al. (2015b), Darijevic et al. (2015c)].

The third research theme is related to the control of the two inverters in bulk and conditioning mode [Corzine et al. (2004), Corzine et al. (2006)]. This is analysed for topologies with one or two dc sources. This approach has never been analysed for multiphase open-end drive supplied from three-level inverters, or with two inverters with different number of voltage levels. Initial analysis in Chapter 6 shows that only two specific cases of all those analysed in Chapters 3 and 4 are suitable for operation with one active dc source. Detailed examination of their performance with regard to drive load and harmonic performance showed that the 3L-OeW-2L drive with dc-link voltage ratio 2:1 is better suited for this kind of operation. The importance of this topic is related to the need for isolation between the two dc-link voltage sources, as well as the overall cost of any additional cables that are required in OeW drives (Fig. 1.3), when compared to single-sided solutions (Fig. 1.2). From that point of view, elimination of one voltage source in Fig. 1.3 makes the application area of OeW drive wider. Preliminary results of this analysis are published in [Darijevic et al. (2015d)].

1.3. ORGANISATION OF THE THESIS

This thesis consists of nine chapters. Chapter 1 is a general introduction to the topic of this research. It discusses the motivation for the research, novelty and explains what the main contributions are.

A literature survey of relevant scientific papers, books and patents is provided in Chapter 2. The aim of that chapter is to provide a clear picture about the current state-of-the-art in the research areas related to high-power drives. Through discussion of these past results, an attempt is made to show what kind of improvements in drive performance can be expected from the topologies that are under investigation in this research.

Five-phase 2L-OeW-2L drives, with equal dc-link voltages, are briefly analysed in Chapter 3. Initial analysis, based on the equivalent drive model, shows that this topology is able to produce three voltage levels if the dc-link voltages of the two inverters are equal and four voltage levels if they are in any other ratio different from 1:1. Two different types of carrier based modulation strategies are introduced in that chapter. The first, so-called coupled modulation schemes, consider the two inverters as a single, coupled entity, which leads to an optimal harmonic performance. Unfortunately, this type of modulation scheme in some cases leads to simultaneous switching of the two inverters which means that dead-time intervals will appear simultaneously in the legs of the two inverters connected to the same drive phase. As a consequence, so-called dead-time spikes occur, which leads to increased low-order phase current harmonics, as well as acoustic noise and electromagnetic interference (EMI). It is shown how this problem can be mitigated by employing a so-called spike removal algorithm. The second kind of modulation, referred to as decoupled modulation scheme, is based on the separate modulation of two inverters. This leads to somewhat worse harmonic performance, since some of the voltage levels in the case of unequal dc-links can be formed only by simultaneous switching of the two inverters, i.e. simultaneous transitions in their leg voltage outputs connected to the same drive phase. Presented modulation strategies, as well as the proposed solution for dead-time spikes, are experimentally verified and their harmonic performance is discussed in summary of Chapter 3.

Five-phase 3L-OeW-2L drive is presented in Chapter 4. The topology comprises of one three-level, neutral point clamped inverter, and one conventional two-level VSI. Using the analysis methods developed in Chapter 3, it is shown that this drive can be configured to operate equivalently to four-, five- and six-level single-sided inverters. Again, the possibility to modulate two inverters using coupled and decoupled control methods are investigated. Obtained results for the coupled modulation methods lead to a general conclusion that dead-time spikes are present in the phase voltage waveforms when the dc-link voltage ratio is used in order to increase the overall number of voltage levels. This conclusion is in agreement with findings in Chapter 3. However, due to higher number of phase voltage levels, harmonic performance of the topology presented in Chapter 4 is less sensitive to dead-time spikes, due to their lower amplitude and less often occurrences during one fundamental period. The decoupled modulation methods offer similar performance to those in Chapter 3, with respect to the coupled methods for the same drive configuration.

Chapter 5 is dedicated to the analysis of dc-link voltage stability in open-end winding drives. A novel approach, which relies on linearized drive models and sinusoidal approximation of the phase currents, is developed in order to explain the influence of modulation strategies on dc-link voltage stability. It is shown that dc-link voltage ratios which lead to the optimal harmonic performance require hardware solutions for dc-link voltage balancing. In some cases, this leads not only to additional hardware cost and complexity, but also to additional losses. This makes certain drive configurations less suitable for variable speed drives. On the other hand, due to superior harmonic performance, these configurations seem to be optimal solutions for applications in which desired machine speed is constant, since lower harmonic pollution of the phase currents leads to lower torque ripple and lower losses. In general, the analysis in Chapter 5 shows that the drive harmonic performance cannot be taken as the most important figure of merit, which is often the case when new topologies are proposed in the literature.

Open-end winding topologies which are aimed to operate in so-called bulk and conditioning mode are analysed in Chapter 6. The first important conclusion from that chapter is that only drive configurations which do not result in simultaneous PWM operation of the two inverters are suitable for bulk and conditioning control. In this case, coupled modulation can be altered in such a way that one inverter operates in staircase mode, while the second one operates in PWM mode throughout the fundamental period. Analysis of previous research efforts in this field shows that the low-frequency switching (bulk) inverter is usually used to deliver the complete phase voltage fundamental, while the (conditioning) inverter in PWM mode is used to mitigate unwanted low-order harmonics, introduced by staircase modulation. In this case, the active dc source of the inverter in PWM mode side can be omitted, since that inverter does not supply any active power to the drive. Naturally, this requires higher dc-link voltage for the low-frequency inverter, in order to produce the phase voltage fundamental of the same amplitude as in the case when two dc sources are used as in Fig. 1.3. However, the proposed control of the two drive configurations in Chapter 6 effectively boost the dc-link voltage utilisation, which means that the same dc-link voltage levels of both inverters can be kept, while the obtainable phase voltage fundamental is the same as in the case of regular OeW configuration with two isolated dc sources. The only limitation of the proposed concept is related to the harmonic performance, which has to be traded for the conditioning inverter side dc-link capacitor voltage balancing and/or the overall dc-link utilisation. Based on simulation results, it is concluded that the 3L-OeW-2L topology with dc-link voltage ratio 2:1 is more suitable for bulk and conditioning operation, when compared to the 2L-OeW-2L drive with dc-link voltage ratio 1:1.

Based on the analysis in Chapters 3-6, several drive configurations are selected to be tested under closed-loop field-oriented control. Experimental results are summarised in Chapter 7. The main motivation for this kind of test comes from modern variable speed drive applications, such as electric vehicles and other propulsion systems, where closed-loop

control is necessary. Performed tests show that the outer speed control loop does not have any effects on modulation strategy performance, while introducing closed-loop current controllers mitigates dead-time effects on phase current low-order harmonics. Produced phase voltage and current waveforms are in agreement with expectations based on the analysis in Chapter 3, 4 and 6, while high-quality speed control dynamic performance is observed.

A summary of the presented results in this thesis is provided in Chapter 8, together with the discussion of topics for future work. It is proposed that developed OeW topologies and modulation strategies can be used as a starting point for future research, which should have in focus modulation strategies for post-fault operation. At the same time, topics related to different hardware organisation and open-end winding drive topologies that employ inverters with higher number of levels are briefly analysed. Possible benefits and drawbacks of such configurations are stated, based on the gained experience during the herein presented research.

Chapter 9 provides the complete list of references used in this thesis. This is followed with three appendices, related to technical descriptions of numerical simulation procedure and the experimental rig used in this thesis, as well as some additional calculations related to expressions used in Chapter 5. Published conference and journal papers that resulted from the research presented in this thesis are appended at the end of the thesis.

Chapter 2

LITERATURE REVIEW

2.1. INTRODUCTION

The aim of this chapter is to provide a survey of the literature relevant to this research. A very good overview of the high-power adjustable speed drive area is given in [Kouro et al. (2012)]. Drives are clearly classified, according to their topologies, choice of semiconductors, application area, machine types and inverter structure. Consequently, it is clear that the topologies mentioned in Chapter 1 are just a few of the many possible solutions for high-power applications. The exact choice of the topologies that are used in this research is driven by hardware complexity, total cost and maturity of the required semiconductor technology. Some of these three important factors will be addressed later in this chapter, where specific solutions are analysed.

This literature review begins with multilevel three-phase drives (Section 2.2), as a starting point for development of multilevel multiphase drives. Research efforts related to three-phase open-end drives are reviewed in Section 2.3. This enables the identification of suitable control methods, which can be applied to multiphase systems after certain modifications. The most relevant work about multilevel multiphase single-sided drives is presented in Section 2.4. Probably the most complete surveys about multiphase drives are presented in [Levi et al. (2007), Levi (2008)], covering both drive modelling and modulation techniques for the most common multilevel inverter topologies and including comparison of single-sided and open-end drive configurations. In [Levi (2008)] the advantages of each topology are emphasised and the use of the additional degrees of freedom is covered. Other issues, such as fault tolerant operation and multi-motor drives are also discussed in [Levi (2008)]. In Section 2.5, recent advances in multiphase open-end winding drives are reviewed. In particular, modulation methods suitable for drives comprising two two-level inverters have been already developed and tested. Section 2.6 considers research relating to fault detection and drive operation under fault conditions. Post-fault modulation strategies and drive control are in many cases enabled by open-end and/or multiphase structures of the drive. Hence, those results are relevant for topologies presented in this thesis and this is an additional motivation for their consideration. At the same time, modulation strategies derived in Chapters 3, 4 and 6, tested for healthy drive conditions, might be a good starting point for future work, with regard to post-fault operation of the proposed open-end winding five-phase drives. The chapter ends with a short summary, where the emphasis is on the main goals of this research.

2.2. MULTILEVEL THREE-PHASE DRIVES

Nowadays, majority of industrial drives are based on three-phase drives, which are the most convenient, off-the-shelf solution, available for more than thirty years. They are usually supplied with two-level inverters, built with Gate Turn Off (GTO) Thyristors, Insulated Gate Bipolar Transistor (IGBT), Integrated Gate Commutated Thyristors (IGCT) [Akdag (2006)] or power MOSFETs [Baliga (2008), Wilamowski and Irwin (2011), Wintrich et al. (2015)]. Recent advances in the semiconductor technology, such as development of Wide Band Gap devices based on Silicon Carbide (SiC) and Gallium Nitride (GaN), enabled extension of the two-level concept to the high-power application range, but only up to certain limits [Hudgins (2013), Wintrich et al. (2015), Xiucheng et al. (2016)]. Many of the proposed concepts

are still under testing and further development. In many cases, these new technologies are not yet in agreement with safety regulations and application demands. The main issues are related to the stability of high-speed switching, more complex gate driver design, and reliability throughout the operating temperature range required in industry [Lemmon et al. (2014)]. For example, a "normally on" device requires more complex module and/or inverter design and special turn on/off procedures [Xiucheng et al. (2016)], but enables benefits of almost an ideal switch dynamical characteristics.

From this point of view, many problems related to high-power conversion are still not solved and probably fast progress is possible only by combining novel semiconductor technologies and hardware design with a multilevel drive concept, which is often considered as a solution to the limitations of semiconductors in medium and high-power drives [Wilamowski and Irwin (2011), Kouro et al. (2012)]. The initial attempts to apply the multilevel concept to a three-phase drive were made by major industrial drive manufacturers. Among them, probably the first successful implementation of this concept was accomplished by General Electric engineers, reported in [McMurray (1971)]. It is based on cascade connection of two H-bridge modules, made of NPN transistors. Still, this is not suitable for medium- and high-power applications, because of the properties of bipolar transistors. Similarly, the first Flying Capacitor (FC) inverter was introduced as a solution for low-power applications [Dickerson (1971)]. A patent introducing the diode clamped converter was granted in [Baker (1980)]. Most of these topologies ware later reintroduced through academic papers. From that perspective, the diode clamped topology is now better known as the neutral point clamped (NPC) inverter, and was again proposed in [Nabae et al. (1981)], cascaded H-bridge (CHB) in [Marchesoni et al. (1988)] and FC in [Meynard and Foch (1992)]. With further development of semiconductor technology and digital electronics, as inverter control units, use of multilevel drives in industry has grown rapidly. Good reviews of this progress are presented in [Wang and Li (2009), Kouro et al. (2010), Malinowski et al. (2010)]. Three-phase multilevel inverters and modulation strategies are explained and compared in detail in [Rodriguez et al. (2002), Rodriguez et al. (2007), Rodriguez et al. (2009)], providing good classification of converters/inverters topologies, their limitations regarding semiconductor technology, and comparison of performance for medium power applications.

Multilevel three-phase drives are important for this research mainly because of the modulation strategies that have been developed for them. In many cases, these are used as a starting point for developing modulation algorithms for multilevel and multiphase drives, which are reviewed in Sections 2.4 and 2.5 and used in Chapters 3 and 4. For this reason it is important to mention some modulation techniques here which were firstly developed for multilevel three-phase drives. General motivation for developing new modulation techniques can be summarised as achieving sinusoidal voltages across stator phases (elimination of low order harmonics leading to reduction of machine losses), reduction of converter losses that are caused by high frequency switching and improvements in dc-link voltage utilisation.

Due to the existence of leg voltages with more than two voltage levels, more than one carrier is required for CB PWM methods. They can be arranged in several ways and this represents a new degree of freedom, offered by the multilevel topology. Carrier phase disposition techniques are introduced in [Carrara et al. (1992)]. Three different cases are recognised: when all the carriers are alternating in opposition disposition (APOD PWM), all the carriers above the zero value reference are in phase among them but in opposition with those below (POD PWM) and all the carriers are in phase (PD PWM). Both analytical expressions and numerical simulations are developed, in order to compare methods. The multilevel concept is proven to be very useful, not only for high-power drives from the power delivery point of view, but also from the perspective of harmonic performance.

Reduction of specific low-order harmonics is one of the strongest motivations for using multilevel converters. This is firstly implemented with switching at the fundamental frequency, as reported in [Tolbert et al. (1999), Li et al.

(2000)]. The solution is based on calculations of leading and lagging times of switching actions within one switching period. The idea is to represent a phase voltage waveform in the time domain as a Fourier series, and to find switching instances which will supress unwanted harmonic components.

Much better performance can be achieved with higher frequency switching and space vector (SV) algorithms. Instead of having only 8 space vectors, as is the case in two-level three-phase drives, with multilevel inverters a much greater number of voltage vectors is available. For example, for a three-level NPC inverter, $3^3 = 27$ vectors are available (including redundant ones), while with four-level NPC inverter the number of vectors is $4^3 = 64$; as the number of levels increases so too does the number of voltage vectors. A general SV PWM method for multilevel three-phase drives is derived and implemented in [Celanovic and Boroyevich (2001)]. The algorithm is optimized, in the sense of reducing the number of computations required, compared with previously proposed techniques, which is exponentially proportional to the number of voltage levels. Before this improvement, implementation of space vector algorithms was very challenging because of limited processor resources. The most computationally demanding parts of SV PWM algorithms are sector determination and the trigonometric calculations or communication with memory where look-up tables are stored.

Somewhat faster algorithm for this process, namely for reducing calculations in the first sector and identifying the nearest three vectors, is presented in [Peng et al. (2002)]. In [McGrath et al. (2003)], the algorithm from [Celanovic and Boroyevich (2001)] is further optimized, providing the minimal number of switching actions during one switching cycle. Also, comparison between SV PWM and CB PWM (with min-max injection) is performed. Both methods, together with discontinuous PWM, are compared through simulation and experiment. The results showed that these three modulation methods produce almost equivalent output waveforms.

One of the most important properties of the developed modulation strategies is that they can be easily extended to any number of voltage levels. For CHB inverters, an algorithm for developing multilevel modulation, both for linear and over-modulation range is presented in [Gupta and Khambadkone (2007)]. A good comparison of SV and CB PWM methods is given in [Yao et al. (2008)]. Furthermore, a very important and useful survey of multilevel inverters and the suitable modulation techniques is provided in [Rodriguez et al. (2009)]. A number of more sophisticated and implementation dependent modulation techniques are analysed and compared from the inverter point of view, like those with unequal dc-link voltages in the case of CHB inverter, or unequal carrier frequencies.

In recent years, modular multilevel converters (MMC) have gained special attention, due to their modularity and superior dynamic performance [Perez et al. (2015)]. As in the case of many conventional and multilevel converter topologies, MMC is also suitable for dc to ac conversion. In [Brando et al. (2014), Jae-Jung et al. (2015), Kolb et al. (2015)] three-phase MMC drives are analysed. Great progress has been made towards solving stability and cell-capacitor voltage balancing issues in the low-frequency operation region. As demonstrated, various solutions, embedded within modulation and control algorithms, can be applied. This enables closed-loop variable speed ac drive realisation and exploitation of all the benefits of MMC, such as a transformer-less multilevel structure operation and usage of power electronics building blocks (PEBB) concept, which leads to lower costs, easer maintenance and increased fault tolerance [Perez et al. (2015)]. So far, only single-sided MMC drives have been analysed.

All this work shows possibilities for further improvement through merging benefits of multilevel drives with multiphase topologies, stated in Chapter 1. Next, an important step towards multilevel multiphase open-end drives are multilevel three-phase drives for machines with stator windings open on both ends. Some of the most relevant papers for this research are reviewed in the next section.

2.3. OPEN-END WINDING THREE-PHASE DRIVES

One possible way to accomplish multilevel operation is to use a machine in open-end winding configuration, as explained in Chapter 1. In this case, the number of overall phase voltage levels is increased, so multilevel performance can be achieved even with two two-level inverters. The open-end three-phase drive was firstly proposed in [Stemmler and Guggenbach (1993)]. Two- and three-level inverters, supplied from either isolated or non-isolated dc-link voltages, are analysed. At that time, only GTO devices were suitable for medium- and high-power applications. Due to their control limitations, high frequency switching was not an option. As a consequence undesirable current harmonics are present, leading to torque ripple and increased losses. The open-end winding machine configuration is introduced as a possible solution, not only for these issues but also for increasing the power applied to the machine, which is still a strong motivation for OeW drive utilisation.

In the OeW drive, the overall number of phase voltage levels depends not only on the number of levels of the individual inverters, but also on the ratio between two dc source voltages [Bodo (2013)], which are used to supply two individual inverters. In the case of open-end drives comprising two two-level inverters with equal dc-link voltages, the overall number of voltage levels is the same as the three-level single-sided drive [Corzine et al. (1999), Bodo (2013)]. If two dc-link voltages are in the ratio 2:1, the machine supply is equivalent to a four-level single-sided drive [Corzine et al. (1999), Bodo (2013)]. One very important advantage of open-end drives is emphasized in [Corzine et al. (1999)]: the same multilevel performance is achieved by using simpler and therefore more robust inverters leading to improvements to the reliability of the drive, when compared to a single four-level inverter supply. Furthermore, if a fault condition appears, the faulted inverter can be short circuited, and the drive can continue to operate with half of its maximal power. Another, very important advantage of open-end three-phase drives, explained in [Corzine et al. (1999)] is the lower overall production price, provided by avoiding additional diodes and capacitors required for multilevel inverters, and the ability to use readily available off-the-shelf three-phase two-level inverter modules.

The continued interest in open-end multilevel drives is also motivated by some difficulties related to single-sided multilevel drives. For example, by increasing the number of voltage levels, capacitor voltage balancing in FC inverters and unequal voltage sharing among the power semiconductors in both FC and NPC inverters become very important issues [Kouro et al. (2012)]. These problems can be reduced and in some cases completely eliminated, using the open-end drive configuration, since the same number of phase voltage levels can be achieved using simpler inverter topologies.

In [Casadei et al. (2007), Casadei et al. (2008)] a control technique for a multilevel open-end drive with two two-level inverters supplied from two isolated dc sources is presented. By choosing appropriate space vectors, two goals are met; minimisation of commutation frequency per one inverter leg and reduction of common mode voltage. Proposed modulation strategies are tested using simulations and experiments with inverters based on low voltage high current MOSFET modules, using a switching frequency of 10 kHz. This work could be extended to multiphase drives, as will be shown in Sections 2.4 and 2.5.

Two three-level NPC inverters are used in [Corzine et al. (2004), Corzine et al. (2006), Lu and Corzine (2007)] to drive a three-phase induction machine. However, it is shown that only one inverter has to be connected to the dc source (so called bulk inverter) while the second inverter can be used as an active filter, in order to supress undesired low-order harmonics. This drive is known as a hybrid inverter, because two different types of semiconductors are used, one for bulk and one for the conditioning inverter. Since the bulk inverter operates in six-step mode, GTO switches are used, while high frequency switching in conditioning inverter is possible using IGBT or power MOSFET devices. In [Corzine et al. (2004)] joint and separate inverter control are introduced. Joint control concept is based on comparison of eight triangle

carriers with a reference voltage, which is followed by space vector selection designed for capacitor voltage balancing. The second method is based on the implementation of separate inverter control, without communication between the two control circuits. Only the bulk inverter is supplied from an active dc source, while the conditioning inverter is supplied from two capacitors, whose voltage balancing is one of the main issues. Experimental results show that the phase voltage THD is approximately 9%, thanks to the very high number of utilised voltage levels. Similar results are achieved using a different control algorithm, explained in [Corzine et al. (2006)]. Here the conditioning inverter switching is synchronized with the bulk inverter using a voltage edge detector. Additionally, a real-time algorithm for harmonics calculation is used to adjust the switching instances. Control of the bulk inverter is further simplified, using an off-the-shelf integrated controller. The first implementation of an OeW topology in a DTC drive is reported in [Lu and Corzine (2007)] where the open-end topology is compared with the equivalent single-sided cascaded drive. The bulk inverter is based on IGCT modules, which have a higher power rating than IGBTs, but lower maximal switching speed. The conditioning inverter is realised using standard IGBT modules. A similar topology is reported in [Kou et al. (2006)] but for over-distension operation, with the main idea of working with extended modulation index range in order to enhance the number of phase voltage levels by adjusting the proper dc-link voltage ratio of the two inverters. Both converters are three-level NPC, but supplied with dc sources with the voltage ratio of 4:1. Because of this, eleven-level operation is utilised, but only for modulation indexes lower than 1.05. For higher modulation indexes, so-called pseudo eleven-level operation is performed. Some of the expected voltage states are not available in this case and they are missing from the space vector pattern. However, it is shown that this does not have a significant influence on the voltage THD and other power quality parameters.

A similar open-end winding configuration is analysed in [Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015), Pramanick et al. (2015)]. In these cases, only one two-level inverter has an active dc source, while the second two-level inverter is used as an active filter. The overall drive complexity is reduced, when compared to [Corzine et al. (2004), Corzine et al. (2006), Kou et al. (2006), Lu and Corzine (2007)], while the demonstrated harmonic performance is comparable to the three- and four-level single-sided supplies. On the other hand, the overall dc-link voltage is limited to the voltage of the active dc source, which eliminates one of the expected benefits of the open-end winding configuration. Namely, it is expected that the overall dc-link voltage is equal to the sum of two inverters' dc-link voltages, while the maximum phase voltage amplitude is equal to one half of that value. [Chowdhury et al. (2015)] shows that regular drive operation is possible up to only 60% of the overall dc-link voltage, if it is calculated as a sum of two dc-link voltage levels. In other words, in order to employ this topology one has to design one inverter (which has an active dc source) for the full voltage rating, while in configuration with two dc sources both inverters share the overall voltage stress. This presents no problem, since only low frequency switching is performed by the inverter with an active dc source, while the filtering inverter operates with several times lower dc-link voltage. However, in [Ewanchuk et al. (2013)] the overall dc-link voltage boosting is demonstrated, based on the first inverter phase angle adjustment. From that point of view, this topology enables utilisation of high-voltage drives, since semiconductor blocking requirements are in agreement with the existing technology: the inverter with an active dc source can be based on IGCTs or thyristors, while the filtering VSI can be realised using conventional IGBTs or power MOSFETs.

In general, the dc-link voltage ratio for two inverters in open-end configuration can be used to increase the number of available voltage levels. A drive that employs two two-level inverters and a dc-link voltage ratio of 2:1 is analysed in [Reddy et al. (2011), Somasekhar and Reddy (2011), Reddy and Somasekhar (2013)]. Firstly, two SV PWM methods are analysed. Both strategies involve decoupled control of the inverters. The first one, equal-duty-PWM, is based on sharing

the overall phase voltage sinusoidal reference between two inverters in the same ratio 2:1, due to the chosen dc-link voltages. Both inverters have the same switching frequency. The second strategy utilizes switching of the two inverters using switching frequencies that are proportional to their dc-link voltage with respect to the overall dc-link. It is shown that the overall energy losses can be reduced this way. Unexpectedly, the second method also has better phase voltage harmonic performance. Extension of this work, with the main focus on hardware improvements, is presented in [Reddy and Somasekhar (2013)]. Realisation of dc voltage sources is done with three passive rectifiers, supplied from a centre-tapped transformer with the secondary winding ratio 1:2:1. This way, the dc-link source for one inverter is nested, made from the output of the rectifier supplied from the middle secondary winding. The second inverter is supplied from the double dc-link voltage, which is made as the difference of the highest and the lowest potential available at the rectifier outputs. Although the number of components is increased, when compared to the traditional realisation, their ratings are lower, and the overall cost is reduced. Unfortunately, the nested rectifier approach does not provide isolation between two dc-link sources, often required in order to eliminate the zero-sequence current circulation path.

The number of voltage levels of each inverter is another degree of freedom to be considered when designing an OeW drive. In [Somasekhar et al. (2005)] one inverter is built as a cascade of two two-level inverters, giving three-level equivalent. The other side of the open-end drive is supplied with one two-level inverter. Since unequal dc-link voltages are used, six-level modulation is performed, with 91 space vectors, while the dc-link voltage ratio is again 4:1. In [Baiju et al. (2003)], four two-level inverters are used as a supply for an open-end three-phase drive. By supplying every inverter with the same dc voltage, and cascading two inverters on each end of the machine windings, a five-level drive is built. In comparison with [Somasekhar et al. (2005)], this drive has 25% more switching components and one voltage level less. On the other hand, this topology requires lower power rating of the semiconductors, which lowers their price. Although multilevel operation is achieved, there is no need for clamping diodes or additional active switches, which are essential for NPC inverters, or capacitor voltage balancing in case of FC inverters. In comparison with CHB topologies, it is shown that for the same number of voltage levels the topology requires fewer dc voltage sources. The same topology, but with unequal dc-link voltages, is applied to cascaded inverters and analysed in [Lakshminarayanan et al. (2007)]. Hardware solution for dc-link voltage elimination by using non isolated dc-link voltages as presented in [Baiju et al. (2004)] is also applied in [Lakshminarayanan et al. (2007)]. As a side effect, the number of dc voltage sources is again reduced. Similar results are reported in [Kanchan et al. (2006)] for two three-level inverter (3L-OeW-3L) drive. The inverters are made as a cascade of two two-level inverters, supplied from only one dc voltage source, with two bulk capacitors that provide equal voltage splitting between the two inverters. Upper and lower inverters from both sides are connected to the same dc-link rails. As a result, common mode voltage is eliminated. It is also shown that further simplification becomes possible, both in the drive topology and the semiconductor gating circuits. A drawback is the capacitor voltage balancing, which must be taken into account during modulation algorithm development and so special attention is paid to this issue. Cascade connection of converters are again used in [Lakshminarayanan et al. (2008)], where 18-step SV PWM is analysed. Three two-level converters are used, two of them in cascade connection, providing three voltage levels for one set of stator windings, while other side is supplied using a two-level inverter. By using three unequal dc-link voltages, eighteen large space vectors are utilised, providing smoother phase voltage than in case of twelve side polygon [Lakshminarayanan et al. (2007)].

A similar topology improvement is reported in [Mondal et al. (2007)]. The analysed drive is originally reported in [Tekwani et al. (2007b, a)], where it is explained that CMV elimination and dc-link capacitor voltage balancing are achieved at the expense of a reduction in the number of voltage levels, from nine to five. The three-phase open-end drive

comprised two five-level inverters which are formed as a cascade connection of two-level and three-level inverters. After defining the switching pattern which provides CMV elimination, the overall number of switches is reduced, by eliminating two two-level inverters from the circuit and using just two dc voltage sources. The same principles are used in [Mondal et al. (2009)]. In this research, four two-level and two three-level inverters are used, and so thirteen voltage levels are available. As expected, the number of voltage levels is reduced to seven, due to implementation of the common mode voltage elimination algorithm and dc link capacitor voltage balancing as secondary goals for the modulation strategy. As presented, both goals remain feasible even for an equivalent topology with a reduced number of dc voltage sources.

Recently, even more complex OeW drives are reported [Sudharshan et al. (2014), Kumar et al. (2015), Sudharshan et al. (2015)]. In [Kumar et al. (2015)] a seventeen-level three-phase drive is realised, by cascading flying capacitor and floating capacitor H-bridge structures. In [Sudharshan et al. (2014), Sudharshan et al. (2015)] two three-level NPC inverters are employed, together with six H-bridge structures. A high number of voltage levels is enabled by cascading two sets of asymmetric three level inverters with isolated H-bridges on both sides of an open-end winding three-phase machine. The proposed modulation results in 24-step staircase waveform. Unfortunately, in [Sudharshan et al. (2014), Kumar et al. (2015), Sudharshan et al. (2015)] only tests with unusually low voltages are reported, where the overall dc-link voltages are several times lower than actual voltage ratings of individual semiconductors. This leaves open a question whether this kind of drive complexity is suitable and reliable for high-power applications, where isolation issues are very common.

The importance of CMV elimination should be emphasised here. Firstly, in non-isolated open-end drives, existence of CMV can initiate circulating currents [Somani et al. (2010)], which increase the losses in the system and potentially damage some parts of the drive. In the case of an isolated system or a single-sided drive, CMV exists as well, and it has similar effects on the drive. Together with other PWM inverter detriments, such as voltage drops, dead time, asymmetrical and diverse dynamical characteristics of the power semiconductors, CMV can cause bearing currents. This issue is analysed in [Chen et al. (1996), Erdman et al. (1996), Akin et al. (2008)] for the general case, regardless of the drive topology. More details about this topic are provided in Section 2.6, where fault causes, detection and algorithms for the post-fault operation are addressed. The most recent progress regarding OeW drives and common mode voltage reduction in the case of connected dc-links can be found in [Zhou and Nian (2015), Nian et al. (2016)], where a novel zero-sequence current suppression strategy is proposed and experimentally verified.

2.4. MULTILEVEL MULTIPHASE SINGLE-SIDED DRIVES

Single-sided multilevel drives that have more than three phases are considered here. Looking from the SV modulation point of view, the number of available space vectors increases rapidly and, as a consequence, development of appropriate control strategies becomes increasingly more complicated. The increased number of space vectors provides new control possibilities, but also demands sophisticated techniques for vector selection and switching timing calculation. Over the last two decades, different modulation techniques have been developed for the multilevel multiphase single sided drives. Generally, two main modulation concepts are considered; carrier based and space vector (SV PWM) techniques. Since carrier based techniques are independent of the number of phases, the same CB PWM techniques as for a three-phase case can be directly applied to multilevel multiphase systems. Due to the simplicity, they are usually the preferred choice. The existing discussions of carrier based strategies for control of multilevel multiphase

systems are predominantly related to the capacitor voltage balancing of the NPC voltage source inverter for a five-phase passive load [Karugaba et al. (2011)]. The most frequently analysed topology is the five-phase three-level system. This topology is analysed in [Mwinyiwiwa et al. (2006)], where continuous and discontinuous CB PWM schemes are used. An experimental set-up is built to verify the findings, together with a simple, but reliable, bang-bang controller for neutral point voltage balancing.

A simple extension from three-phase to multiphase SV PWM is not possible, in contrast to the CB PWM approach, as explained in [Huang and Corzine (2008)]. With an increase of the number of phases the number of space vectors increases and, even more importantly, the analysis cannot be conducted in a single plane only, as the case is for a three-phase system.

Initial attempts to use SV PWM to control a five-phase three-level inverter, employed techniques originally developed for the three-phase three-level drive. Thus, in [Song et al. (2006)] each sector in the α - β plane is divided into three triangular sub-sectors and only three space vectors per switching period are used. However, this concept does not consider the second plane ($x - y$) and leads to a large amount of low-order harmonics in this plane. In [Huang and Corzine (2008)] new "walking patterns" are used to select the vectors. The algorithm for space vector choice and determination of dwell times is not based on the closest vectors, but on analysis of both vector position and its distance from the commanded voltage reference. It is clearly demonstrated that this algorithm is superior in comparison with CB PWM with harmonic injection (3^{rd}, 5^{th} and 7^{th} harmonics are injected), as far as torque ripple is concerned. To achieve the same performance (torque ripple level), one will have to use CB PWM with three times higher switching frequency.

The algorithm in [Gao and Fletcher (2010)] for a five-phase three-level VSI is the first one that develops SV PWM for multilevel multiphase VSIs using the vector space decomposition (VSD) approach and therefore considers space vector projections in all planes (two in the five-phase case). A modification of the algorithm of [Gao and Fletcher (2010)] is suggested in [Dordevic et al. (2013a)], where comparison of two SV PWM algorithms with three CB PWM techniques is presented for a five-phase three-level VSI. The drive performance is examined for all four cases, and comparison is based on spectrum analysis of phase voltages in both planes separately. It is shown that all four algorithms are very similar with respect to phase voltage THD and HD. Only the CMV component slightly differs, especially for modulation indexes lower than 0.5. Other comparisons based on spectrum analysis for three different frequency bands, centred on switching frequency, are performed as well. It is shown that the differences between the four methods are very small. It is important to emphasize here, that this type of analysis is developed for multiphase drives and it is very useful for understanding how each voltage component affects drive performance. This can enable improvements in modulation strategies. A similar method is used in [Dordevic et al. (2013a)], where five modulation methods are compared and experimentally verified. It is shown how mapping of harmonics and their position in the phase voltage spectrum influence the phase current spectrum. Differences in the low-frequency band are next to nothing, while different modulation methods introduced different harmonic mapping around multiples of the switching frequency. Depending on whether these harmonics belong to the first or the second plane, their influence on motor currents is different because of very different impedances among planes. Finally, it is concluded that CB PWM methods are easier to implement and extend to higher phase numbers.

An SV PWM algorithm for a three-level seven-phase VSI, based on the VSD approach, is for the first time introduced in [Dordevic et al. (2011)], by extending the algorithm of [Gao and Fletcher (2010)]. It is demonstrated that the majority of theoretically available space vectors (2187 in total) are not useful, and only 297 of them can be used after an order-per-sector method is applied. Also, each sector is divided into 18 sub-sectors, in order to easily determine which

vectors are instantaneously used to achieve the reference on average. Finally, dc-link capacitor voltage balancing is taken into account, and redundant space vectors are used for that purpose. Calculation of dwell times is derived from the three-level five-phase case, with focus on elimination of the voltage components mapped in the $x_1 - y_1$ and $x_2 - y_2$ planes. It is noticed that the developed algorithm is far more complicated than for the five-phase case. Basically, all these complicated calculations do not have important effect on real-time drive performance, because they are implemented using mostly offline calculations.

Comparison of SV PWM and CB PWM for the three-level seven-phase drives is reported in [Dordevic et al. (2013b)]. The machine is supplied using a three-level NPC inverter. Similar to the results presented in [Dordevic et al. (2013a)], the only noticeable difference between SV PWM and CB PWM methods is in the implementation, while drive performance is the same. Again, it is found that, not only are the offline calculations more demanding in the case of SV PWM, but also real-time calculation time is about two times greater, in comparison with the CB PWM technique. In case of SV PWM, the algorithm execution includes a large number of memory reads, which is one of the most time-demanding tasks.

A different topology is analysed in [Leon et al. (2010)], based on cascaded H-bridge modules. A modulation algorithm is developed for the general case of a multilevel multiphase single-sided drive, but its implementation is no less complicated than the methods mentioned above. The developed modulation is tested using a five-level five-phase drive, which is also used in [Leon et al. (2010)], where the algorithm is extended with a feed-forward controller, in order to eliminate variation of voltage levels, caused by unbalanced dc voltage sources. This method produced a very good improvement, for the systems that use several dc voltage sources, like CHB inverters. It has been shown that, in case of unbalanced dc voltage sources, feed-forward control can improve drive performance and lower the phase voltage THD by several percent. Similar work is reported in [Celanovic et al. (2001)] for a three-level NPC inverter where a feed-forward controller is proven to be a very robust choice for mitigating any dc-links voltage disturbance, with only one measurement point required.

A topology proposed in [Lopez et al. (2009), Leon et al. (2010)] is also interesting for applications where post-fault operation is required. In [Leon et al. (2010)] dynamic response with feed forward control is tested for the single H-bridge cell fault. Unfortunately, this is done only for one special case, when the inverter supply is asymmetrical with dc-links voltage ratio 2:1, and when the cell with the lower voltage is faulted (short circuited). This is discussed further in Section 2.6.

2.5. OPEN-END WINDING MULTIPHASE DRIVES

Dual-inverter supplies for multiphase machines have only recently been investigated for a number of phases higher than three [Shuai and Corzine (2005), Jones et al. (2010), Grandi et al. (2011b), Levi et al. (2012), Patkar et al. (2012), Bodo et al. (2013a), Sun et al. (2015)]. One of the first attempts to control a multilevel multiphase open-end drive is described in [Shuai and Corzine (2005)]. The suggested topology is made of two two-level inverters, with a dc-link voltage ratio of 2:1, and a five-phase open-end machine. This way, an equivalent to a four-level five-phase drive is achieved. Similarly to the ideas presented in [Corzine et al. (2004), Corzine et al. (2006)], it is proposed that one inverter should be used for the delivering most of the power to the machine, while the other one, made of high-speed power switches, should be used for filtering purposes. This concept will be analysed in detail in this work, together with the lower dc-link capacitor overcharging, phenomenon reported in [Somasekhar and Reddy (2011)].

Important research about a five-phase open-end induction machine supplied with two two-level inverters is reported in [Jones et al. (2010)]. It has been shown that this topology is equivalent to the five-phase single-side machine supplied with a three-level inverter. The first attempt to realise a modulation algorithm is based on independent inverter control, with both inverters have the same switching frequency. From this, additional degrees of freedom are available, because the reference must be shared between modulators, and that could be done with different sharing ratio. In the case of equal reference sharing (ERS), both inverters are operated in the same mode and they deliver the same amount of power to the machine. Unequal reference sharing (URS) provides more possibilities, since the inverters are operating with different modulation indexes. In this case, power distribution can be realised in several ways. For example, one inverter can deliver the majority of the power to the machine, while the second one is used to deliver the remaining power. This feature can be used to transfer energy from one dc source to the other. This is particularly useful in HEV and EV applications where one battery can be used to charge the other. Both ERS and URS methods could be used both with or without equal dc-link voltages, and also with inverters with the same or different number of voltage levels. It can be concluded that a great number of supply combinations and modulation techniques remain to be investigated, and some of them will be addressed in this research, using theoretical considerations, simulations and practical experiments.

The ERS method is analysed in detail, for the five-phase case, and supported with experimental results in [Levi et al. (2012)]. Two different modes are utilised, depending on the modulation index value. For values lower than 0.525, only one inverter is operated, while the second one is used for short circuiting the other side of the stator windings, forming a single neutral point. Basically, in this case the drive can be viewed as a two-level five-phase topology. For modulation indexes greater than 0.525, the second inverter also operates, and reference is shared among the two modulators equally.

Very soon after the initial research efforts, it became clear that CB PWM algorithms could be a good solution as well. This is based on equivalence of SV PWM and CB PWM, as explained in [Dujic et al. (2007), Dordevic (2013), Dordevic et al. (2013a)]. In [Levi et al. (2010)] the modulation algorithm utilises two carriers, each one associated with a two-level inverter. Min-max injection is applied, and two cases are explored. In the first case, carriers are phase-shifted by 180 degrees, while they are kept in phase in the second case. Analysis showed that, for the case when the carriers are in phase, unwanted phase voltage harmonic components around odd multiples of the switching frequency are removed. They exist in leg voltages, but have been cancelled out in the phase voltages.

Carrier based modulation techniques are further investigated and several solutions for an open-end five-phase drive with two two-level inverters are presented in [Bodo et al. (2013b)]. As a continuation of the work presented in [Levi et al. (2010)] several modulation algorithms are developed and compared. The system is driven using a single modulator. The phase voltage reference is compared with two carriers and the modulation algorithms differ by carrier signal arrangement. Thus, phase- and level-shifted PWM (PS PWM and LS PWM) modulations are distinguished. Based on detailed spectrum analyses, the results are compared with earlier research for three-level drives. It can be concluded that both PS PWM and LS PWM techniques are applicable to this topology, since they provide very low phase current and voltage THD, at switching frequency of 2 kHz. General comparison of CB PWM and SV PWM techniques for multilevel single-sided and open-end drives is given in [Bodo et al. (2012), Jones et al. (2012), Bodo (2013)]. Firstly, in [Jones et al. (2012)] several methods are reviewed. For both single-sided and open-end drives CB PWM and SV PWM are explained and their relationships and similarities have been underlined. Performance is compared for URS (open-end) and PD PWM (single-sided drive). The first topology showed better performance for low modulation index values, while both topologies had similar behaviour for modulation indexes greater than 0.525. Two different PWM methods, one for

single-sided and one for open-end drive are compared in [Jones et al. (2012)]. In [Bodo et al. (2012)] PD PWM algorithm is tested using a three-level five-phase single-sided drive and a two two-level five-phase open-end drive. Simulation results are followed with experimental verification, and the work demonstrated that differences in performance between the two topologies are negligible regarding the harmonic distortion of machine's stator voltages and currents.

Another way to create near-sinusoidal phase voltage in multilevel multiphase open-end drives is to operate two inverters with different switching frequencies. This technique is based on the decomposition method explained in [Jones et al. (2011)]. By analysing the space vector distribution in the torque production plane, it becomes clear that the plane can be divided into sub-domains, the shape of which is a polygon, defined by the longest space vectors. In the case of a five-phase multilevel multiphase open-end drive, the decagon in $\alpha - \beta$ plane is divided into 10 smaller decagons. Their centres are defined by space vectors that correspond to phase voltages produced when one inverter works in 10-step operation, while the second inverter is short circuited. This fact is used for the development of a new modulation strategy, explained in [Satiawan and Jones (2011)]. Again, the drive is built with two two-level inverters and a five-phase induction machine. For modulation indexes lower than 0.525 (half of the maximum), the first inverter operates in PWM mode, with a 2 kHz switching frequency, while the second inverter is short circuited. This allows generation of sinusoidal phase voltage, providing the amplitude up to one half of the maximal achievable by the drive. Once the modulation index exceeds what can be achieved using one inverter alone, the second inverter is activated. One inverter operates in 10-step mode, generating only one large vector per switching period, while the second one is operating in PWM mode. Since this PWM inverter must be able to suppress unwanted harmonics from phase voltage, its modulation algorithm must consider the first and the second planes simultaneously. A benefit of this modulation technique is reduction of switching losses, since the first inverter switches at fundamental frequency when the second one operates in PWM mode.

Seven- and nine-phase machines supplied with two two-level inverters are analysed in [Bodo et al. (2013a)]. Development of modulation strategies for these two topologies is based on already known algorithms for five-phase open-end drives. The presented modulation strategies are based on a reference sharing principle.

The asymmetrical six-phase machine (30º between three-phase sets) in the open-end configuration has also been a topic of research. In [Mohapatra et al. (2002)] four two-level three-phase inverters are used, supplied from two unequal dc sources. Only 12-step modulation is performed, but this is enough to demonstrate improvements in stator current waveforms and torque ripple reduction, in comparison with three-phase open-end drives. Further research into this topology is presented in [Grandi et al. (2011a)]. Four independent dc sources are used in order to achieve one more degree of freedom in power sharing control. This leads to a simplification of the modulation, since the drive can be reduced to a dual three-phase system. Hence, the challenges imposed by the nature of the multiphase systems (more than one plane that has to be considered) are not encountered in this configuration. On the other hand, while the control is simplified and high frequency switching is performed, the huge disadvantage of the topology is the requirement for four isolated dc sources.

A symmetrical six-phase drive in open-end configuration, supplied using two isolated two-level six-phase inverters, is analysed in [Patkar et al. (2012)] and a suitable SV PWM method is introduced. It is based on the reference sharing algorithm originally proposed in [Jones et al. (2010)] for the five-phase case. Two inverters are modulated separately using the same switching frequency, but multilevel operation is performed only for modulation indexes higher than 0.5, following the same principles from [Jones et al. (2010), Jones et al. (2013)].

One of the most recent studies about common mode voltage elimination, with a main goal of defining the merits for CMV characterization, is presented in [Karugaba et al. (2012)]. Both single-sided and open-end winding drives are

covered for the five-phase case, and several new notions are proposed for further use, in order to make easier comparison of common mode voltage properties of different drives. These terms, such as dv/dt of CMV, amplitude and total number of voltage levels in CMV, are used in this research, for comparison of common mode voltage waveforms obtained using different modulation strategies.

Very interesting work considering a 20 MW drive that is based on a fifteen-phase OeW structure with two three-level inverters and connected dc-link rails is reported in [Sun et al. (2015)]. After a discussion of the main hardware design issues related to high-power application requirements, detailed analysis of the proposed distributed control is provided. Finally, the full scale experimental validation is given, demonstrating superior phase voltage and current harmonic quality and excellent closed-loop dynamic performance.

2.6. FAULT TOLERANCE AND POST-FAULT MODULATION STRATEGIES

One of the benefits of multilevel multiphase drives is related to a higher number of possibilities for the drive reconfiguration and development of post-fault operation strategies, when compared to three-phase drives. This is based on electrical properties of stator windings and flux production conditions. As long as there are two independent and controllable currents, torque and speed control are possible [Parsa (2005), Levi (2008)]. In areas such as aerospace, oil and petrochemical industries and marine operations, a high degree of reliability is required and so increasing fault tolerance is a very important issue [Thorsen and Dalva (1995), Lezana et al. (2010)].

In [Thorsen and Dalva (1995)] it is shown that semiconductor or driver circuit failure is responsible for about 35% of all faults in the case of two-level drives, excluding their influence on bearing currents [Chen et al. (1996), Erdman et al. (1996), Akin et al. (2008)]. Bearing this in mind, it can be concluded that more complex inverters, with more switches, diodes and driver components, will have a greater share in the total number of drive failures.

In order to exploit the fault tolerance of multiphase drives, the first step is fault detection. Essentially, the majority of fault detection methods are based on current and voltage measurements. Fortunately, the required sensors are included in most commercial drives. Over the last two decades, several approaches have been developed and implemented [Peuget et al. (1998), de Araujo Ribeiro et al. (2003)]. In [Peuget et al. (1998)] fault detection is performed in the $\alpha - \beta$ plane, by observing current vectors, obtained by measuring two out of three stator currents in a two-level three-phase single-sided drive. Fault identification of an open-switch, based on line voltage measurement, is explained in [de Araujo Ribeiro et al. (2003)]. Key points for voltage measurement are found and four methods are introduced, each capable of fault detection in one fourth of the fundamental reference period. Generally, both short circuited and open switch faults could be considered as open leg faults. In both cases, protection fuses will be activated, and switches will be disconnected from the dc supply, becoming, in essence, an open leg fault.

The second important topic is post-fault control. Firstly, post-fault control strategies are developed for three-phase drives. Drive reliability could be improved by adding one extra inverter leg and additional switches, in order to reconfigure the supply circuit, and replace the faulted leg [de Araujo Ribeiro et al. (2004)]. In essence, the modulation strategy remains the same, and only the driving signals are rerouted after inverter reconfiguration. An important consideration is the removal of the faulted leg from the system, by opening the two protection fuses which are standard part of every inverter leg.

In the case when one phase or inverter leg is faulted in a multiphase drive, circuit reconfiguration is not necessary. With proper changes in modulation strategy, the drive can continue operation with reduced power. In [Jacobina et al.

(2004)] post-fault modulation is derived and experimentally verified for a five phase single-sided drive. Initially, the case when one phase is disconnected from the VSI is analysed and it is shown that current projection in the first plane can remain the same as during pre-fault operation, while phase currents are unbalanced. The solution is based on minimal copper losses criterion, and torque production is not taken into account. The same principle is used for the case when two phases are faulted. In both cases, the unchanged pre-faulted rotational transformation is used, having two planes for control, with asymmetrical space vector distribution.

Post-fault modelling and control of a five-phase synchronous machine is presented in [Ryu et al. (2006)]. In essence, this method treats the faulted machine as an asymmetrical machine. The number of phases is equal to the number of healthy phases. This way, the transformation matrix is changed, which suggests that in the case of a five-phase machine with one faulted phase, post-fault algorithm should consider the system as a four-phase asymmetrical drive. This algorithm is reused again in [Guzman et al. (2011)], where the modelling method is used in conjunction with a predictive current control algorithm to achieve either minimal copper losses or maximal torque production.

Similar modelling methods are used for developing post-fault control techniques for seven-phase drives in [Tani et al. (2012)]. Stator currents are measured and their space vector representations are used for fault detection and localization. Firstly, a general algorithm for *n*-phase machine is derived, for fault detection and post-fault operation. The proposed method is then tested on a seven-phase machine using simulations and experiments, for cases of one and two faulted phases.

Another interesting approach to modelling of faults in multiphase drives is presented in [Apsley and Williamson (2006)], where each stator winding is considered as a separate, concentrated winding, with its own contribution to the overall magneto-motive force (MMF). The developed model brings a more general approach and direct insight of the impact of a fault in stator windings on the MMF distribution. At the same time, it enables the analysis of more complex faults, such as interphase short circuits, while being applicable to an arbitrary number of phases. An open circuit fault mitigation method, based on the usage of complete drive model with additional constraints that effectively model zero current in the faulted drive phase is proposed in [Apsley (2010)]. It is shown that instead of switching between two drive models in order to examine fault conditions, one may use PI controllers to force the current in faulted phase to be zero, which presents the open circuit fault. This way, a complete machine model can be retained, even in the case of multiple faulted phases. The major advantage of this modelling approach is its applicability to the various fault conditions, while so-called reduced-order models have to be developed for each case separately.

The majority of the reported research is based on the assumption that an open phase fault takes place, meaning that both the active semiconductor and its antiparallel diode are not conducting. This simplification cannot be justified in many cases and implementation of the proposed algorithm requires additional hardware which should be used to completely disconnect faulted drive phase from the circuitry. Recently, in [Guzman et al. (2015)] an analysis of the driver and/or IGBT fault is provided, assuming healthy condition of antiparallel diode. Compared to an open phase fault case, it is shown that existence of freewheeling path in faulted phase can be treated as external system perturbation, which is manifested in additional common mode voltage components, resulting in lower torque production and additional copper losses.

The only known examples of fault strategies for a multilevel open-end drive are presented in [Grandi et al. (2011a), Grandi et al. (2012)], where a six phase open-end machine with two three-phase windings is analysed. In both papers a fault resulted in the loss of three-phase inverters. Three possible cases are compared in [Grandi et al. (2011a)], regarding a number of faulted inverters. Firstly, a straightforward operating regime is proposed, whereby the faulted

inverter is removed from the circuit using bypass switches and the corresponding stator ends short circuited. This way, one side of the three-phase winding will form an isolated neutral point, while the other one will remain connected to a functional inverter, if only one inverter on that winding is faulted. When two inverters are faulted, two cases are possible; both three-phase windings have one healthy supply, while the other side is short circuited, or one three-phase winding is supplied using two healthy inverters, while the second winding is completely non-operational. The analysis in [Grandi et al. (2011a)] is undertaken from the standpoint of power delivered to the machine, and the fault strategies are compared from this point of view. The case when only one inverter is faulted is analysed in more detail in [Grandi et al. (2012)], where two post-fault strategies are presented. The first strategy is to remove one more (healthy) inverter from the other set of stator windings, in order to provide a balanced supply in single-sided manner. Unfortunately, this approach removes all benefits of open-end winding, while one huge part of hardware is unused (healthy three-phase inverter and its power source). The second strategy uses all three healthy inverters, which equally share the total drive power. Loss of one inverter in this case means that remaining conversion power units can operate with a reduced power rating only in order to provide a balanced supply of all machine windings. Post-fault strategies for six-phase open-end drives with dual three-phase windings, supplied with four two-level inverters, are summarised in [Grandi et al. (2011a)]. According to the number of faulted inverters, three cases are distinguished, and drive performance is compared with healthy conditions. Different solutions are proposed, regarding number of faulted inverters and number of three-phase winding sets that can be used in post-fault operations.

A nine-phase permanent magnet machine with three sets of three-phase windings, supplied from three two-level inverters, is analysed in [Ruba and Fodorean (2012)]. Fault tolerant strategies are based on mixed hardware and software solutions, where an additional inverter leg is added to each inverter with the purpose of compensating a fault in one of the phases. A control algorithm for post-fault operation is developed for this case, without any extension to multiple faults, that can take away several phases from the nine-phase drive.

So far, very little attention is paid to post-fault operation of multilevel inverters. Still, in [Lezana et al. (2010)] different topologies of multilevel inverters are reviewed, from the point of view of post-fault reconfiguration strategies and limitations for post-fault operations. Several types of solutions are analysed, with and without additional power components. It is also shown that the reliability of NPC inverters can be improved with the addition of a few extra components, like in the case of two-level inverters. For example, the NPC inverter can become more fault-tolerant, without any oversizing of components, by replacing clamping diodes with IGBTs with antiparallel diodes. This provides the possibility to reconfigure faulted inverter leg and to continue operation with reduced power. Limitations of this kind are very important for developing post-fault modulation strategies. Other topologies are analysed as well. CHB is proven to be the most convenient solution for applications where fault-tolerant operation is required. Beside possibilities for cheap hardware solutions and protection measures, this inverter type offers the possibility of fault compensation with modification of control and modulation algorithms. More details about this can be found in [Lezana and Ortiz (2009)].

From this review of research efforts related to fault issues in machine drives, it can be concluded that fault tolerant control strategies for multiphase multilevel open-end drives have not been developed so far. However, having in mind complexity of this research field, it is clear that these topics should be covered in a separate, more detailed study. Therefore, this thesis considers only healthy operation of the proposed topologies (in Chapters 3, 4 and 6), and only a few guidelines regarding possible post-fault strategies are provided. Most of them are based on circuit reconfiguration using only existing hardware, where one inverter (i.e. its healthy switches) can be used for star connection formation, enabling post-fault operation with a reduced number of voltage levels and overall power.

2.7. SUMMARY

In this chapter, a review of the literature relevant to this research is given. All mentioned patents, books and scientific papers are classified according to the topology of the drive in order to clearly follow the development area of medium- and high-power drives. From that, it can be predicted that interest in multilevel multiphase open-end drives will increasingly grow in the future.

This research is focused on the modulation techniques for open-end winding drives, made from five-phase induction machine and with inverters supplied with equal and unequal dc-link voltages. The influence of inverter voltage source configuration in multilevel multiphase open-end drives is the main focus. The most important findings presented in Sections 2.3, 2.4 and 2.5 are analysed. The presented modulation strategies are extended to the proposed drive topologies in Chapters 3 and 4. Special attention is given to capacitor voltage balancing and power flow analysis in Chapter 5. Bulk and conditioning for one novel drive configuration is analysed in Chapter 6. Based on the recent progress in this field, reported in this survey, it is clear that novel drive performance and modulation strategies should be tested within closed-loop control, which is nowadays inevitable in industrial applications. This topic is covered in Chapter 7, where several drive configurations and modulation strategies are tested under rotor field oriented control.

Chapter 3

FIVE-PHASE OPEN-END WINDING DRIVES WITH TWO TWO-LEVEL INVERTERS

3.1. INTRODUCTION

The simplest open-end winding topology is the one that employs two two-level inverters, used to supply the machine from two sides of its stator windings. This drive structure is referred in this thesis as 2L-OeW-2L, illustrating its configuration. In the literature review, presented in the previous chapter, several publications about this topology are reported. The majority of the research efforts have focused on three-phase drives with some recent publications considering the multiphase case. Regardless of the number of phases, it has been demonstrated that this simple OeW configuration is able to provide multilevel phase voltage waveforms. The number of levels in the phase voltage waveforms depends not only on the modulation strategy, but also on the ratio between the two dc-link voltages, used to supply the two inverters.

The results in this chapter were presented in several conference publications [Darijevic et al. (2013a), Darijevic et al. (2013b), Jones et al. (2014), Darijevic et al. (2015a)] and one journal paper [Darijevic et al. (2016)]. The aim of this chapter is to provide a more general and unifying analysis of 2L-OeW-2L drives, with the main focus on the influence of the dc-link voltage ratio on the harmonic performance of the drive. The topology is analysed in detail in the next section, using the so-called equivalent drive model for modulation algorithm development. Two different kinds of carrier based (CB) pulse width modulation (PWM) methods are considered in this chapter.

Firstly, an attempt is made to adopt well-known CB PWM methods for single-sided multilevel drives to the 2L-OeW-2L drive. It is explained why in this case the two inverters cannot be treated separately, but rather as a coupled entity. It is demonstrated using simulation results that this approach indeed leads to true multilevel output waveforms. Unfortunately, this approach suffers from one drawback, related to dead-time and simultaneous switching on the two OeW sides. It is shown that this issue can be mitigated with modification of the modulation algorithm. Next, detailed simulation results are used in order to determine the optimal dc-link voltage ratio, and experimental results for selected cases are presented and discussed. The final section is dedicated to so-called decoupled modulation strategies, which are based on reference sharing algorithms.

3.2. MODELLING AND ANALYSIS OF THE TOPOLOGY

The topology under consideration is shown in Fig. 3.1. It consists of two two-level voltage source inverters (VSI_1 and VSI_2), supplied from two dc voltage sources (V_{dc1} and V_{dc2}, respectively) and a five-phase open-end winding machine.

In Fig. 3.1 each of the power switches is formed using as a pair of one IGBT and one antiparallel diode and is referred to the rest of the text as IGBT+D structure. These semiconductors represent a current bidirectional two-quadrant active switch, basic building block of any VSI. Each inverter leg comprises two IGBT+D, denoted in Fig. 3.1 with

subscript "up" and "dn", indicating component location (up or down). Active devices are denoted with S_{upjk} and S_{dnjk} for j^{th} inverter (j = 1 or 2) and k^{th} drive phase (k = 1, 2, 3, 4 or 5). Likewise, antiparallel diodes are labelled with D_{upjk} and D_{dnjk}. These labels will be used in the rest of the analysis, where conduction states and properties of individual components are of interest.

For modulation strategy development, voltage source inverters are usually considered as PWM signal amplifiers, where IGBT+D structure is treated as an ideal bidirectional switch. In most of the cases, at least for hard switching applications, this approach seems to be sufficient. Analysis can be vastly simplified using switching states, which are representing the one IGBT+D, rather than considering each semiconductor independently. Let us define switching state S_{jk}:

- S_{jk} is equal to 1 if S_{upjk} or D_{upjk} is conducting. Disregarding voltage drops on semiconductor device, inverter leg voltage v_{jk}, measured with respect to v_{n1}, is equal to V_{dcj}.
- S_{jk} is equal to 0 if S_{dnjk} or D_{dnjk} is conducting. In this case, v_{jk} is equal to 0.

As known from VSI operation theory, the only technically possible state in which previous definitions are not valid is when both S_{upjk} and S_{dnjk} are conducting at the same time. However, this state is not allowed, since it would result in dc-link short circuit. In order to avoid this situation, one has to make sure that turn-off transient of previously conducting active switch is over, before complementary active switch in the same leg is turned on. The simplest solution is to introduce so-called dead time interval in gating signals, during which both gating signals (g_{upjk} and g_{dnjk} in Fig. 3.1) are low. During dead time interval, leg voltage is determined with conduction of antiparallel diodes, which depends on load current sign. Final phase voltage is formed as voltage potential difference of two inverters' leg voltages and common mode voltage (CMV). Therefore, phase voltage waveform can be obtained using:

$$v_k = v_{1k} - v_{2k} - v_{n2n1} \tag{3.1}$$

where CMV is calculated as:

$$v_{n2n1} = v_{n2} - v_{n1} = \frac{1}{5}\sum_{k=1}^{5}(v_{1k} - v_{2k}) \tag{3.2}$$

This way, both v_k and CMV are expressed as a function of controllable voltages in the system – leg voltages of the two inverters. Since both inverters can produce two different leg voltage values, 0 and V_{dcj}, which correspond to switching states 0 and 1, four different combinations are possible, per phase. The drive analysis can be further simplified using so-called equivalent drive model, which represents one drive phase as shown in Fig. 3.2. Under the assumption that the two lower dc-link voltage potentials are equal ($v_{n2} - v_{n1} = 0$), one is able to derive exact phase voltage levels that correspond with each of four switching combinations, as summarised in Table. 3.1.

Table 3.1 indicates that in the case of an open-end winding drive one has to consider both dc-link voltage levels. In order to generalise and simplify the analysis, dc-link voltage ratio r is introduced:

$$r = \frac{V_{dc1}}{V_{dc2}} \tag{3.3}$$

while the overall dc-link voltage is defined with:

$$V_{dc} = V_{dc1} + V_{dc2} \tag{3.4}$$

In this study, only $r \geq 1$ is considered, i.e. $V_{dc1} \geq V_{dc2}$. Any other dc-link voltage ratio would be equivalent with the case in which two inverters have swapped their places and due to drive symmetry (VSI_1 and VSI_2 have identical structure) this would again result in the same 2L-OeW-2L structure and performance. Using new variables, data from Table 3.1 can be given in the generalised form as in Table 3.2, where leg and phase voltages are normalised with V_{dc}.

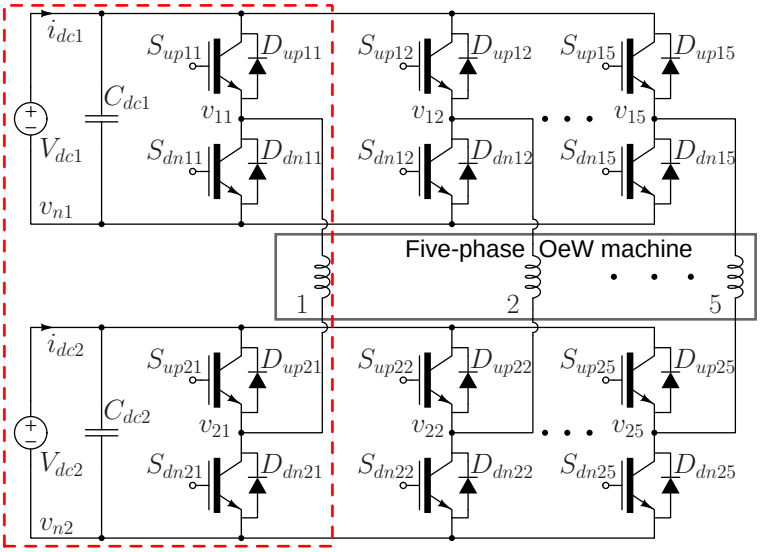


Fig. 3.1. Five-phase multilevel open-end winding drive with two two-level inverters (2L-OeW-2L structure).

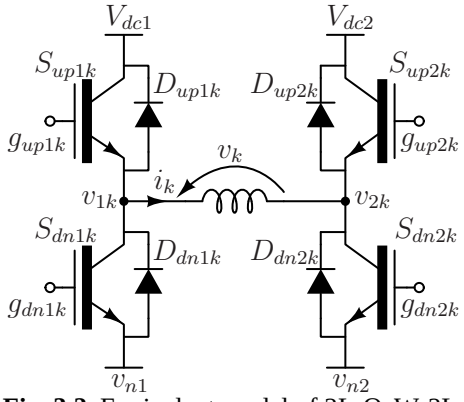


Fig. 3.2. Equivalent model of 2L-OeW-2L.

Table 3.1. Relationship between switching states, leg and phase voltages.

N	S_{1k}	S_{2k}	v_{1k} [V]	v_{2k} [V]	Equivalent v_k [V]
1	1	1	V_{dc1}	V_{dc2}	$V_{dc1}-V_{dc2}$
2	1	0	V_{dc1}	0	V_{dc1}
3	0	1	0	V_{dc2}	$-V_{dc2}$
4	0	0	0	0	0

Table 3.2. Relationship between switching states, normalised leg and phase voltages.

N	S_{1k}	S_{2k}	v_{1k}/V_{dc}	v_{2k}/V_{dc}	Equivalent v_k/V_{dc}
1	1	1	$r/(r+1)$	$1/(r+1)$	$(r-1)/(r+1)$
2	1	0	$r/(r+1)$	0	$r/(r+1)$
3	0	1	0	$1/(r+1)$	$-1/(r+1)$
4	0	0	0	0	0

Analysis of Tables 3.1 and 3.2 yields several important conclusions:

- Difference between minimal and maximal voltage levels is always $V_{dc1} - (-V_{dc2}) = V_{dc}$. Hence, if this inverter structure is to be compared with a single-sided multilevel drive, the dc-link voltages should be equal. However, dc-link voltages of individual inverters in 2L-OeW-2L structure are lower than V_{dc} in the case of a single-sided supply. This makes multilevel inverter structures based on OeW concept easier to produce, with regard to semiconductor module cost and count, blocking voltage limitations, capacitor bank cost and size.

- For $r = 1$, 2L-OeW-2L drive can produce three voltage levels, since switching state combinations 1 and 4 (Table 3.2) result in the same voltage level. Hence, the 2L-OeW-2L drive with equal dc-link voltages corresponds to a three-level single-sided machine supply. Available voltage levels are equidistant: $-V_{dc}/2$, 0 and $V_{dc}/2$, with respect to v_{n1} in Fig. 3.1.
- For $r \neq 1$, the 2L-OeW-2L drive acts as a four-level drive, since all switching states result in a different voltage level.
- From all unequal dc-link voltage cases ($r \neq 1$), only $r = 2$ results in equidistant voltage levels: $-V_{dc}/3$, 0, $V_{dc}/3$ and $2 \cdot V_{dc}/3$. Only this case is fully comparable with single-sided multilevel supplies, since they are usually employing equidistant voltage levels.
- Common mode voltage dc component is $V_{n2n1} = (V_{dc1} - V_{dc2})/2$. This voltage potential is always in the middle between minimal and maximal voltage level.

The imposing question from the previous analysis is: what is the optimal value of parameter r? One approach, based on the analysis of drive harmonic performance is used in the two following sections, where coupled and decoupled modulation methods are introduced for the 2L-OeW-2L drive.

So far, it has been demonstrated that the 2L-OeW-2L structure is equivalent to some single-sided multilevel topologies. From that point of view, it seems natural that well-known modulation methods, used for multilevel drives, can be applied to the open-end winding topology. As already stated in the introduction, modern drives usually employ CB or SV PWM for inverter control. Previous research results showed that CB PWM can achieve the same level of harmonic performance and dc-link voltage utilisation as the SV PWM methods. On the other hand, it is demonstrated that CB methods are computationally less demanding [Dordevic et al. (2013)]. Namely, regardless of the number of phases and number of voltage levels, the final PWM signal is always formed using simple reference comparison with a carrier signal. On the contrary, complexity of SV methods rapidly rises with an increment of number of the drive phases or voltage levels. Hence, in this research only CB PWM methods are analysed in detail. Space vectors are only used to visualise the influence of r on drive performance and capabilities. In Fig. 3.3, space vectors generated by two VSIs, for different values of r, are shown. Resulting phase voltage space vectors are depicted in Fig. 3.4. Space vectors in the two planes are determined with:

$$\begin{aligned} \underline{v}_{\alpha-\beta} &= (2/5)\cdot\left(v_1 + \underline{a}\cdot v_2 + \underline{a}^2\cdot v_3 + \underline{a}^3\cdot v_4 + \underline{a}^4\cdot v_5\right) \\ \underline{v}_{x-y} &= (2/5)\cdot\left(v_1 + \underline{a}^2\cdot v_2 + \underline{a}^4\cdot v_3 + \underline{a}^6\cdot v_4 + \underline{a}^8\cdot v_5\right) \end{aligned} \tag{3.5}$$

where $\underline{a} = e^{2\cdot\pi\cdot j/5}$. In this case, j stands for imaginary unit, $j^2 = -1$. Since $v_{n2n1}\cdot(1 + \underline{a} + \underline{a}^2 + \underline{a}^3 + \underline{a}^4) = 0$, using (3.5) one gets:

$$\begin{aligned} \underline{v}_{\alpha-\beta} &= \underline{v}_{\alpha-\beta(11,12,13,14,15)} - \underline{v}_{\alpha-\beta(21,22,23,24,25)} \\ \underline{v}_{x-y} &= \underline{v}_{x-y(11,12,13,14,15)} - \underline{v}_{x-y(21,22,23,24,25)} \end{aligned} \tag{3.6}$$

In (3.6) the two space vectors on the right-hand sides of the two equations are corresponding voltage space vectors of the five-phase two-level VSIs. Each two-level five-phase inverter can produce 31 unique vectors [Jones et al. (2010)]. Since the drive comprises two two-level five-phase inverters, the overall number of switching states is $2^5 \cdot 2^5 = 1024$.

In the case of a three-level drive ($r = 1$), both VSI_1 and VSI_2 produce the same space voltage vectors (Fig. 3.3a). From the overall number of switching states, only $3^5 - 2^5 = 211$ produce unique voltages, which is equal to the number of available phase voltage space vectors [Levi et al. (2012)]. The overall number of available magnitudes is 18, as shown in the 1st and the 9th sector in Fig. 3.4a, where radial and circular lines corresponding to each unique vector are used to indicate the plane coverage. From this point of view, it can be concluded that vectors are uniformly distributed.

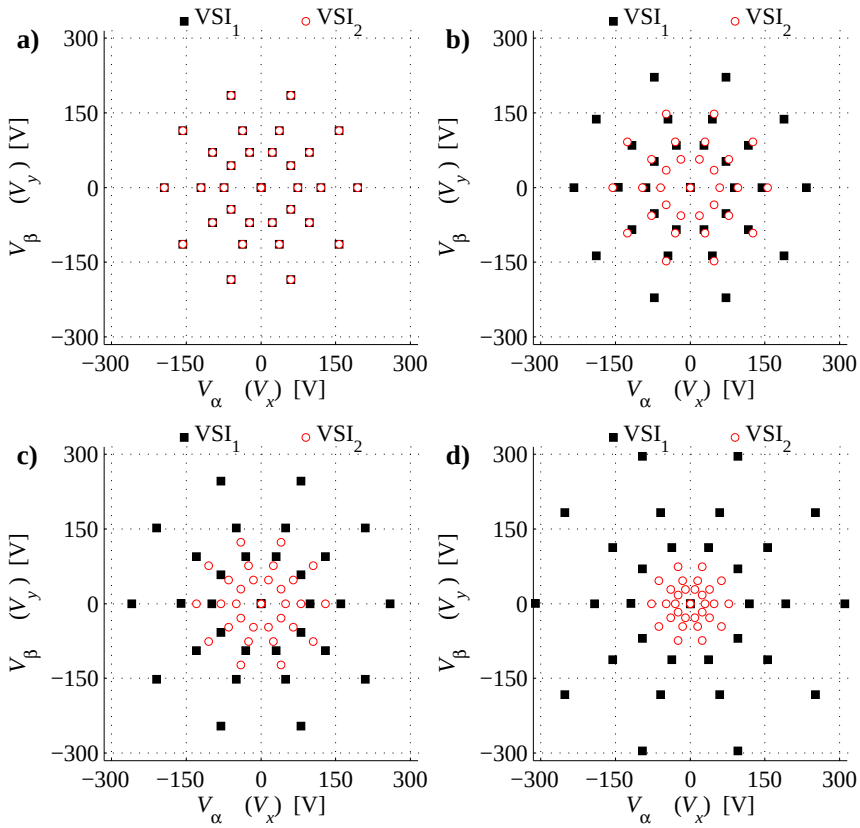


Fig. 3.3. Leg voltage space vectors of two inverters obtained with: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

In the case of a four-level drive, there are $4^5 - 3^5 = 781$ unique space vectors. With r = 1.5 and 4, there are 61 different space vectors magnitudes, while r = 2 provides 51 unique magnitudes. With r = 1.5 some of the produced leg space vectors of VSI_1 and VSI_2 have approximately the same amplitude and position, due to small difference in their dc-link voltages. Hence, resulting space vectors are grouped together, which eliminates the expected benefits from a larger number of available space vectors, when compared with r = 2. In Fig. 3.4d one can observe a different kind of clustering – in this case phase voltage space vectors are clearly distributed around space vectors produced with VSI_1, which has 4 times higher dc-link voltage then VSI_2. This seems to be a more promising case than r = 1.5, since the space vectors are uniformly distributed at least in the inner part of the plane.

Due to the increased number of phases, in order to fully utilise the benefits of the proposed topology, one has to develop a far more complex space vector algorithm than those proposed for the three-phase OeW drive. Implementation of such an algorithm is demanding regarding computation time, as shown in [Dordevic et al. (2013a)]. Additionally, since the distribution of space vectors is highly dependent on r, different SV algorithms should be developed for different dc-link voltage ratios. With CB PWM however, the same scheme can be applied regardless of r. This conclusion comes from Table 3.2, which shows that the distance between minimal and maximal normalised voltage level is always equal to 1, while the two inner voltage level positions are dependent on r. Since the distances between voltage levels define the amplitudes of carrier signals for level shifted (LS) CB PWM methods, it is clear that information about the dc-link voltage ratio is naturally incorporated in the CB PWM algorithm. Keeping this in mind, one is able to develop a universal algorithm, which can be applied to any 2L-OeW-2L drive, regardless of the number of phases and dc-link voltage ratio. Other CB PWM methods, such as those with phase-shifted carriers, are not in the scope of this research, since it was proven in earlier research efforts that the most promising of them are equivalent with some LS CB PWM methods [Wilamowski and Irwin (2011)].

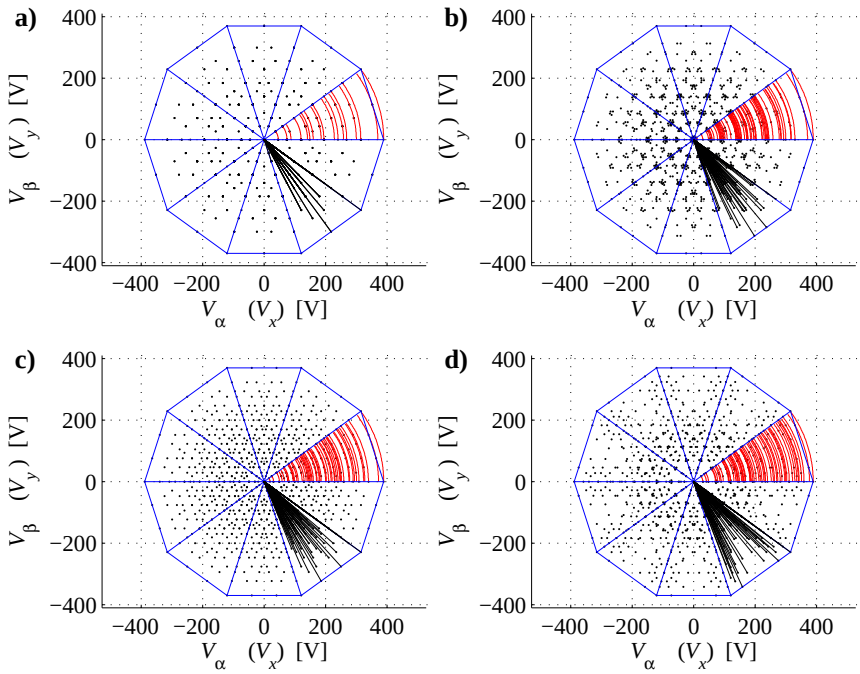


Fig. 3.4. Phase voltage space vectors, obtained with: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d). Red radial lines in the first sector and black lines in ninth sector lines that correspond to unique vectors are used to indicate the plane coverage.

3.3. COUPLED CARRIER BASED MODULATION METHODS

3.3.1. PRELIMINARY ANALYSIS

As already stated, one of the major advantages of SV over CB PWM is better dc-link voltage utilisation. Recent studies have shown that the same maximal utilisation can be achieved with CB PWM as well, by adding the zero-sequence injection to the sinusoidal leg voltage reference signals [Levi et al. (2008)], calculated as:

$$v_{inj} = -\frac{1}{2}\cdot\left(v_{min} + v_{max}\right) \tag{3.7}$$

where v_{max} and v_{min} stand for the maximum and minimum value, respectively, of the normalised sinusoidal phase voltage references. The final phase voltage references for open-loop constant V/f control are generated using the following expression:

$$v_k^*(t) = R_{offset} + \frac{M}{2}\cdot\sin\left(M\cdot\omega_n\cdot t - \frac{2\cdot\pi}{5}\cdot k\right) + v_{inj} \tag{3.8}$$

In the case of the five-phase machine, dc-link voltage utilisation increased using (3.8) to $M_{max} = 1/\cos(\pi/10) = 1.05$. Modulation index M in (3.8) is defined as a ratio between the reference amplitude and $V_{dc}/2$. Equation (3.8) provides phase voltage references for V/f control, since sine wave amplitude is normalised with M, as is the nominal angular frequency, $\omega_n = 2\cdot\pi\cdot f_n$, where f_n is nominal machine frequency. The phase shift in (3.8) is $2\cdot k\cdot\pi/5$ for the k^{th} drive phase. In this research, only range $0.1 < M < 1$ is analysed, mainly because of the practical constraints related to dead-time effects. Here, only linear modulation range is analysed, while voltage boost in low modulation index range is neglected.

The second important part of any CB PWM method development is defining the carriers' disposition. It is well known that the number of carrier signals for LS methods is always equal to the overall number of voltage levels minus one. Hence, a three-level inverter requires two carrier signals, while any four-level inverter employs three carriers, and so on. The situation is the same for OeW drives. For this reason the whole drive structure can be considered as a coupled entity, meaning that the overall number of voltage levels and their values are the only parameters that determine carrier

signal disposition and amplitude. In other words, since development of CB PWM strategies for single-sided multilevel drives always considers all possible switching state combinations that can be obtained in one drive phase, the same rule must be used for OeW drives, in order to obtain identical waveforms. Previous research results about modulation strategies for multilevel inverters show that symmetrical carrier dispositions result in optimal harmonic performance [Holmes and Lipo (2003)]. This narrows down the overall number of possible carrier arrangements to:

- CB PWM with carriers in phase disposition (PD).
- CB PWM with carriers in alternate phase opposite disposition (APOD).

Carriers for four different values of r are shown in Figs. 3.5 (PD PWM) and 3.6 (APOD PWM). These cases correspond to space vector distributions in Fig. 3.3 and 3.4. Table 3.2 shows that 2L-OeW-2L drive can operate as a three- or four-level inverter, depending on the dc-link voltage ratios. Before complete derivation of the modulation algorithm, it is beneficial to analyse Figs. 3.3-3.6, together with data in Tables 3.1 and 3.2:

- Carriers divide the overall phase voltage co-domain into several so-called reference zones. Their number is equal to the number of carriers.
- The distance between two inner voltage levels is proportional to r and so the middle carrier amplitude (C_2 in Figs. 3.5 and 3.6 b, c and d) becomes higher with increment of r.
- Data from Table 3.2 suggests that C_2 amplitude is equal to the difference between the dc-link voltages, normalised by the overall dc-link voltage $(V_{dc1} - V_{dc2})/V_{dc}$. Clearly, extreme values of r will lead to higher disproportion in carrier amplitudes. This is valid for two cases, when value of r is very close to 1 and much higher than 2.
- For some values of M, the complete phase voltage reference will be placed in the middle reference zone during one complete fundamental period. This means that 2L-OeW-2L drive will act as a two-level drive, since only two inner voltage levels can be triggered when v_k^* is compared with C_2. For an arbitrary value of $r > 1$, as long as $M < M_{max} \cdot (r - 1)/(r + 1)$, two-level operation will take place. Clearly, for $r >> 2$, the drive will operate as two-level for a wide modulation index range.

Disproportion of carrier amplitudes leads to higher ripple content during one fundamental period, since available voltage levels are either very close or very far from the instantaneous reference value. In these situations, dead-time effects are increased as well, since the final duty ratio will be close to 0 or 1. This has a similar impact on harmonic performance as clustering of the phase voltage space vectors in Fig. 3.4 and in [Corzine et al. (1999)].

Based on the previous analysis, it can be concluded that only dc-link voltage ratios around $r = 1$ and 2 are promising, regarding harmonic content of produced phase voltages. However, in order to fully investigate what is/are the most suitable values of r, one has to include other parameters, such as dead-time effects on low-order harmonics. Regardless of the chosen carrier arrangement, one has to derive the relations between reference comparison with the carriers and actual switching states. As known from CB theory, reference comparison with each of the carrier signals is associated with logical variables, which have the value of logical high if the reference instantaneous value is bigger than the carrier instantaneous value, otherwise comparison returns logical low. Let us define for this purpose logical variables A_{ik}, which correspond with k^{th} phase voltage reference comparison with i^{th} carrier signal (Figs. 3.5 and 3.6):

$$A_{ik} = \begin{cases} 1 & if \quad v_k^* > C_i \\ 0 & if \quad v_k^* \le C_i \end{cases} \tag{3.9}$$

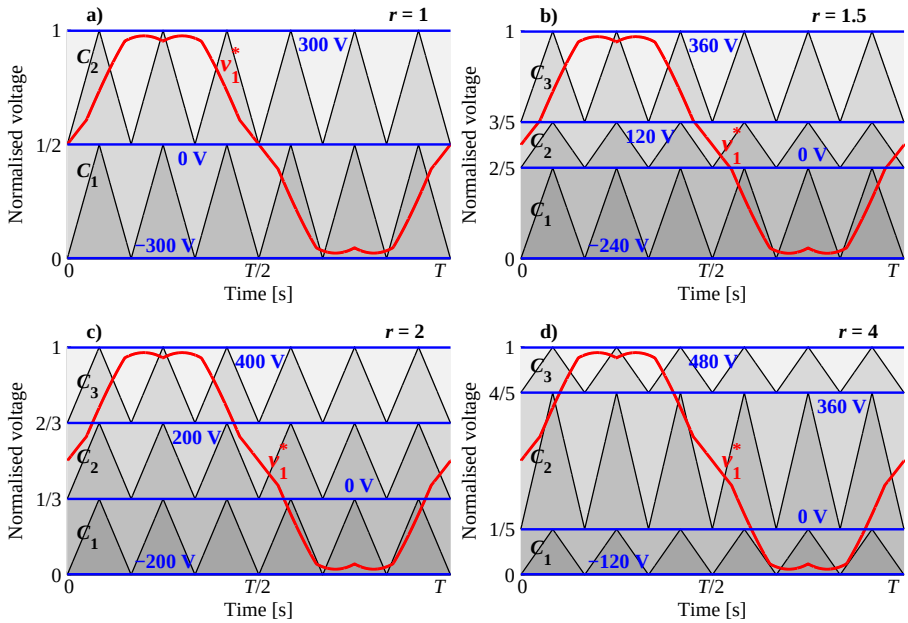


Fig. 3.5. PD PWM: Phase voltage reference and carrier signals for r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

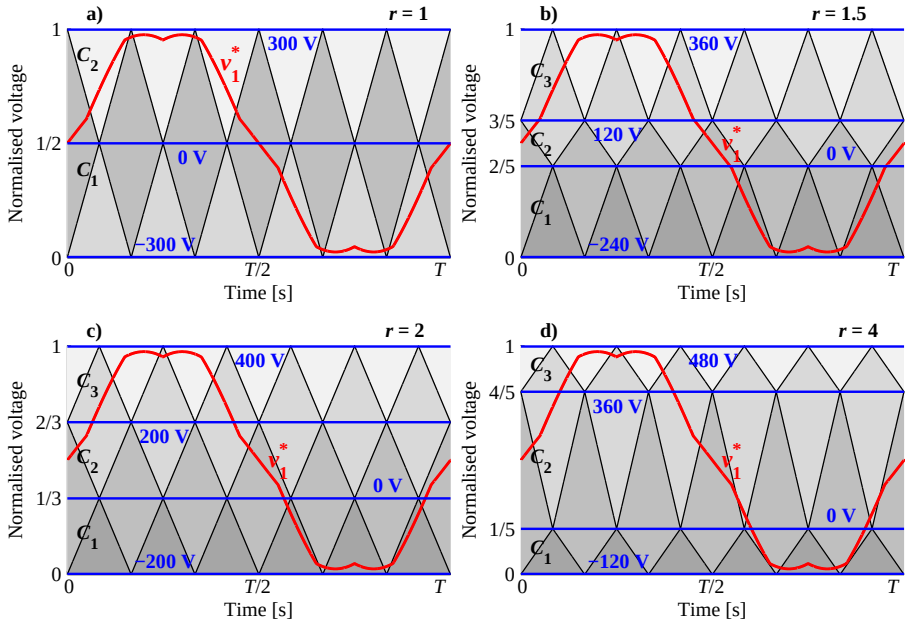


Fig. 3.6. APOD PWM: Phase voltage reference and carrier signals for r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

The next stage in the modulation strategy development is to establish a relationship between A_{ik} and the desired switching states that should be triggered for A_{ik} = 0 and A_{ik} = 1. In general, this should be done for each IGBT+D pair in the circuit. Due to the complementary nature of switches in each leg, it is sufficient to establish relations between A_{ik} and S_{jk}. The final step is to implement dead-time, in order to obtain gating signals g_{upjk} and g_{dnjk} from S_{jk}.

3.3.2. CB PWM FOR THE EQUAL DC-LINK VOLTAGE CASE

Firstly, let us analyse the simplest case, when both inverters are supplied with equal dc-link voltages (r = 1). The equivalent model in Fig. 3.2, Tables 3.1 and 3.2, and carrier arrangements in Figs. 3.5a and 3.6a indicate that reference comparison with C_1 provides switching state for VSI_1, while VSI_2 is modulated with C_2. The control diagram is shown in Fig. 3.7.

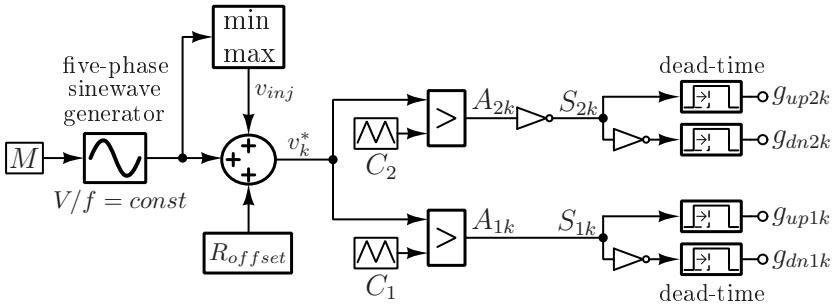


Fig. 3.7. Coupled CB PWM algorithm for the three-level operation with 2L-OeW-2L drive (r = 1).

The relation between A_{ik} and S_{jk} can be expressed as:

$$\begin{aligned} S_{1k} &= A_{1k} \\ S_{2k} &= \overline{A}_{2k} \end{aligned} \tag{3.10}$$

As a direct consequence of equal dc-link voltages, in this case two VSIs never operate at the same time in PWM mode. This is an important conclusion, based on the fact that the reference cannot belong to two reference zones at the same time, while (3.10) separates two inverter's operation. Detailed analysis of this case can be found in [Bodo (2013), Bodo et al. (2013b)]. VSI_1 and VSI_2 operation is summarised in Table 3.3, where term "PWM" is used to indicate that inverter is modulated, according to reference comparison with a carrier signal. Otherwise the VSI holds its leg output at the same voltage level during one half of the fundamental period and operates in PWM mode for the rest of the time.

Table 3.3. Operation of two VSIs vs. reference zone for r = 1.

Reference zone (i)	Range in Figs. 3.5 and 3.6.	VSI_1 operation	VSI_2 operation
1	0 to 1/2	PWM	holds 0
2	1/2 to 1	holds 0	PWM

3.3.3. CB PWM FOR THE UNEQUAL DC-LINK VOLTAGES CASE

Development of the modulation strategy for 2L-OeW-2L with unequal dc-link voltages is somewhat more complex. Namely, it is clear that four voltage levels cannot be directly produced, using two two-level inverters separately. Carrier arrangements and equivalent model analysis shows that two inner voltage levels are formed as a voltage difference between VSI_1 and VSI_2 upper and lower dc-link rails. This means that any transition between these two voltage levels has to be performed by simultaneous PWM switching of the inverters (in corresponding legs attached to the same phase). Switching in two other (outer) reference zones is performed using only one inverter, as summarised in Table 3.4.

Table 3.4. Operation of two VSIs vs. reference zone for r > 1.

Reference zone (i)	Range in Figs. 3.5 and 3.6.	VSI_1 operation	VSI_2 operation
1	0 to $r/(r+1)$	holds 0	PWM
2	$r/(r+1)$ to $r/(r+1)$	PWM	PWM
3	$r/(r+1)$ to 1	holds V_{dc1}	PWM

Clearly, as in any carrier based modulation strategy, reference comparison with carrier signals provides information about the switching states that should be triggered. In this case however, there are three carrier signals, while both VSI_1 and VSI_2 contain only one complementary IGBT+D pair per drive phase. Hence, the question is how to use the obtained A_{ik} in order to calculate S_{jk}. One approach is to consider the system as a combinational network, with A_{ik} as

inputs and S_{jk} as outputs. All possible combinations are summarised in Table 3.5. Cases which are not possible are eliminated from the analysis (denoted with "X" – don't care state). Those combinations of A_{ik} signals never occur, since phase voltage reference cannot be smaller than C_{i-1} and higher then C_i at the same time. For the remaining combinations, the desired equivalent phase voltage level is determined based on Figs. 3.5 and 3.6. Further calculations of desired leg voltages and required switching states are obtained using the data in Table 3.2 and equivalent model analysis. The final step is to determine the mathematical expression that connects A_{ik} and switching states S_{jk}. Following the rules from Boolean algebra, where truth tables are commonly used, Table 3.5 is transformed into two separate truth tables (Karnaugh's maps), each for one switching state (Tables 3.6 and 3.7). The simplest method for obtaining a mathematical expression from the truth table is to use Karnaugh map analysis. Using the well-known rules for derivation of a truth function (sums of products or product of sums), one is able to obtain the following expressions:

$$\begin{aligned} S_{1k} &= A_{2k} \\ S_{2k} &= \overline{A}_{1k} + A_{2k} \cdot \overline{A}_{3k} \end{aligned} \tag{3.11}$$

Table 3.5. CB PWM for 2L-OeW-2L four-level operation in state machine form.

Inputs			Resulting voltages			Resulting switching states	
A_{1k}	A_{2k}	A_{3k}	v_k	v_{1k}	v_{2k}	S_{1k}	S_{2k}
0	0	0	$-V_{dc2}$	0	V_{dc2}	0	1
0	0	1	X	X	X	X	X
0	1	0	X	X	X	X	X
0	1	1	X	X	X	X	X
1	0	0	0	0	0	0	0
1	0	1	X	X	X	X	X
1	1	0	$V_{dc1} - V_{dc2}$	V_{dc1}	V_{dc2}	1	1
1	1	1	V_{dc1}	V_{dc1}	0	1	0

Table 3.6. Karnaugh map for S_{1k}.

A_{1k} \ A_{2k} A_{3k}	0 0	0 1	1 1	1 0
0	0	X	X	X
1	0	X	1	1

Table 3.7. Karnaugh map for S_{2k}.

A_{1k} \ A_{2k} A_{3k}	0 0	0 1	1 1	1 0
0	1	X	X	X
1	0	X	0	1

As expected, the obtained expressions are in agreement with Table 3.4, which is not used for (3.11) derivation. The final modulation diagram is shown in Fig. 3.8. Alternatively, one is able to use only one inverter in the case of $M < M_{max}/2$ for $r = 1$ and for $M < M_{max} \cdot (r-1)/(r+1)$ with $r > 1$. The algorithm is presented in Fig. 3.9. In these cases, VSI_1 effectively forms a star connection on its side of the windings, while VSI_2 works in PWM mode. This modification of modulation strategy for low modulation index range is not necessary for the three-level operation, since two inverters never operate at the same time as demonstrated further in subsection 3.3.7. This effectively reduces switching losses, by reducing the overall number of switching actions per one switching period when the drive operates in two-level mode. Therefore, this kind of modulation is called switching action reduction (SAR) algorithm. It should be combined with strategies in Figs. 3.7 and 3.8, which comes down to a simple *if-then-else* statement based on the instantaneous value of M.

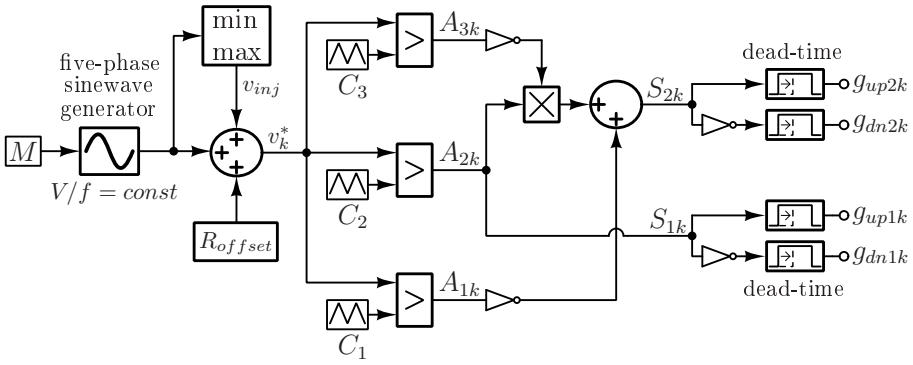


Fig. 3.8. Coupled CB PWM algorithm for the four-level operation with 2L-OeW-2L drive ($r > 1$).

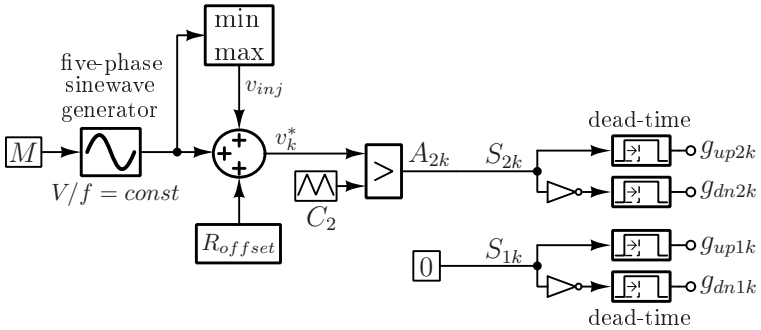


Fig. 3.9. Switching action reduction (SAR) algorithm for 2L-OeW-2L drive.

3.3.4. SIMULATION RESULTS

The coupled carrier based modulation approach was firstly analysed and verified in [Darijevic et al. (2013a)], using $r = 2$, for both PD and APOD PWM, including the SAR algorithm. The simulation results were obtained using the parameters and setup from Appendix 1, but without dead-time. It was later discovered that coupled CB PWM methods for unequal dc-link voltages are accompanied with one drawback, which is a direct consequence of the drive topology and the inevitable inverter dead-time [Darijevic et al. (2013b), Darijevic et al. (2015a), Darijevic et al. (2016)]. Simulation results, including inverter dead-time of 6 µs, for three values of r when $M = 1$ are shown in Figs. 3.10 and 3.11 for PD and APOD PWM, respectively. To aid clarity, here, as well as in the rest of the thesis, waveforms are shown for one fundamental period, when machine is under no load. Waveforms are starting at the maximum of the phase voltage waveform which corresponds with a cosine phase voltage reference.

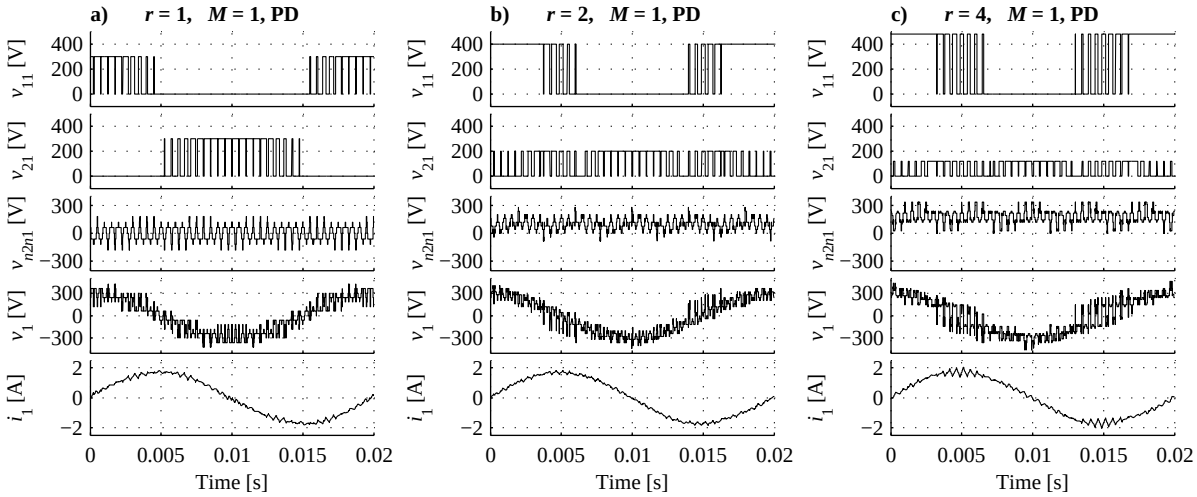


Fig. 3.10. Simulation results: conventional PD PWM for $M = 1$ and $r = 1$ (a), $r = 2$ (b), $r = 4$ (c).

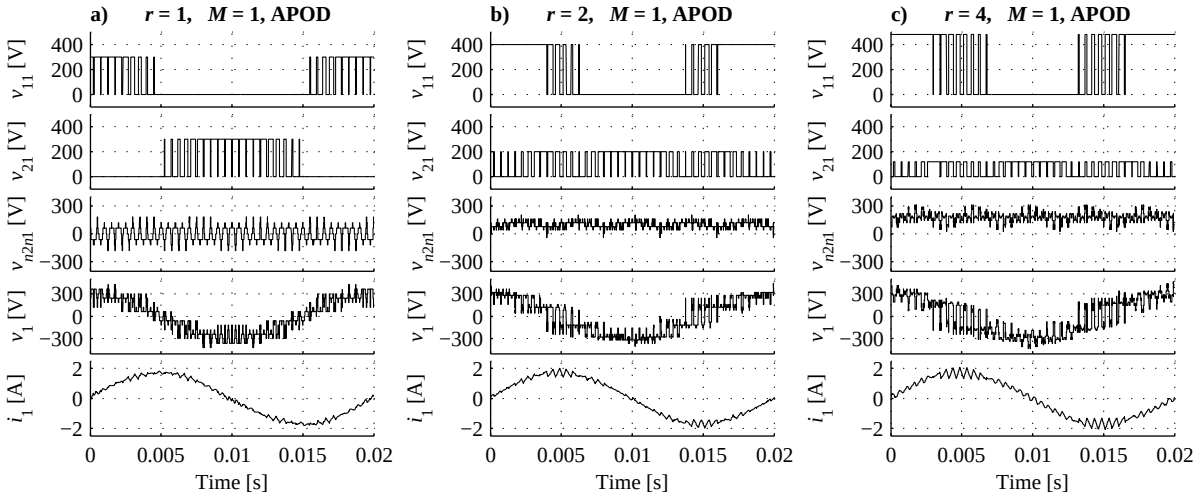


Fig. 3.11. Simulation results: conventional APOD PWM for $M = 1$ and $r = 1$ (a), $r = 2$ (b), $r = 4$ (c).

Clearly, the produced phase voltage waveforms are multilevel in nature. However, it is also easy to notice some unexpected transitions in the middle part of the phase voltage waveforms (around zero crossings). This phenomenon is discussed in the next subsection.

3.3.5. DEAD-TIME SPIKES

Table 3.4 shows that VSI_1 and VSI_2 operate in the PWM mode in the reference zone 2 for $r > 1$. This characteristic of the proposed modulation method leads to the existence of an additional voltage level, when compared with the equal dc-link voltage case (Table 3.3). Clearly the transition between two inner voltage levels is only possible with simultaneous switching action on both sides of the windings. This is incorporated in CB PWM algorithm in Fig. 3.8 and equation (3.11), since the same value of A_{2k} is used for calculating both S_{1k} and S_{2k}. Since conventional PWM strategies do not take dead-time into account, this means that simultaneous switching will take place, with dead-time intervals in two VSIs taking place at the same time, in the same drive phase [Darijevic et al. (2013b)]. There are two switching actions per one switching period and so two so-called dead-time spikes will occur in each switching period (per drive phase). This phenomenon occurs only when the phase voltage reference is in the zone 2 (Figs. 3.5 and 3.6) and leads to the voltage spikes visible in Figs. 3.10 and 3.11. As known from the inverter operation theory, VSIs output (leg) voltages are determined by the load current which flows through antiparallel diodes during dead-time intervals. As a result, there are two possible outcomes:

- Case 1: The phase voltage during the dead time interval takes a value equal to one of the two voltage levels between which the transition is to be done.
- Case 2: The phase voltage during the dead time interval takes a value which is different from both initial and final voltage levels between which the transition is to be done.

As far as single-sided supplied drives are concerned, only case 1 is possible. For example, in a four-level neutral point clamped (NPC) inverter [Perantzakis et al. (2007)], only one complementary switch pair in the leg will change state during transition between adjacent leg voltage levels. On the other hand, in the OeW drive, the phase voltage is formed as the difference of the corresponding leg voltages of the two inverters. Case 1 will occur when transition from one phase voltage level to the adjacent voltage level is to be accomplished by switching one inverter only, while the leg voltage of the second inverter in that phase remains unchanged. When leg voltages in both inverters must be changed in order to

make phase voltage transition between adjacent levels, case 2 will take place. Obviously, investigation of this phenomenon cannot be based on the analysis of IGBT+D switching states since the actions of all semiconductor devices must be taken into account. Two examples of the drive behaviour in reference zone 2 are depicted in Fig. 3.12, for positive and negative phase current. These results are obtained by simulation for PD PWM and $r = 2$ [Darijevic et al. (2013b)].

Analysis from [Darijevic et al. (2013b)] is generalised in this subsection and can be applied for any dc-link voltage ratio, for both PD and APOD PWM. The software solution for this problem, originally proposed in [Darijevic et al. (2013b)], is extended here as well, for an arbitrary value of r.

In Fig. 3.12, semiconductor states are shown for the first drive phase ($k = 1$), during the n^{th} switching period ($T_S = 500$ µs), for the phase voltage reference in zone 2. For the purpose of demonstration, dead-time is set to $t_{d\text{-}t} = 15$ µs. Semiconductor states are marked with 1 when the corresponding power transistor or diode conducts; otherwise they are equal to 0. The reference signal is sampled at the beginning of each switching period.

Let us first determine the antiparallel diode states during this switching period. In the case of negative phase current (Fig. 3.12a), diodes D_{up11} and D_{dn21} will conduct in periods when phase current cannot flow through the switches, while diodes D_{dn11} and D_{up21} will be turned off. In the time instant $t = (n-1)\cdot T_S$, S_{up11} and S_{up21} should be turned on, which will result in an equivalent phase voltage of $(r-1)/(r+1)\cdot V_{dc}$. However, since current i_1 has the negative sign, S_{up11} will not conduct. Instead, antiparallel diode D_{up11} will be turned on. Complementary transistors, S_{dn11} and S_{dn21} are in off state.

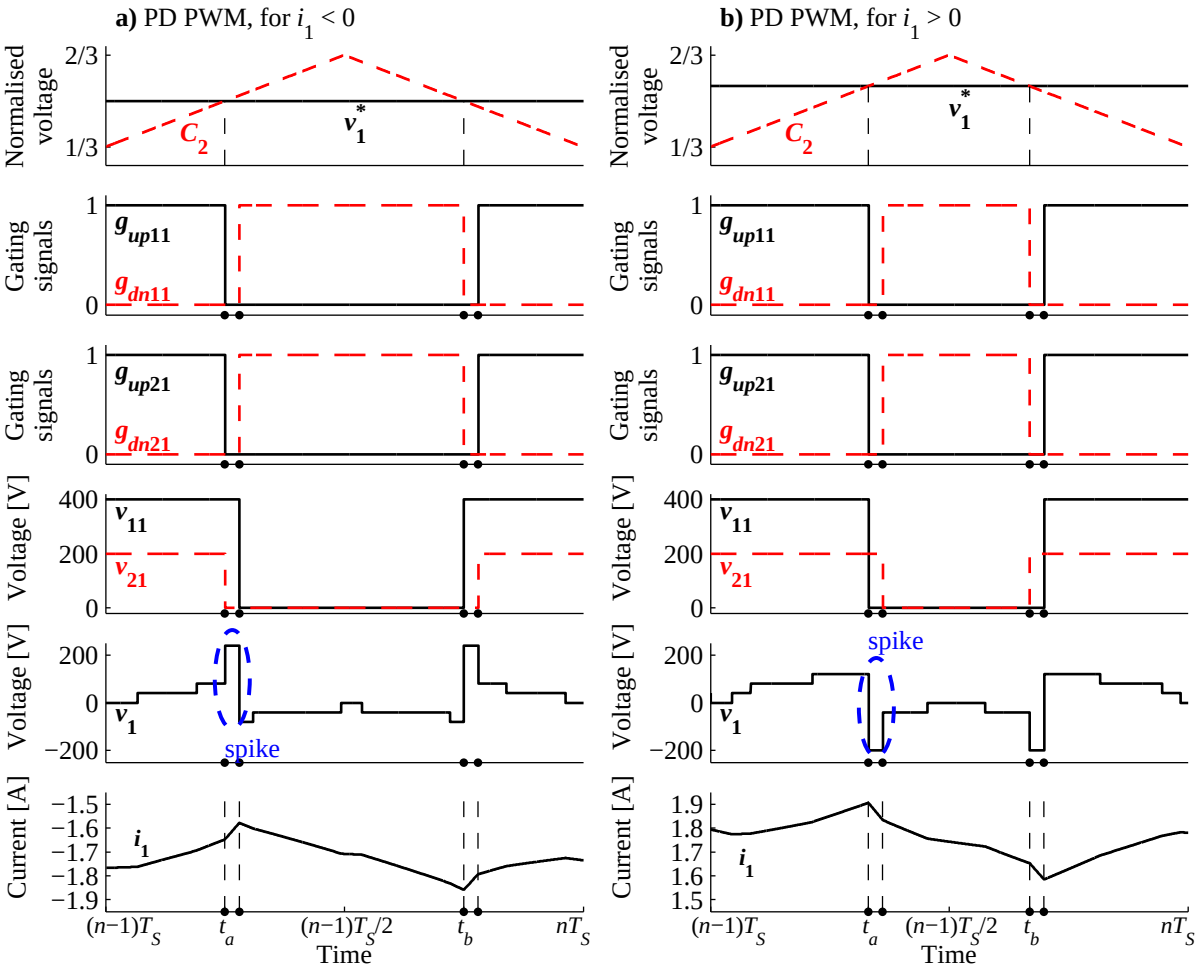


Fig. 3.12. Simulation waveforms for one T_S showing dead-time spike formation in the case of PD PWM with $r = 2$, $M = 1$: for negative (a) and positive (b) phase current. The first appearing spike are denoted with blue lines.

This continues until $t = t_a$, when the first transition occurs (reference intersects with the carrier's rising edge). The equivalent voltage should change from $1/(r + 1)\cdot V_{dc}$ to 0 at t_a, however the dead-time interval will start in both inverter legs. The end of the dead-time interval takes place at $t_a + t_{d\text{-}t}$. Clearly, phase voltage during interval $t_{d\text{-}t}$ will not be determined by the switches in this phase, but with phase current sign, which means that diodes D_{up11} and D_{dn21} will conduct and the equivalent voltage level will be $r/(r + 1)\cdot V_{dc}$. The consequence of this transition is a spike in phase voltage, as shown in Fig. 3.12a. Other transitions in the phase voltage are consequence of CMV influence, equation (3.1).

Similarly, at the time instant determined with the second reference intersection with carrier signal ($t = t_b$), another dead-time spike will occur, with the same direction and amplitude. It is clear that phase current has different slope (di/dt) for $t_a < t < (t_a + t_{d\text{-}t})$ and $t_b < t < (t_b + t_{d\text{-}t})$, which amplifies the detrimental dead-time influence on the phase current low-order harmonics. The same analysis can be applied on the positive phase current case, shown in Fig. 3.12b. The only difference is that spikes are in this case in the other direction, due to conduction of different antiparallel diodes.

In general, as long as the switching actions of both VSIs are determined with the same intersection of the phase voltage reference and carrier C_2, unwanted voltage levels will be triggered during dead time intervals. Recurrence, duration and shape of so-called dead-time spikes are determined not only by dead-time duration, but also with r, M, and dynamic characteristics of IGBT+D structures and snubber circuits. This issue has a greater significance for high-power applications, where dead-time intervals are usually long, due to slower dynamic performance of semiconductor devices aimed for high currents and voltages. The consequences of dead-time spikes are increased harmonic pollution of both phase voltages and currents and increased acoustic noise. Finally, the additional voltage transitions will bring additional switching losses and unnecessary ripple in common mode voltage, which is essential to be kept low, due to bearing currents and other parasitic effects that have detrimental impact on the drives' performance. In other words, this phenomenon clearly diminishes the expected performance in the case of the four-level OeW drive.

It is easy to conclude from the previous analysis that dead-time spikes are naturally eliminated for $M < M_{max}\cdot(r - 1)/(r + 1)$, since only two-level operation takes place, which can be utilised using only the VSI with the lower dc-link voltage. If both inverters are employed in this mode, dead-time spikes will appear at every switching instant during one fundamental period. In the four-level mode, appearance of dead-time spikes is inversely proportional to M, since the reference is less present in the zone 2 for higher values of M (during one fundamental period).

The per-unit amplitude of the dead-time spikes is always equal to $r/(r + 1)$, which is the height of reference zones 1 and 3. This conclusion comes from the analysis of the triggered voltage levels: instead of switching directly between two inner levels, simultaneous gating signals trigger one of the other two levels during dead time. Which unwanted level is going to be triggered depends on the phase current sign, i.e. conduction of antiparallel diodes. Together with the previous analysis of the influence of M on dead-time spikes occurrence, this leads to another important conclusion: dead-time spike amplitude is inversely proportional to r, but their occurrence during one fundamental period in four-level operation mode is directly proportional to r.

The previous analysis shows that there is no ideal value of $r > 1$, which will lead to elimination of this issue. Hence, the problem has to be solved by modification of the modulation strategy. In what follows, the proposed solution in [Darijevic et al. (2013b)] is extended for an arbitrary dc-link voltage ratio. Essentially, this issue stems from the fact that CB PWM methods use the same phase voltage reference for A_{ik} calculation (3.9), which are later used in (3.11) to obtain S_{1k} and S_{2k}. Looking at Fig. 3.12, it is clear that the problem comes from the fact that final gating signals are synchronised, instead of leg voltage transitions (v_{1k} and v_{2k}). One solution to this problem is to shift the switching instants of one VSI by the dead-time interval, in order to synchronise transitions of v_{1k} and v_{2k}. This can be achieved by addition

or subtraction of a small reference offset (Δv), in order to shift in time the reference intersection with carrier signal for one dead-time duration. This should be done for only one VSI. Hence, two references are needed and their comparison with C_2 should give two different values of A_{2k}, which should be later used in (3.11). Fig. 3.13 shows one example of phase voltage reference and carrier C_2 intersection that can be used in order to determine Δv. Analysis of similar triangles in Fig. 3.13 reveals the proportion:

$$\Delta v : t_{d-t} = \left(\frac{r}{r+1} - \frac{1}{r+1} \right) : \frac{T_S}{2} \tag{3.12}$$

Using $T_S = 1/f_S$, above expression can be written as:

$$\Delta v = 2 \cdot f_S \cdot t_{d-t} \cdot \frac{r-1}{r+1} \tag{3.13}$$

The complete so-called spike removal algorithm (SRA) is depicted in Fig. 3.14. This algorithm has to be incorporated within CB PWM shown in Fig. 3.8, using Δv_{1k} and Δv_{2k} from Fig. 3.14, as shown in Fig. 3.15. Simulation results that demonstrate the effectiveness of the proposed method are shown in Figs. 3.16 and 3.17. Although this is probably the simplest compensation method for dead-time spikes, it requires a different switching algorithm in the first and the second half of the switching period T_S:

- For $n \cdot T_S < t \leq (n + 0.5) \cdot T_S$ and $i_k > 0$, the reference will be increased by Δv in the case of VSI_1, while switching of the VSI_2 should be governed with the original reference value.
- For $(n + 0.5) \cdot T_S < t \leq (n + 1) \cdot T_S$ and $i_k > 0$, reference for VSI_1 should remain unchanged, while switching of the VSI_2 should be determined with the reference value reduced by Δv.
- For $n \cdot T_S < t \leq (n + 0.5) \cdot T_S$ and $i_k \leq 0$, only reference for VSI_1 should be reduced by Δv.
- For $(n + 0.5) \cdot T_S < t \leq (n + 1) \cdot T_S$ and $i_k \leq 0$, only reference for VSI_2 should be increased by Δv.

As a result of SRA implementation, dead-time intervals will never coincide in the legs of two VSIs that are associated to the same phase, as shown in Fig. 3.18, for the same switching period as in Fig. 3.12, but for PD with SRA. Looking from the load perspective, this modification doubles the effective duration of dead-time, in comparison to the original PD PWM, but only in zone 2, as is visible from comparison of Figs. 3.12 and 3.18. This means that the diodes will conduct for twice longer period and will either hold the existing voltage level or switch to the next level, as in the case 1.

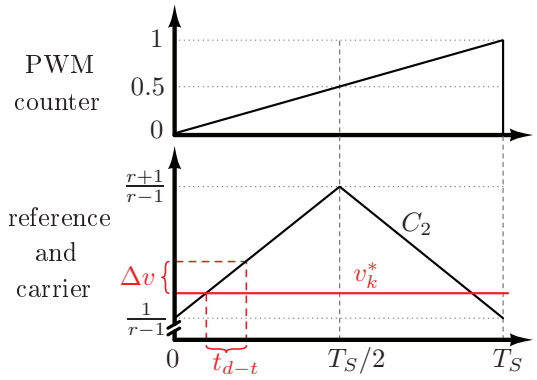


Fig. 3.13. Determination of Δv for SRA implementation, based on phase voltage reference and carrier intersection in zone 2. The reference is sampled at the beginning of switching period, denoted for simplicity with $t = 0$. The dead time interval length has been exaggerated for clearer geometrical representation.

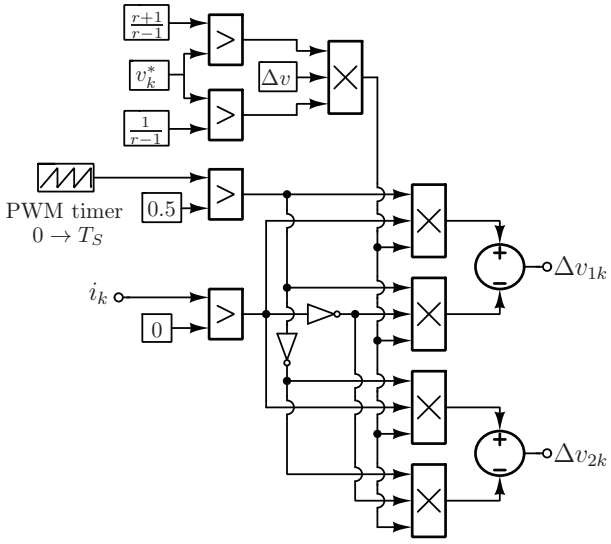


Fig. 3.14. SRA algorithm for 2L-OeW-2L drive.

As reported in [Darijevic et al. (2013b)] SRA leads in some cases to a small increase in phase current THD for certain modulation index values, due to the more dominant effect of dead-time duration in reference zone 2 (the effective dead-time is increased due to the SRA). Hence, PD PWM with SRA results in somewhat larger low-order current harmonic amplitudes for modulation indices around $M = 0.5$. This does not represent a huge drawback, since modern drives are usually controlled in a closed-loop manner, where current controllers are used to supress undesired harmonics, as discussed in Chapter 7.

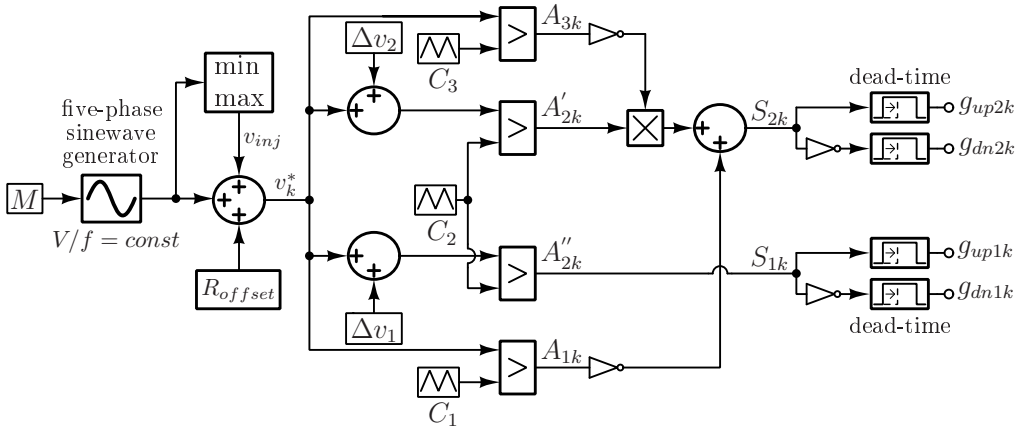


Fig. 3.15. Coupled CB PWM with SRA for the four-level operation for 2L-OeW-2L drive.

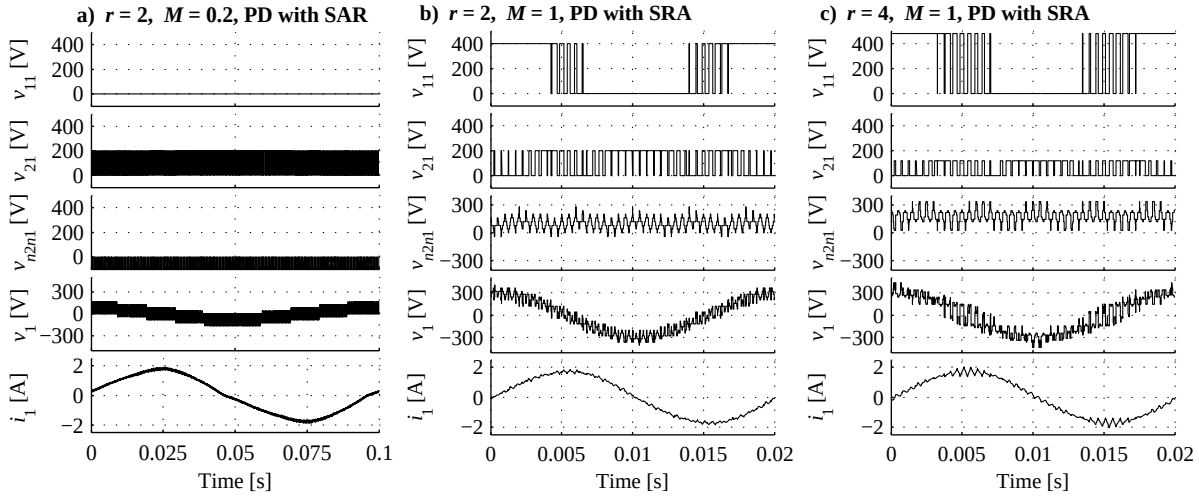


Fig. 3.16. Simulation results: PD PWM with SAR/SRA for $M = 0.2$, $r = 2$ (a), $M = 1$, $r = 2$ (b), $M = 1$, $r = 4$ (c).

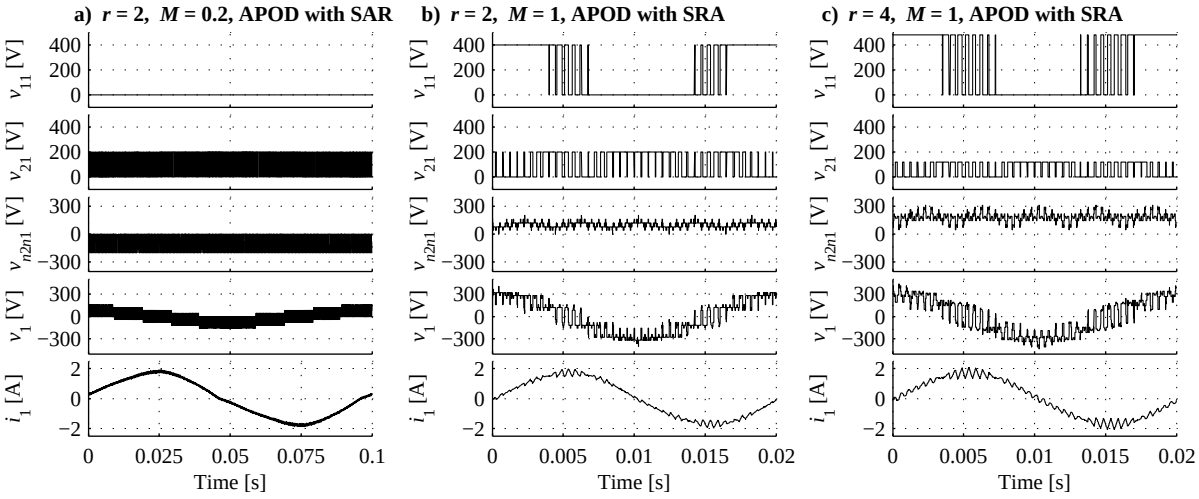


Fig. 3.17. Simulation results: APOD PWM with SAR/SRA for $M = 0.2$ (a), $M = 1$, $r = 2$ (b), $M = 1$, $r = 4$ (c).

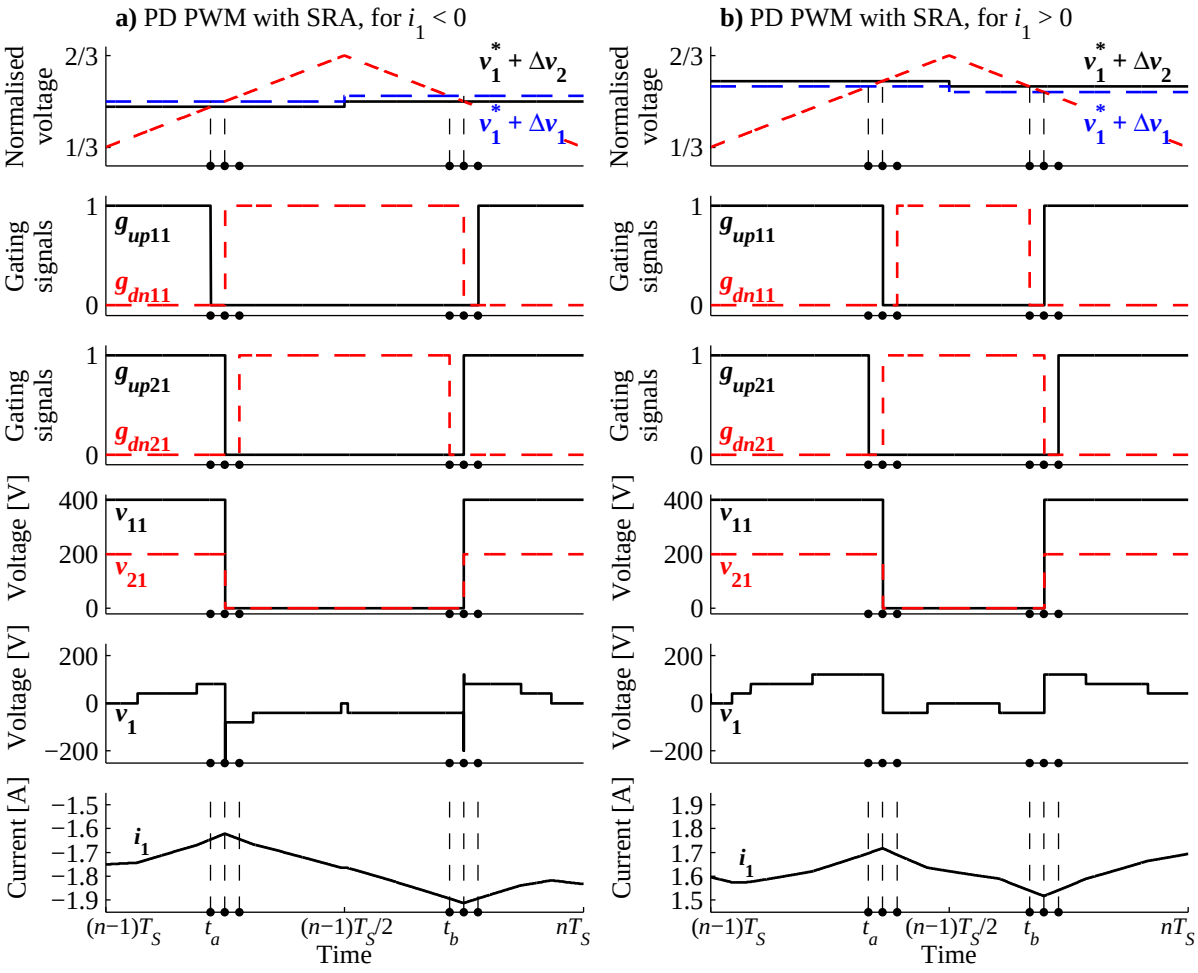


Fig. 3.18. Simulation waveforms for one T_S showing SRA effects on gating signals and dead-time spike elimination in the case of PD PWM with $r = 2$, $M = 1$ with SRA: for negative (a) and positive (b) phase current.

Experimental verification shown in Fig. 3.19 reveals some other issues. Details about experimental verification and laboratory setup can be found in Appendix 2. In this case, open-loop control and *V*/*f* = *const*. rule is applied, while machine is under no load. Due to imperfect match of rise/fall slopes on two OeW sides, since IGBTs and antiparallel diodes have different dynamic responses, it is practically impossible to perfectly match and synchronise leg voltage transitions. Nevertheless, influence of this short spike in Fig. 3.19b on the phase current slope is much shorter and with a lower amplitude than in the case of Fig. 3.19a. Furthermore, it is clear that for some values of *M*, *r* and phase angles between phase voltage and phase current, phase current sign is of interest when current is close to zero, which makes SRA implementation less certain, due to the limitations of current sensors. This can be partly overcome by using SAR for two-level operation, but in the case of four-level operation only hardware improvement (current measurement precision) can eliminate this issue.

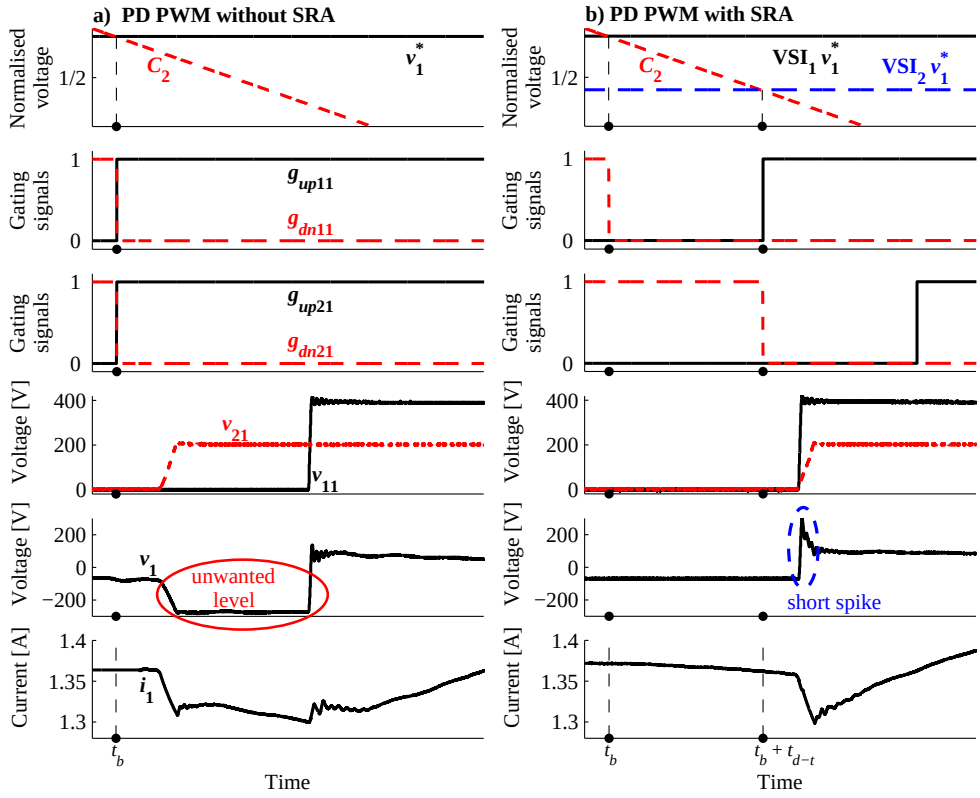


Fig. 3.19. Experimental verification for dead-time spikes. Zoom at one simultaneous switching in reference zone 2 in the case of $r = 2$, $M = 1$ with PD PWM (a) and PD PWM with SRA (b).

3.3.6. INFLUENCE OF THE DC-LINK VOLTAGE RATIO ON DRIVE HARMONIC PERFORMANCE

The previous analysis provided several important conclusions regarding the dc-link voltage ratio influence on the performance of the drive. However, it is very hard to determine the optimal value of r from the simple analysis of waveform shapes in time domain or the space vector distribution. From that point of view, it seems natural to analyse drive harmonic performance, i.e. stator voltage and stator current harmonic content, for different dc-link voltage ratios. Having in mind that two different modulation strategies are under consideration, while both M and r parameters should be varied over a wide range of values, it is clear that detailed numerical simulation is the only way to provide a complete picture. Harmonic performance against r is evaluated using the simulation set-up and parameters from Appendix 1. The drive is controlled in the open-loop manner, using $V/f = const.$ rule as in (3.8), while R_{offset} is 0.5. For both PD and APOD PWM, the complete range of M is covered, starting from 0.1 to 1.05, with 0.05 steps. This is done for different values of dc-link voltage ratio values, in the range from 1 to 4, with 0.1 steps. Recordings of steady state phase voltages and phase currents are then used for total harmonic distortion (THD) calculation, based on the following equation:

$$THD = \sqrt{\sum_{i=2}^{K} \frac{X_i^2}{X_1^2}} \tag{3.14}$$

where X_i is the rms value of the i^{th} harmonic, the fundamental is denoted with X_1 and K is set to 5000. The same set of simulation results is obtained for modified CB PWM, which uses SAR and SRA. THD dependences on M, for several different values of r are depicted in Fig. 3.20.

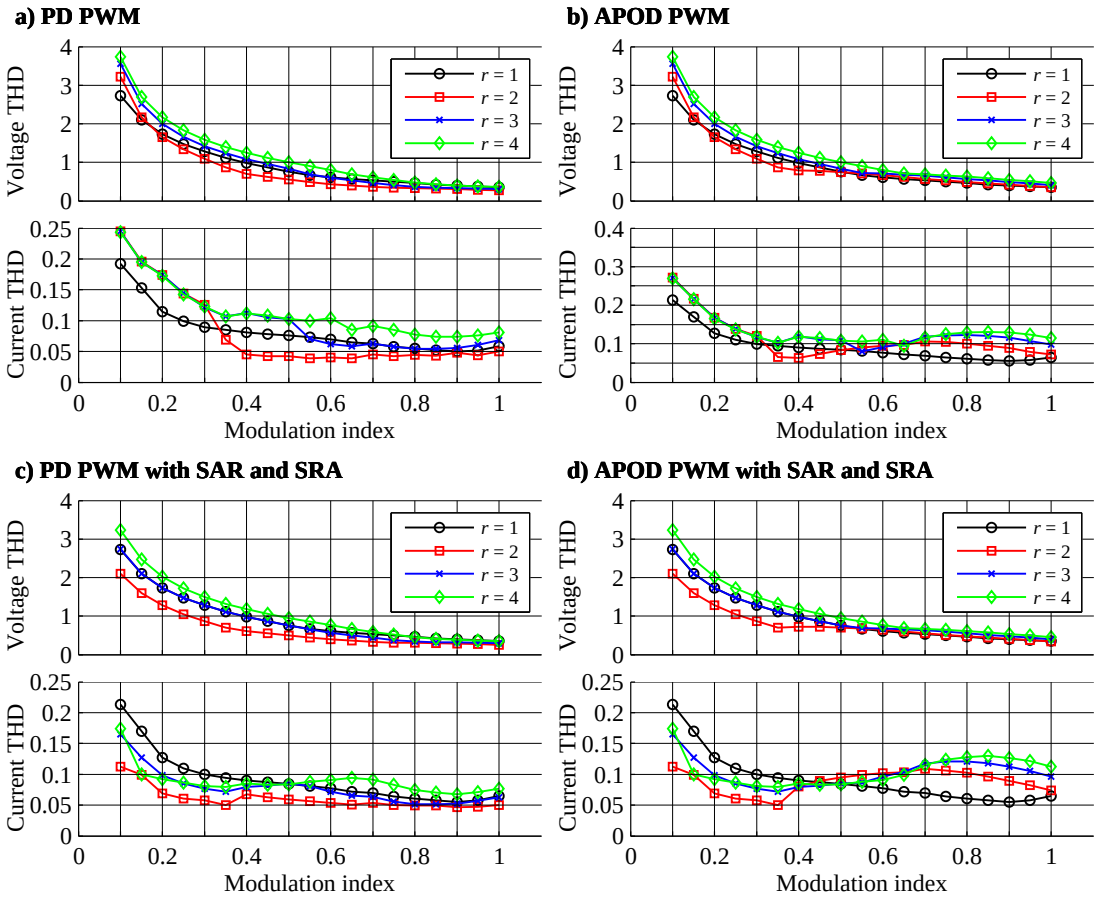


Fig. 3.20. Simulation results: phase voltage and phase current THD(*M*) for conventional PD and APOD (a, b) and with SAR and SRA (c, d), with different dc-link voltage ratios.

Although all phase voltage THD(*M*) have the same trend, the influence of dead-time on low-order harmonics in phase current spectra is different. For example, the three-level case with conventional APOD has the best current harmonic performance (Fig. 3.20b) only because there are no dead-time spikes for $r = 1$. This is also the case with conventional PD PWM, for low modulation index range. As expected, large value of r leads to an overall increment of harmonic distortion in the phase voltage, especially for low modulation index values, where the drive operates in two-level mode. Clearly, PD has superior harmonic performance. However, simulation results in Figs. 3.16 and 3.17 show that APOD has lower common mode voltage ac components, which might be of interest for high-voltage applications, where bearing currents and similar isolation issues are of the particular importance.

Furthermore, while an arbitrary dc-link voltage ratio can be obtained using dc-dc converters, a simpler approach, suitable for traction applications and electric vehicles is to use battery packs (with an integrated voltage regulation). This limits the number of possible dc-link voltage ratios and probably the two simplest to produce are V_{dc1}:V_{dc2} = 1:1 and 2:1 (i.e. r = 1 and 2).

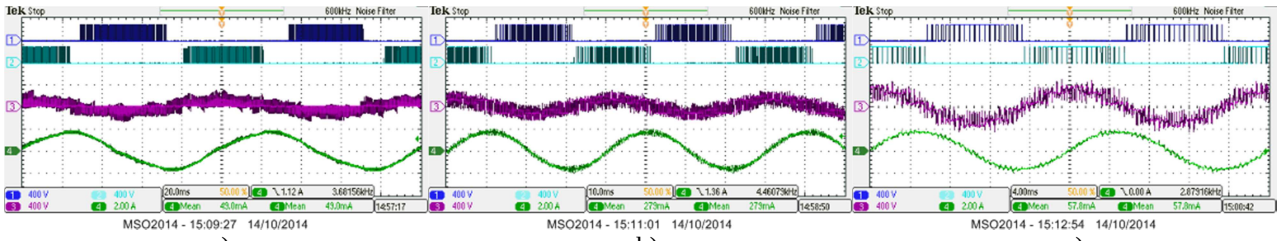
3.3.7. EXPERIMENTAL RESULTS FOR THE THREE-LEVEL CONFIGURATION

The three-level drive configuration (with $r = 1$) is experimentally evaluated here using the modulation algorithm developed in Section 3.3.2. For the sake of easier comparison with results in [Bodo et al. (2013)], the same drive parameters are used, i.e. $V_{dc1} = V_{dc2} = 300$ V, switching frequency of two inverters is set to $f_S = 2$ kHz, while both inverters have hardware implemented dead-time, of 6 µs. More details about the experimental set-up can be found in

Appendix 2. Obtained waveforms, for $M = 0.2$, 0.5 and 1 are shown in Figs. 3.21 for PD PWM and 3.22 for APOD PWM. The oscilloscope screen shot shows, from top to bottom, the VSI_2 leg voltage v_{21} (CH1), VSI_1 leg voltage v_{11} (CH2), machine phase voltage v_1 (CH3) and the stator current i_1 (CH4). Obtained waveforms are identical with those presented in [Bodo et al. (2013)]. Looking at the leg voltages it can be seen that the two inverters never switch at the same time, while the phase-voltage is indeed identical to the one produced using a three-level single-sided supply [Bodo et al. (2012)].

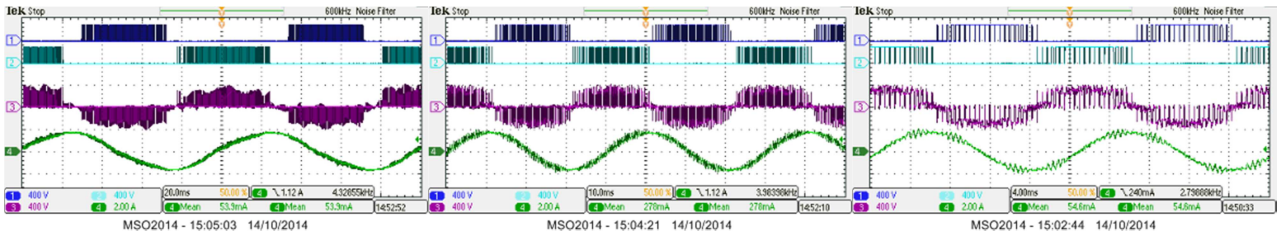
As already stated, the open-end winding structure offers a possibility to use only one of the two inverters under certain operating conditions. In the case of $r = 1$, this operation mode is possible for $M < M_{max}/2$. This way the topology is effectively transformed from a three-level inverter with $V_{dc} = 600$ V to a two-level inverter with $V_{dc} = 300$ V. In this case, only one carrier from Fig. 3.5a and 3.6a should be used. This can be achieved by changing the R_{offset} value from 1/2 to 1/4 so that the reference will be completely placed in reference zone 1, intersecting with only one carrier signal. Using the same set of equations for S_{1k} and S_{2k}, VSI_1 will operate in PWM mode, while VSI_2 will form a star connection on its side of the windings. The perceived advantage of this operating regime is that the switching losses are halved (since only one inverter is switching) and the switching harmonics are reduced since the phase voltage is obtained using dc-link voltage of 300 V rather than 600 V. This mode of operation is not further investigated here; instead, the method explained in subsection 3.3.2 is favoured, for reasons that will be given later.

The waveforms in Figs. 3.21 and 3.22 show that VSI_1 and VSI_2 never work in PWM mode at the same time, so the modification mentioned above does not seem to be so beneficial. On the contrary, it reduces the overall number of voltage levels, leading to a lower harmonic performance. Furthermore, the total number of switching events is the same and, by extension, so are the switching losses. Phase voltage and phase current spectra are shown in Figs. 3.23 and 3.24, covering the first two sidebands centred around the switching frequency ($f_S = 2$kHz); in the top right corner rms values of the first ten low-order harmonics are shown. Corresponding THD(M) dependencies are shown in Fig. 3.25. THD is calculated using (3.14), for modulation index ranging from 0.1 to 1.05 in 0.05 increments.



a) b) c)

Fig. 3.21. Experimental results: waveforms with PD PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c). Traces from top to bottom: CH1 shows v_{21} (400 V/div), CH2 v_{11} (400 V/div), CH3 v_1 (400 V/div) and CH4 i_1 (2 A/div). This arrangement of oscilloscope screenshot is used in the rest of the thesis, unless specified differently.



a) b) c)

Fig. 3.22. Experimental results: waveforms with APOD PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

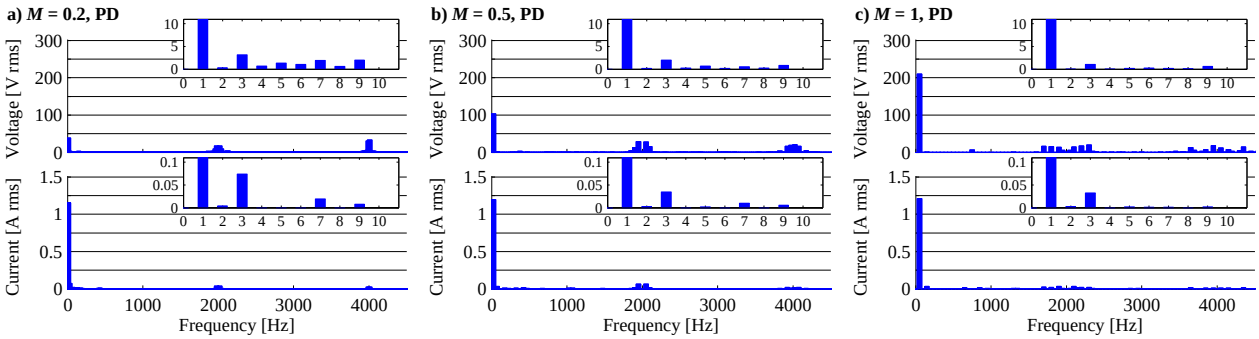


Fig. 3.23. Experimental results: v_1 and i_1 spectra for PD PWM and r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c). Subfigure in the top right corner shows rms values of the first 10 low-order harmonics.

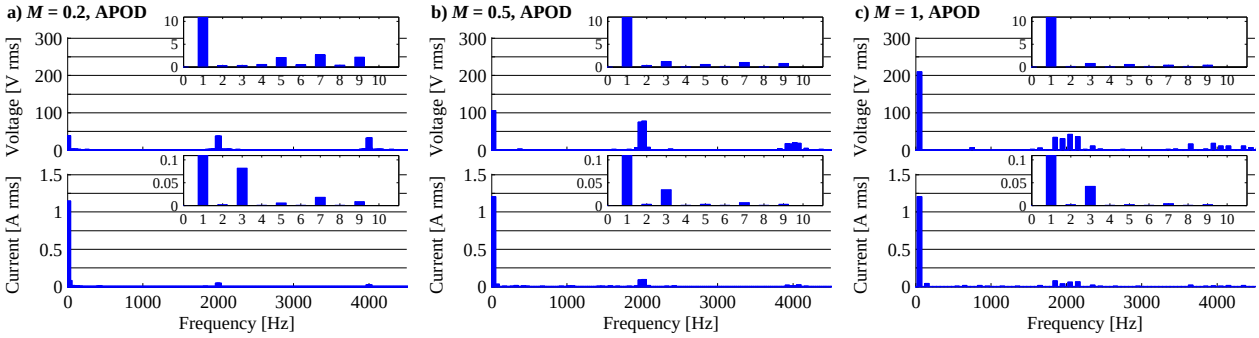


Fig. 3.24. Experimental results: v_1 and i_1 spectra for APOD PWM and r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

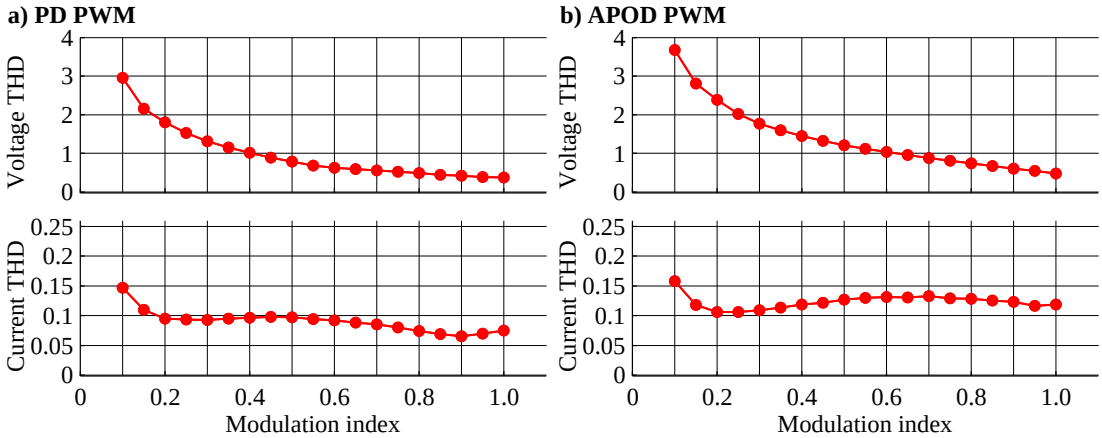


Fig. 3.25. Experimental results: THD(M) for r = 1, with PD (a) and APOD (b).

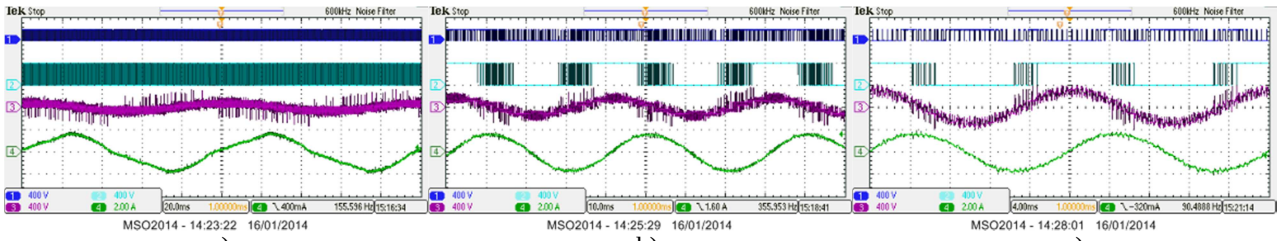
Comparison with the waveforms from [Bodo et al. (2013)] confirms that the proposed modulation scheme with equation (3.10) and Fig. 3.7 results in the same phase voltage and current waveforms. Clearly, PD results in lower harmonic distortion. Due to the limited number of oscilloscope channels, v_{n2n1} is not shown in Figs. 3.21 and 3.22. Analysis of simulation results (Fig. 3.10a, 3.11a) shows that v_{n2n1} dc component is the same regardless of the modulation strategy, while ac components are lower in the case of APOD, which may well be of interest for high-power applications, where v_{n2n1} has a strong influence on bearing currents and other isolation related unwanted phenomena. Calculated according to [Karugaba et al. (2012)], the number of CMV levels is approximately 50% smaller in the case of APOD for r = 1 and 20% smaller in the case of r = 2. CMV dv/dt is the same with both PD and APOD for the same value of r, since this parameter is mainly dependent on the size of the equivalent voltage level steps.

3.3.8. EXPERIMENTAL RESULTS FOR THE FOUR-LEVEL CONFIGURATION

For examination of four-level operation $r = 2$ is chosen. This value leads to two-level operation in the low modulation index range ($0 < M \leq 0.35$), since the reference is completely in the second reference zone (Table 3.4, Figs. 3.5c and 3.6c). For $M > 0.35$, full four-level operation, with equidistant voltage levels, takes place. At the same time, setting $R_{offset} = 1/2$ results in CMV dc component V_{n2n1} to be equal to −100 V, which is in the middle between minimal (−400 V) and maximal (200 V) equivalent voltage levels. Experimental results are shown in Figs. 3.26-3.34.

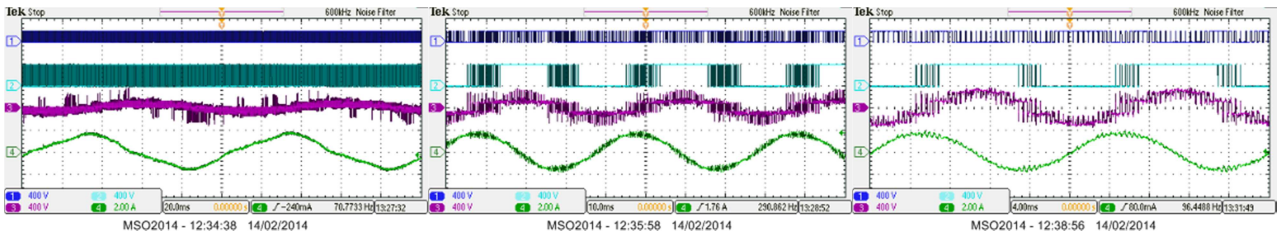
It is important to notice that SAR implementation in this case is very simple, since two-level operation can be utilised by setting $R_{offset} = 1/6$ or 5/6. In these two cases only VSI_1 will operate in PWM mode, while all leg voltages of the VSI_2 will be on the same voltage potential. Averaging the output of (3.2) for this case, one can find that $V_{n2n1} = 100$ V in this operation mode. It should be noted here that for other four-level cases ($r > 1$ and $r \neq 2$), SAR implementation is not possible using the R_{offset} parameter only, since voltage levels are not equidistant. Hence, one is not able to perform two-level operation with VSI_2 only in reference zones 1 or 3 for the same modulation index range as in zone 2. In the case when $r = 2$, R_{offset} can be used to achieve three-level operation as well. This is possible for low ($M \leq 0.35$) and medium modulation index range ($0.35 < M < 0.7$), by setting R_{offset} to either 1/3 or 2/3, which would result in the phase voltage reference passing through two reference zones. However, from Figs. 3.5c, 3.6c and Table 3.4, it can be concluded that VSI_1 and VSI_2 operate in different modes in adjacent zones, meaning that simultaneous switching will be present in only one half of the fundamental period. This asymmetrical operation leads to an increased low-order harmonic content in phase voltage and current spectra. Therefore, in [Darijevic et al. (2013b)] the drive operates as a two-level drive with only one VSI in PWM mode for $M \leq 0.35$, while for the rest of the modulation index range four-level operation is utilised.

Comparison of the waveforms in Figs. 3.26-3.27 and 3.28-3.29 confirms previously shown simulation results and effectiveness of SAR and SRA. It should be noted here that for $M = 0.2$ dead-time spikes are not completely visible in oscilloscope screenshots, due to very low resolution of captured images and reduced sampling over the large interval of time. The dead-time detrimental impact in low modulation index range without SAR is clear from the phase current waveforms. Spectra in Figs. 3.30-3.33 shows that for $M = 0.5$ SRA causes somewhat increased 3rd current harmonic, which clearly affects the overall THD performance, as shown in Fig. 3.34. As already stated, this can be resolved with closed-loop current controllers as demonstrated in Chapter 7.



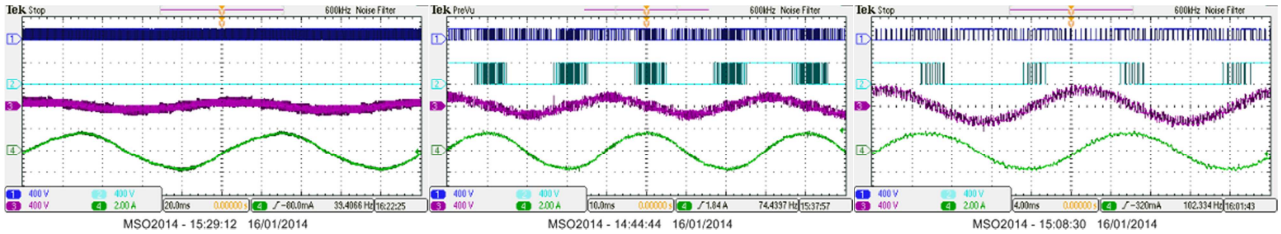
a) b) c)

Fig. 3.26. Experimental results: obtained waveforms with PD PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



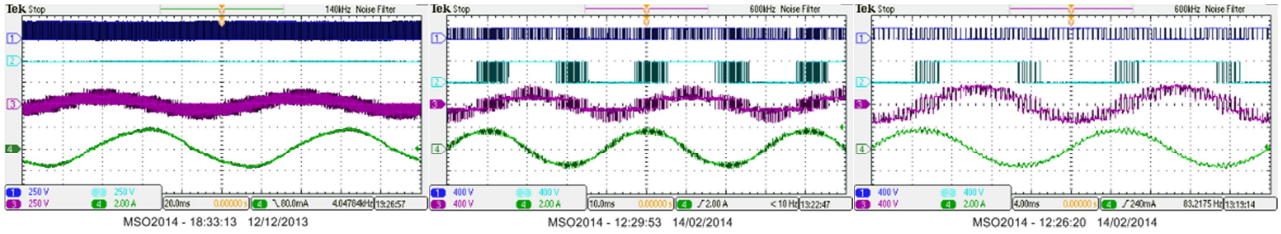
a) b) c)

Fig. 3.27. Experimental results: waveforms with APOD PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 3.28. Experimental results: with PD PWM with SAR/SRA and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 3.29. Experimental results: APOD PWM with SAR/SRA and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

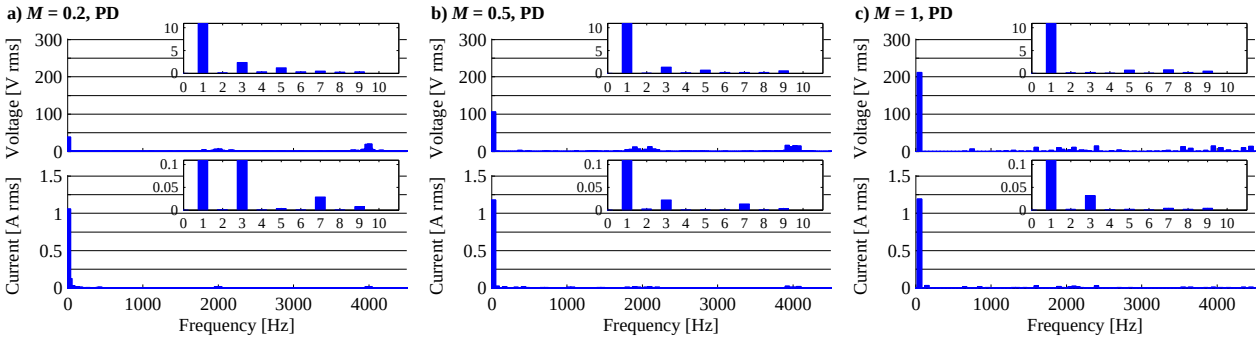


Fig. 3.30. Experimental results: v_1 and i_1 spectra for PD PWM and $r = 2$ for $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

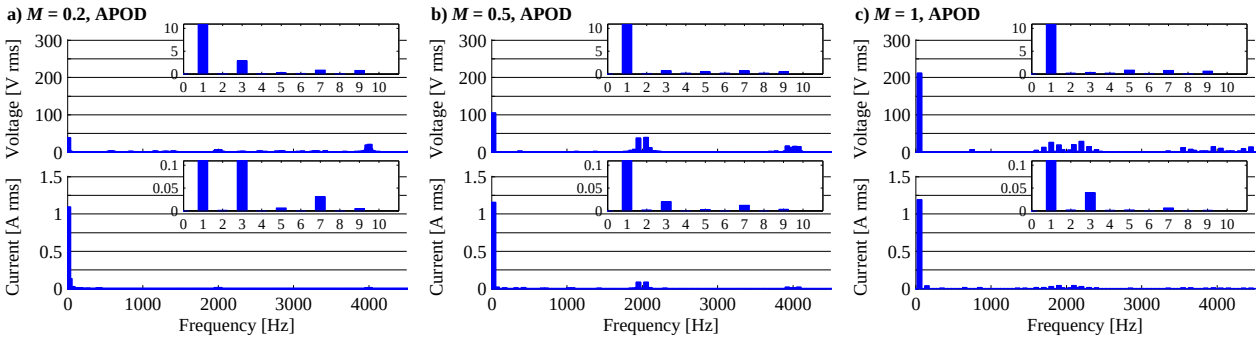


Fig. 3.31. Experimental results: v_1 and i_1 spectra for APOD PWM and $r = 2$ for $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

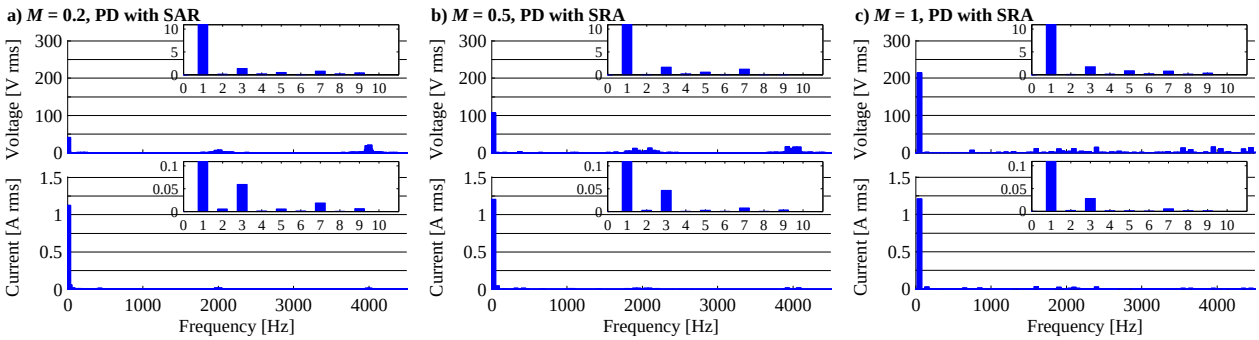


Fig. 3.32. Experimental results: v_1 and i_1 spectra for PD PWM with SAR/SRA and $r = 2$ for $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

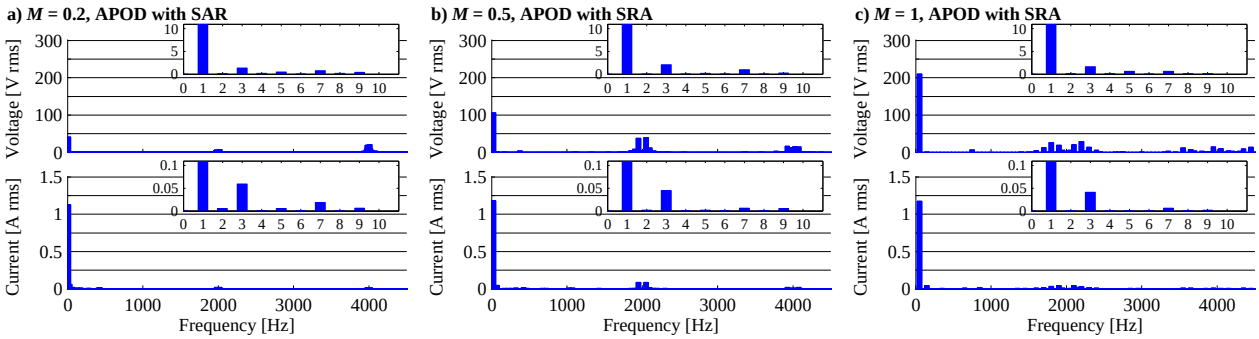


Fig. 3.33. Experimental results: v_1 and i_1 spectra for APOD PWM with SAR/SRA and $r = 2$, for $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

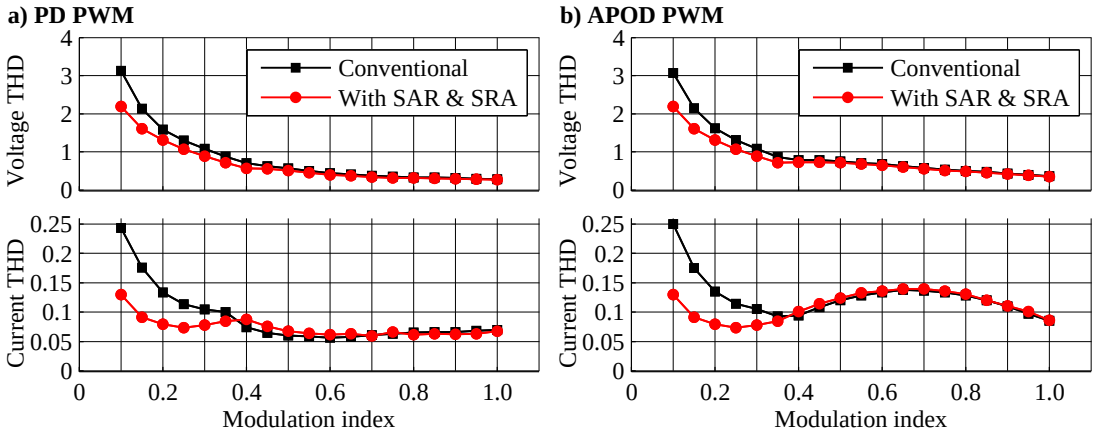


Fig. 3.34. Experimental results: THD(M) for $r = 1$, with PD (a) and APOD (b).

It should be noted that the application of closed-loop current control is not able to eliminate simultaneous switching, the main cause of dead-time spikes. Namely, closed-loop current controllers are based on negative feedback and this leads to adjustment of the phase voltage reference that results in optimal sinusoidal phase current waveform and suppression of low-order harmonics (or some other unwanted effects). Closed-loop control cannot prevent simultaneous switching of two VSIs since the same reference will be used as in (3.8). From that point of view, it is clear that closed-loop control should be applied to the 2L-OeW-2L drive only after SAR and SRA implementation.

3.4. DECOUPLED CARRIER BASED MODULATION METHODS

3.4.1. PRELIMINARY ANALYSIS

An alternative approach, when developing a PWM strategy for the OeW drive, is to consider the two VSIs as separate entities. Having in mind a dual inverter machine supply and considering (3.1) and (3.6), it seems possible to achieve multilevel phase voltage waveforms using a two-level PWM method [Dujic et al. (2009)] for each five-phase VSI separately. The basic idea is to decompose the control of the complete system into two sub-problems of a lower level of complexity, by splitting the total reference into individual references of the two inverters. By doing so, it becomes possible to apply well-known SV and CB PWM methods for two-level inverters [Dujic et al. (2009), Levi et al. (2012)] to two individual two-level inverters at each set of winding ends. Hence, this kind of modulation strategies are referred to as “decoupled” methods.

Common to all decoupled modulation methods is splitting of the original phase voltage reference into two parts, in order to share it between two VSIs. Modulation is performed later, separately for v_{1k}^* and v_{2k}^*, which are voltage references

for VSI_1 and VSI_2 leg outputs, respectively. Since decoupling affects the voltage references only, it is applicable to both SV and CB PWM methods.

In the case of 2L-OeW-2L five-phase topology, the decoupled SV PWM method is used in [Levi et al. (2012), Satiawan (2012), Bodo (2013)] for $r = 1$ and in [Jones et al. (2014)] for $r = 2$. In this section however, the same approach is covered considering dc-link voltage ratio as a degree of freedom, which allows an easier comparison with the results obtained for coupled strategies in the previous section. As expected, presented results show that the decoupled CB PWM approach has the same performance, but lower algorithm complexity, when compared with decoupled SV PWM methods in [Levi et al. (2012), Satiawan (2012), Bodo (2013), Jones et al. (2014)].

Clearly, there are several ways to realise decoupled control for the OeW drive. In other words, one is able to perform reference sharing between the VSI modulators using different approaches and criteria. Probably the most important parameters to be considered are the dc-link voltages of the two inverters, which should be maximally utilised. At the same time, the two inverters can be operated with different switching frequencies. One of the proposed methods in [Reddy et al. (2011)] uses switching frequencies and phase voltage references for two inverters that are proportional to their dc-link voltages.

In [Corzine et al. (2006)] the original sinusoidal voltage reference is shared based on the harmonic content, using SV PWM methods for a three-phase open-end winding drive, supplied from two three-level inverters. The primary, so called bulk inverter (realised using slow-switching but high-voltage blocking components) is operated at fundamental frequency (so-called square-wave modulation). The secondary (conditioning) inverter is operated at a higher switching frequency, with the aim to filter out the unwanted low-order harmonic content. Although this method is not referred to as a reference sharing algorithm, the analogy is obvious, since both inverters are independently operated. This method however is not applicable to a 2L-OeW-2L topology, due to an insufficient number of switching states as will be explained in Chapter 6, where so-called bulk and conditioning method is analysed.

In this section reference sharing algorithms based on combining two sinusoidal references with different amplitudes are analysed. This concept is based on splitting the original phase voltage reference into two parts, which have their maximum amplitudes proportional to the dc-link voltages of the VSIs. Both VSIs are operated with the same switching frequency. Pioneering results, for multiphase drives, can be found in [Jones et al. (2010), Levi et al. (2012), Satiawan (2012), Bodo (2013), Jones et al. (2014)].

3.4.2. REFERENCE SHARING ALGOTIHMS BASED ON DC-LINK VOLTAGE RATIO

As explained above, both VSIs modulators are fed with sets of five sinusoidal references, labelled with v_{1k}^* and v_{2k}^* for VSI_1 and VSI_2, respectively. The fundamental frequencies of v_{1k}^* and v_{2k}^* are equal and determined with an overall modulation index M, in accordance with (3.8). Their amplitude however, is determined with modulation indices M_1 and M_2, associated with VSI_1 and VSI_2, respectively. Clearly, in order to utilise the full potential of the two available dc-link voltages, one has to take into account the dc-link voltage ratio. At the same time, SAR should be implemented, in order to reduce switching losses in the low modulation index range. As shown in the previous section, it is sufficient to operate the drive in two-level mode for $M \leq M_{max}/(r + 1)$, using only VSI_2.

In [Jones et al. (2010), Levi et al. (2012), Satiawan (2012), Bodo (2013), Jones et al. (2014)], the inverter that operates in the low modulation index range is referred to as VSI_1, while VSI_2 stands for the inverter that works in PWM mode only in multilevel range, for $M > M_{max}/(r + 1)$. Here, the same labels and terminology as in Section 3.3 are used, in

order to make easier comparison within this chapter, as well as with the results in following chapters. Calculation of M_1 and M_2 is based on the following expressions:

$$M_1 = \begin{cases} 0 & \text{if} \quad 0 \le M \le M_{max}/(r+1) \\ (r+1)\cdot\left(M - M_{max}/(r+1)\right) & \text{if} \quad M_{max}/(r+1) \le M \le M_{max} \end{cases}$$
$$M_2 = \begin{cases} (r+1)\cdot M & \text{if} \quad 0 \le M \le M_{max}/(r+1) \\ M_{max} & \text{if} \quad M_{max}/(r+1) \le M \le M_{max} \end{cases} \tag{3.16}$$

Obtained modulation indices, together with phase voltage references from (3.8) should be used for formation of two VSI voltage reference sets. They are referred here as v_{1k}^* and v_{2k}^*, for VSI_1 and VSI_2, respectively. It is important to stress here that for *V/f* control one has to take care about the overall phase voltage reference amplitude and fundamental frequency. Hence, M_1 and M_2 correspond to v_{1k}^* and v_{2k}^* amplitudes only. Frequencies of v_{1k}^* and v_{2k}^* references have to be determined with the original M, used in (3.8) and (3.16). In order to make the final calculations simpler, $R_{offset} = 0$ case is here assumed. Final v_{1k}^* and v_{2k}^* can be obtained using the following expression:

$$v_{1k}^*(t) = \frac{1}{2} + \frac{M_1}{M}\cdot v_k^*(t)$$
$$v_{2k}^*(t) = \frac{1}{2} - \frac{M_2}{M}\cdot v_k^*(t) \tag{3.17}$$

Equations (3.16) and (3.17) represent so-called unequal reference sharing (URS). Note that reference dc component of 1/2 is added only because it is chosen that carrier signals should be in the range from 0 to 1, which makes the final implementation easier. The complete URS modulation strategy block diagram is shown in Fig. 3.35. The VSI modulation indices and voltage references with respect to the overall modulation index and commanded phase voltage reference are shown in Fig. 3.36. Depending on carriers C_1 and C_2 mutual phase disposition, as explained in [Bodo (2013)], two different URS methods exist. The first method, URS1, is based on carrier signals in phase disposition, while URS2 relies on carriers with mutual phase angle of 180°.

There is however, another option: for $M < 2/(r+1)\cdot M_{max}$, an equal reference sharing (ERS) can be used. Naturally, for equal dc-link voltages this border corresponds with maximal modulation index value, while in the case of unequal dc-link voltages, one has to adopt a different approach for $2/(r+1)\cdot M_{max} < M < M_{max}$. A similar approach, which is based on the proportional reference sharing (PRS) between two inverters, regardless of their dc-link voltages, is applicable for any M and r value. However, ERS and PRS, employ both inverters even for low M values, which results in worse harmonic performance than URS [Bodo (2013)]. Hence, only URS is considered here, covering values of r from 1 to 4.

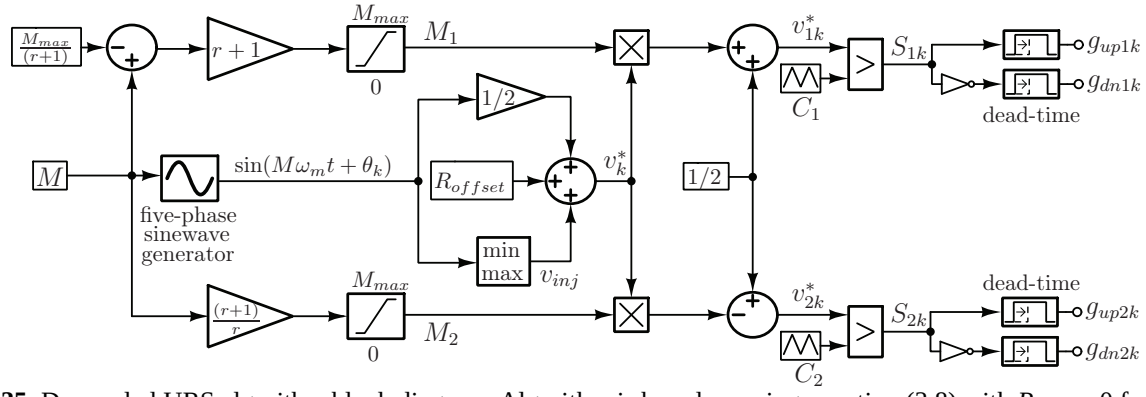


Fig. 3.35. Decoupled URS algorithm block diagram: Algorithm is based on using equation (3.8) with $R_{offset} = 0$ for initial phase voltage reference formation and (3.16) and (3.17) for obtaining the final VSI_1 and VSI_2 references. Their comparison with two carrier signals results in the final VSI switching states.

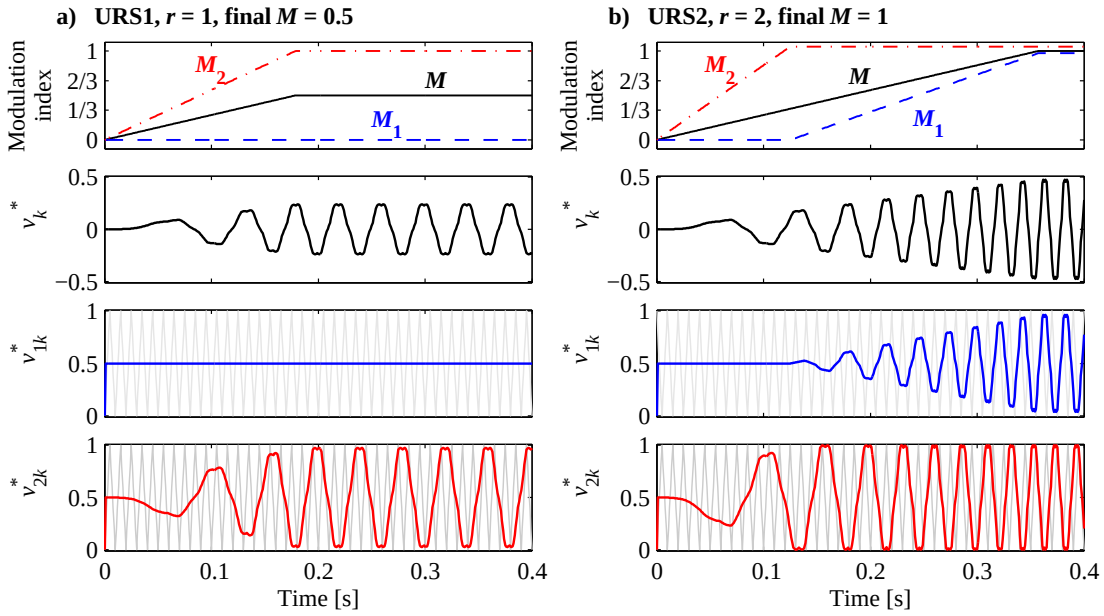


Fig. 3.36. Formation of VSI voltage references using algorithm from Fig. 3.36: *V/f* acceleration with URS1, $r = 1$ and final M equal to 0.5 (a) and with URS2, $r = 2$ and final M equal to 1 (b). Difference between URS1 and URS2 is only in carrier signal disposition (carrier frequency is reduced to 100 Hz, for better visualisation).

3.4.3. SIMULATION RESULTS

The decoupled modulation methods are tested using numerical simulations and the parameters given in Appendix 1. Obtained waveforms for several values of r and $M = 1$, the same as in Figs. 3.10 and 3.11, are depicted in Figs. 3.37 and 3.38. The results demonstrate that the dc-link voltage ratio does not have a strong influence on URS1 and URS2 performance regarding phase voltage waveforms, while URS1 results in somewhat higher phase current switching ripple as r increases. The second observation is that there are no dead-time spikes present in the phase voltage waveforms. This is due to the fact that the phase voltages obtained with URS1 and URS2 contain switching transitions between all four voltage levels throughout the fundamental period, while in the case of PD and APOD (Fig. 3.10 and 3.11) only the two nearest voltage levels were used, resulting in optimal four-level phase voltage waveforms, polluted only with unwanted transitions, during dead-time intervals. Hence, dead-time spike phenomenon is not present in the decoupled methods, due to absence of simultaneous switching.

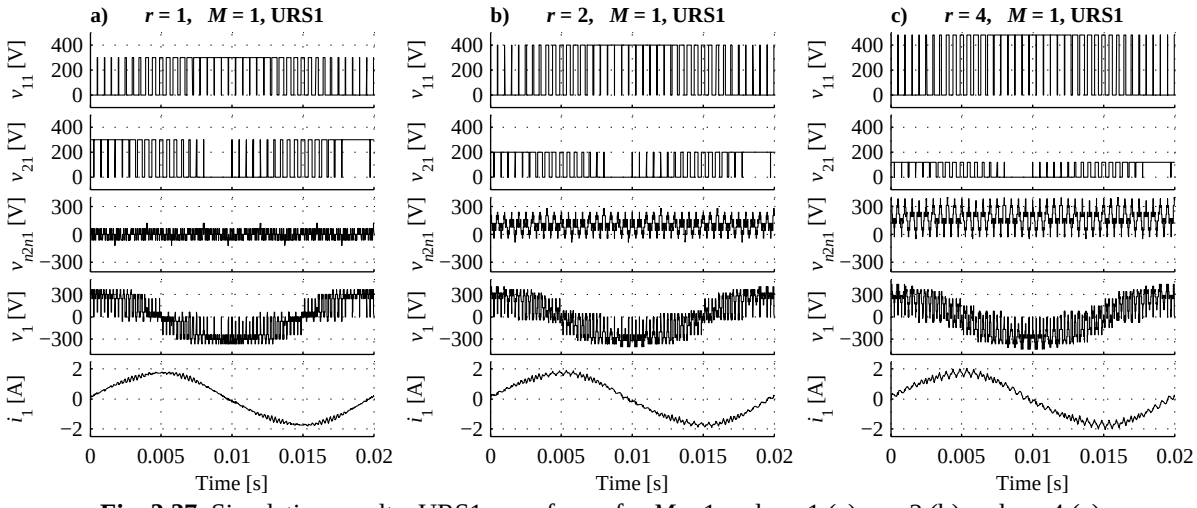


Fig. 3.37. Simulation results: URS1 waveforms for $M = 1$ and $r = 1$ (a), $r = 2$ (b) and $r = 4$ (c).

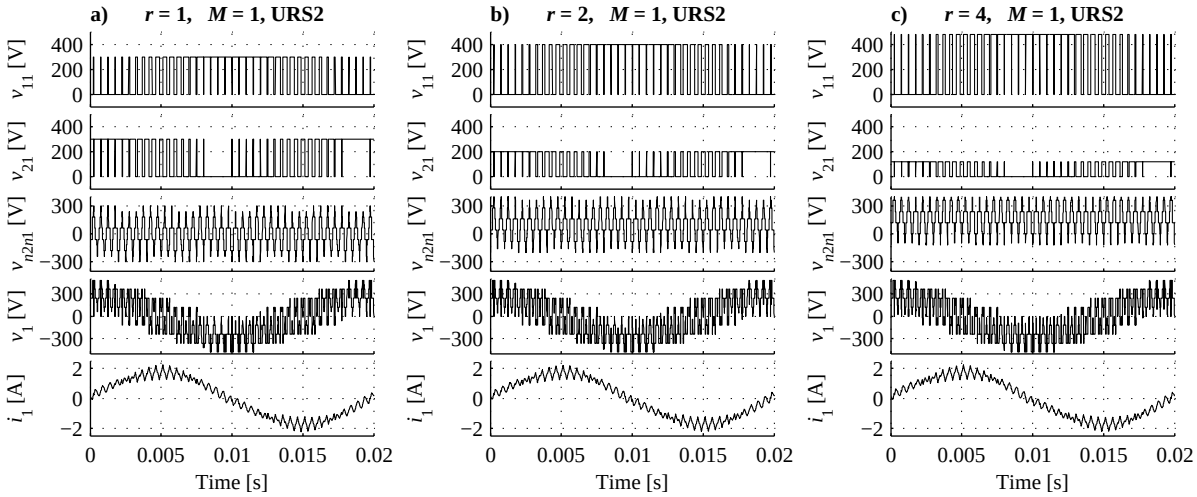


Fig. 3.38. Simulation results: URS2 waveforms for $M = 1$ and $r = 1$ (a), $r = 2$ (b) and $r = 4$ (c).

3.4.4. INFLUENCE OF THE DC-LINK VOLTAGE RATIO ON DRIVE HARMONIC PERFORMANCE

The harmonic performance of the 2L-OeW-2L drive is examined against dc-link voltage ratio, for URS1 and URS2. The simulation results are presented in Fig. 3.39. It is shown that the transition from two-level to multilevel operation leads to a noticeable increase in harmonic pollution. This is especially pronounced for high values of r. When $r = 1$, transition between two-level and multilevel modes takes place at $M = 0.525$. When $M < 0.525$, two-level operation is performed by VSI_2 ($V_{dc2} = 300$ V) only. Above $M = 0.525$, VSI_1, which has the same dc-link voltage value, $V_{dc1} = 300$ V, starts modulation due to the residual part of the original phase voltage reference, according to (3.16) and Figs. 3.36. Since the amplitude of v_{1k}^* is very small, for example in the case of $M = 0.6$, harmonic pollution increases due to dead-time effects and low duty ratio on VSI_1 side (in this case, $M_1 = 0.15$, $M_2 = 1.05$). The same thing happens around $M = 0.25$ for $r = 4$. In this case however, the increase in THD around the border between two-level and multilevel modes is much higher. This can be explained by considering that two-level modulation with VSI_2 and $V_{dc2} = 120$ V was optimal for $M < 0.2$, but modulation for $M = 0.25$ is far from optimal since the amplitude of v_{1k}^* is very small, while VSI_1 dc-link voltage is 480 V. Hence, in these cases there is an increased low-order harmonic content, which leads to an increased THD. It can be concluded that for both URS1 and URS2, $r = 2$ is the superior choice. Comparison with Fig. 3.20 shows that decoupled modulation results in a somewhat higher harmonic content than the coupled methods.

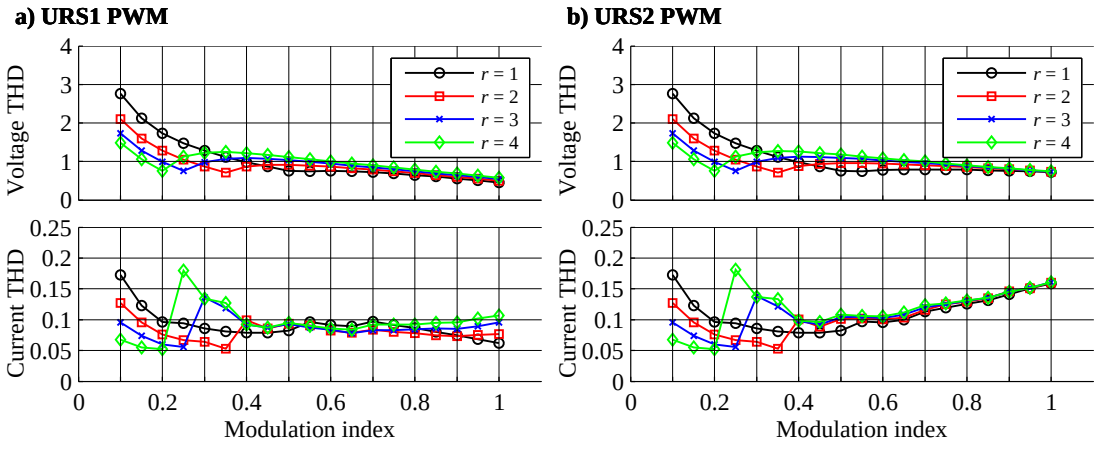


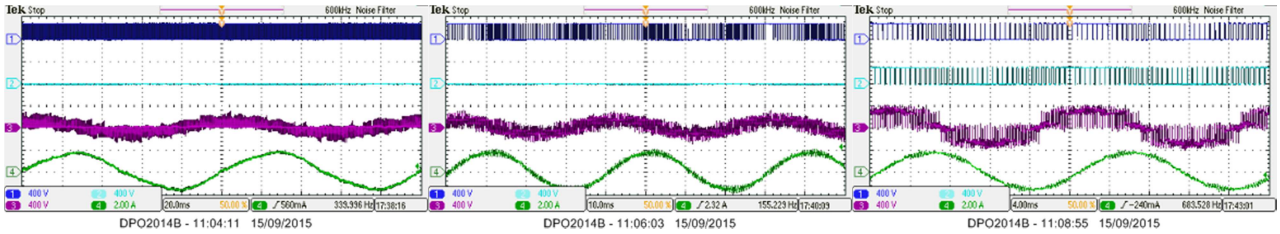
Fig. 3.39. Simulation results: phase voltage and phase current THD(M) for URS1 (a) and URS2 (b) with different r.

Furthermore, decoupled modulation does not offer a degree of freedom equivalent to R_{offset} as in the case of coupled methods. This is because the decoupled methods rely on the inverters' sine references (v_{1k}^* and v_{2k}^*) being compared with a single carrier signal (Figs. 3.35 and 3.36), so there is no possibility to choose between the different numbers of voltage levels, other than two-level and multilevel modes.

3.4.5. EXPERIMENTAL RESULTS

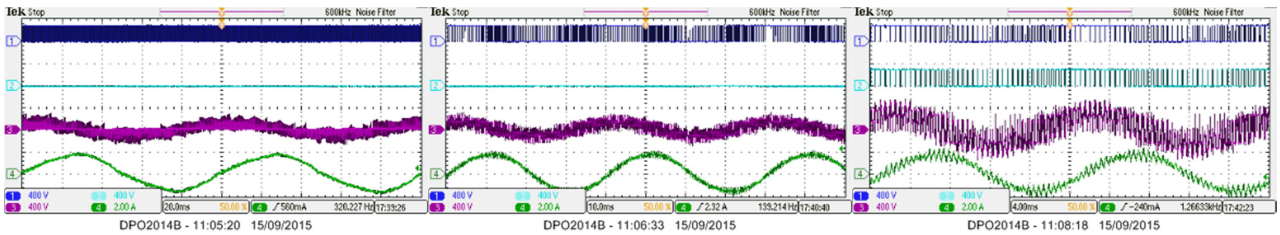
Following on from the previously analysed simulation results, it appears that case $r = 2$ ($V_{dc1} = 400$ V, $V_{dc2} = 200$ V) is the most beneficial, due to the lowest harmonic distortion of the phase voltages and currents. Hence, this case is experimentally verified. However, in order to allow consistent and complete comparison between coupled modulation methods, and decoupled strategies implemented using SV PWM [Satiawan (2012), Bodo (2013)], experimental results for $r = 1$ are obtained as well. In both cases, the maximal value of M_2 is set to 1.03, in order to avoid pulse dropping in VSI_2 operation.

Experimental setup parameters are the same as in Section 3.3 (Appendix 2). Captured oscilloscope screenshots, showing v_{21} (CH1), v_{11} (CH2), v_1 (CH3) and i_1 (CH4) for different M are shown in Figs. 3.40 and 3.41, with URS1 and URS2 respectively, for $r = 1$. Phase voltage and current spectra are shown in Figs. 3.42 and 3.43. Comparison with results in [Satiawan (2012), Bodo (2013)] confirms that CB PWM implementation of URS results in the same performance as SV PWM.



a) b) c)

Fig. 3.40. Experimental results: waveforms with URS1 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 3.41. Experimental results: waveforms with URS2 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

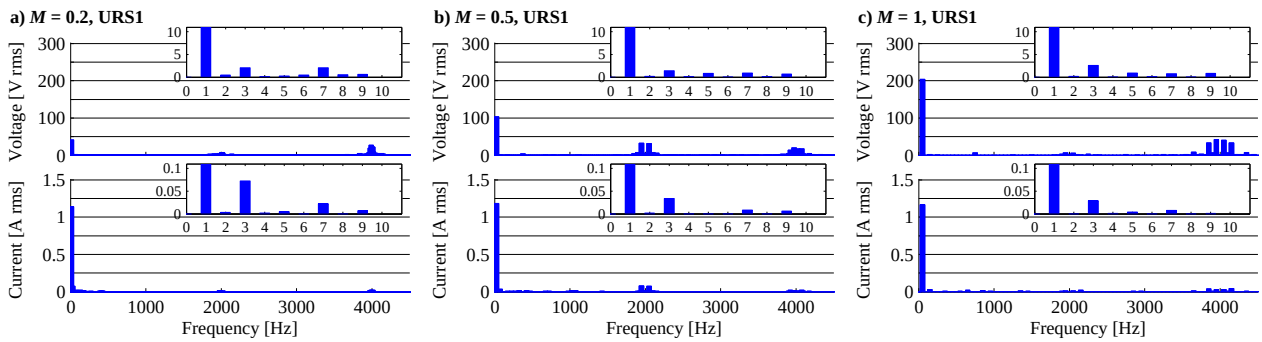


Fig. 3.42. Experimental results: v_1 and i_1 spectra for URS1 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c). Subfigure in the top right corner shows rms values of the first 10 low-order harmonics.

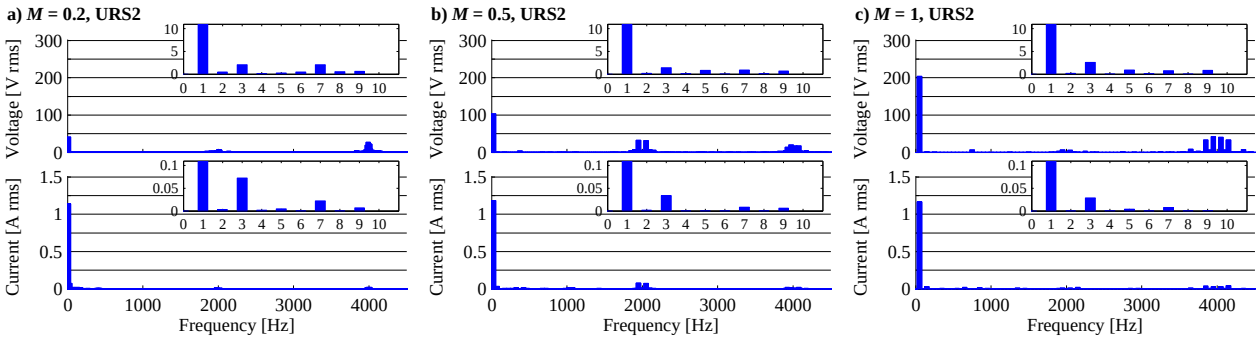
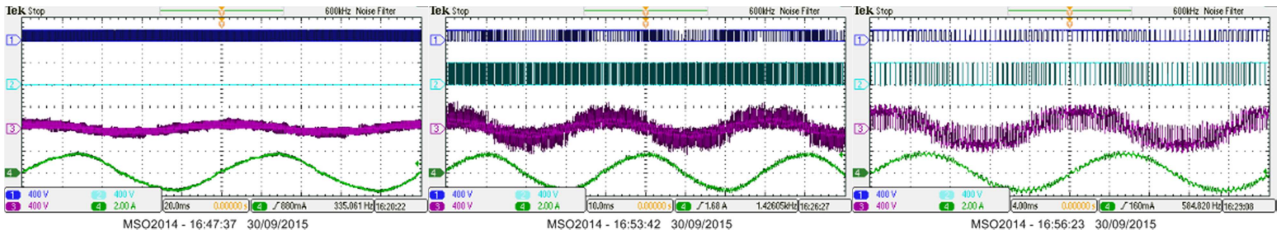


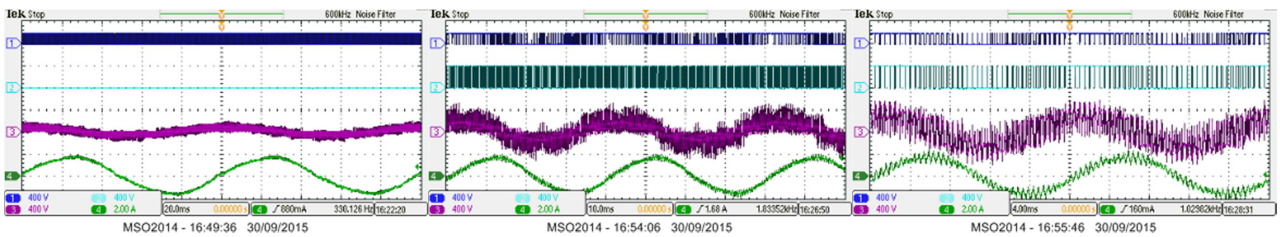
Fig. 3.43. Experimental results: v_1 and i_1 spectra for URS2 PWM and r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

It should be noted that both URS1 and URS2 are in essence the same modulation strategy up to M = 0.525, if the dc-link voltages are equal, since only one VSI operates. This does not seem optimal regarding OeW structure, since the second inverter does not operate in the lower half of the modulation index (i.e. speed) range. From this point of view, it seems that decoupled methods are better suited for unequal dc-links. Fortunately, the algorithm presented here (Fig. 3.35) requires no modification in order to be applied to an arbitrary dc-link voltage ratio. Hence, the same algorithm (equations (3.8), (3.16), (3.17), diagram in Fig. 3.35) is applied for r = 2. Obtained results are shown in Figs. 3.44-3.48. Waveforms in Figs. 3.44 and 3.45 are the same as in [Jones et al. (2014)] demonstrating that SV and CB methods are equivalent regardless of r. Spectra presented in Figs. 3.46 and 3.47 show that both URS methods result in somewhat lower low-order phase current harmonics with r = 2 and M = 0.2. This is due to the lower dc-link voltage of VSI_2, for commanded phase voltage reference, when compared with the case of r = 1, where dead-time effects for M = 0.2 are more dominant. With M = 0.5, r = 1 results in better performance, since decoupled modulation in this case effectively leads to two-level operation with M_1 = 0 and M_2 = 1, while r = 2 results in multilevel operation with M_1 = 0.45, M_2 = 1.03, but with combined dead-time effects from both VSIs. Comparison of THDs in Fig. 3.48 shows that URS1 has superior performance, not only because it is less dependent on M, but also due to the fact that for the same dc-link voltage ratio URS2 always results in higher THD. URS2 has similar performance for both r values. Once again, due to limited number of available oscilloscope channels, v_{n2n1} is not shown. Analysis of this parameter can be performed by considering the simulation results shown in Figs. 3.37 and 3.38. It can be seen that URS1 introduces much lower ripple in common mode voltage, regardless of r.



a) b) c)

Fig. 3.44. Experimental results: waveforms with URS1 PWM and r = 2, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).



a) b) c)

Fig. 3.45. Experimental results: waveforms with URS2 PWM and r = 2, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

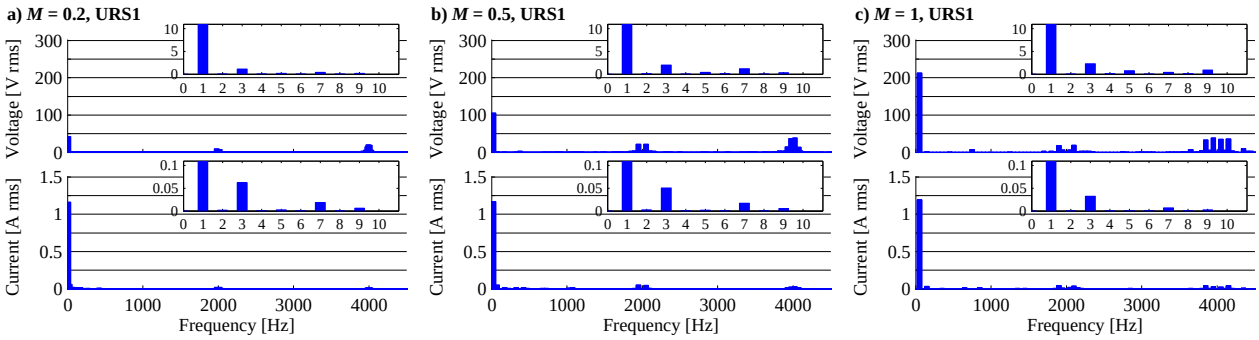


Fig. 3.46. Experimental results: v_1 and i_1 spectra for URS1 PWM and r = 2, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

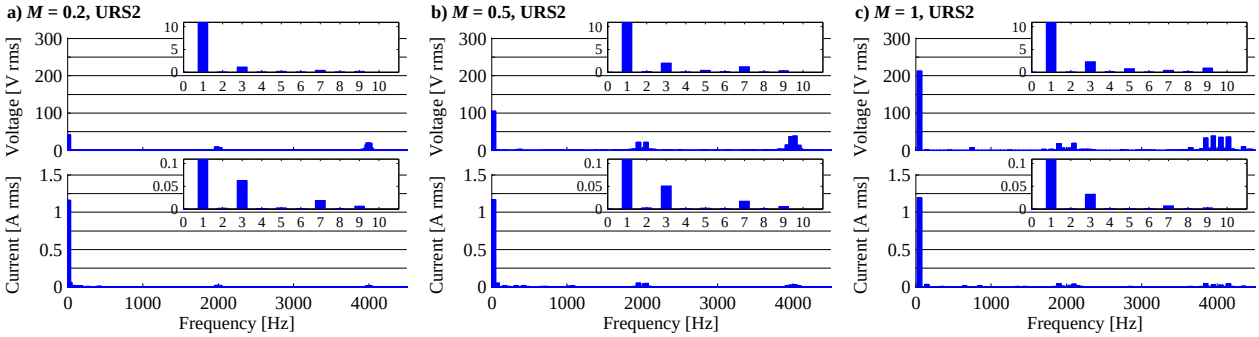


Fig. 3.47. Experimental results: v_1 and i_1 spectra for URS2 PWM and r = 2, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

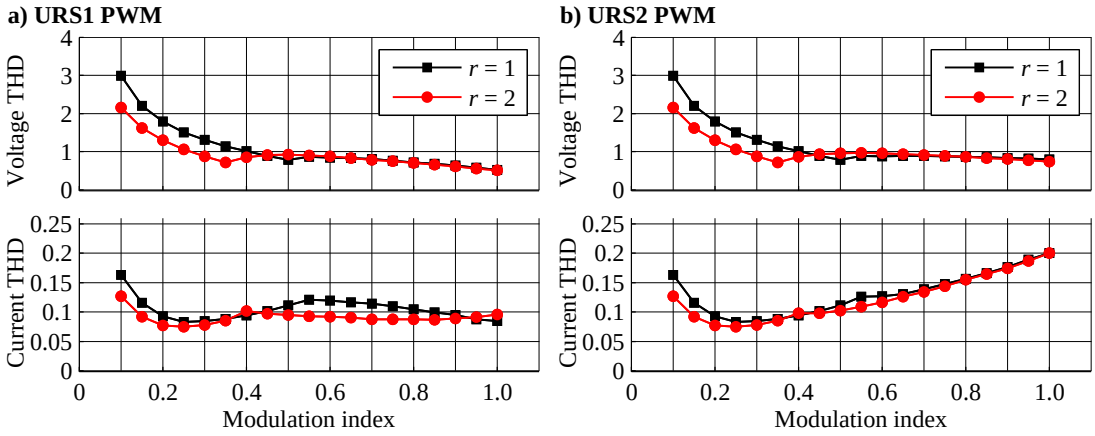


Fig. 3.48. Experimental results: THD(M) for r = 1 and 2, with URS1 (a) and URS2 (b).

3.5. SUMMARY

An open-end winding topology that comprises two two-level inverters is analysed in this chapter. Two kinds of modulation strategies are explained and their influence on the drive harmonic performance is investigated. Firstly, the drive performance is examined using numerical simulations in order to identify suitable values of the dc-link voltage ratio, a parameter that is seen as an additional degree of freedom, offered by the OeW topology. It is shown that unequal dc-link voltages in the ratio V_{dc1}:V_{dc2} = 2:1 (r = 2) provides optimal harmonic performance, while previous research efforts were mainly focused on equal dc-link voltages. Hence, these two cases are compared and experimentally verified. It is demonstrated that coupled modulation methods, which are developed starting from level-shifted CB PWM methods for multilevel single-sided drives, have superior performance, compared to decoupled methods, which are based on reference sharing algorithms. It is shown that operation with unequal dc-link voltages and coupled CB PWM schemes can lead to four-level phase voltage waveforms, while decoupled methods for the same dc-link voltage ratios result in

worse harmonic performance. This is because the coupled methods are designed considering both inverters in the topology as one combined structure, while decoupled methods rely on separate and independent modulation of the VSIs. Hence, simultaneous switching action of the inverters can be used to obtain one additional voltage level, but only in the case of coupled CB PWM schemes. Expected performance of this approach is achieved only after elimination of so-called dead-time spikes, which are present due to the triggering of unwanted voltage levels during simultaneous dead-time intervals in the inverters' legs on the two sides of the phase stator winding.

Both coupled and decoupled approaches are analysed in terms of CB PWM for open-loop control in V/f manner. Comparison with earlier research results confirmed once again that CB and SV concepts are equivalent in terms of harmonic performances. As reported earlier, CB PWM seems more practical for multiphase drives because of the reduced algorithm complexity and lower computational requirements. Furthermore, the presented analysis shows that modification of CB PWM for different dc-link voltage ratios is simpler for the 2L-OeW-2L drive when compared to the SV PWM approach. This is due to the fact that the same set of equations and modulation scheme can be used for CB PWM, while the choice of which space vectors to apply, and their dwell times, are heavily dependent on r. It is demonstrated that the 2L-OeW-2L drives offer a possibility to use only one inverter for modulation indices lower than $M_{max}/(r + 1)$. This operation mode can be used as a replacement for two-level modulation that relies on simultaneous switching of the inverters. This leads to a reduction of the switching losses and an improvement in harmonic performance, if the inverter with a lower dc-link voltage is used.

Chapter 4

FIVE-PHASE OPEN-END WINDING DRIVES WITH ONE THREE-LEVEL INVERTER AND ONE TWO-LEVEL INVERTER

4.1. INTRODUCTION

In this chapter, an open-end winding topology that employs one three-level inverter and one two-level inverter is analysed. This structure is referred as the 3L-OeW-2L drive and it is examined for a five-phase drive. The three-level inverter (VSI_1) is realised using a neutral point diode-clamped (NPC) topology [Kouro et al. (2012)]. VSI_2 is a conventional two-level voltage source inverter. This choice of three-level topology is mainly driven by the available hardware in LJMU EMD laboratory. However, the developed modulation strategies, presented in this chapter, can be extended to other topologies, where VSI_1 is realised using an active neutral point clamped (ANPC) VSI often referred to as T-type NPC or a neutral point piloted (NPP) converter [Rodriguez et al. (2009)]. Analysis of modulation strategies for three-level inverters which are useful for this research can be found in [Rodriguez et al. (2009), Kouro et al. (2012), Dordevic (2013)]. Firstly, the topology is analysed using the equivalent model approach. It is shown that the 3L-OeW-2L can be made equivalent to a four-, five- or six-level single-sided supply. The number of levels depends on the dc-link voltage ratio (r), which is similar to the 2L-OeW-2L case. As in Chapter 3, two coupled and two decoupled CB PWM methods are developed and tested using simulations and an experimental prototype. The analysis shows that $r = 2$ is optimal in the case of PD and APOD PWM methods, although it leads to four-level operation, which is the lowest number of levels obtainable with a 3L-OeW-2L topology. Results from this chapter are reported in [Darijevic et al. (2015a), Darijevic et al. (2015b), Darijevic et al. (2015c)]. In the case of decoupled inverter control, the dc-link voltage ratio has a very small impact on the drive harmonic performance. At the same time, only minor differences between URS1 and URS2 are observed, contrary to the 2L-OeW-2L drive case, where URS1 resulted in superior harmonic performance.

4.2. MODELLING AND ANALYSIS OF THE TOPOLOGY

The 3L-OeW-2L drive and its equivalent model are shown in Figs. 4.1 and 4.2, respectively. Leg voltages of VSI_1 and VSI_2 are denoted with v_{1k} and v_{2k} for the k^{th} drive phase and measured with respect to the bottom dc-link rail of the corresponding inverter (v_{n1} and v_{n2}). Phase voltage and phase current in the k^{th} drive phase are labelled with v_k and i_k, respectively (Fig. 4.2). In Fig. 4.1, two complementary pairs of power switches in VSI_1 are denoted with superscripts "*a*" and "*b*" (S^a_{up1k} and S^a_{dn1k}, S^b_{up1k} and S^b_{dn1k}) for the k^{th} drive phase. Complementary switches in VSI_2 are labelled as S_{up2k} and S_{dn2k}. The rule is that complementary switches with the indices "*up*" and "*dn*" should not be turned on at the same time in order to prevent dc-link short circuiting. Having that in mind, analysis is simplified using switching states, which represent complementary pairs in Fig. 4.1:

- $S^a_{1k} = 1$ if S^a_{up1k} or D^a_{up1k} is turned on; $S^a_{1k} = 0$ if S^a_{dn1k} or D^a_{dn1k} is turned on;
- $S^b_{1k} = 1$ if S^b_{up1k} or D^b_{up1k} is turned on; $S^b_{1k} = 0$ if S^b_{dn1k} or D^b_{dn1k} is turned on;
- $S_{2k} = 1$ if S_{up2k} or D_{up2k} is turned on; $S_{2k} = 0$ if S_{dn2k} or D_{dn2k} is turned on.

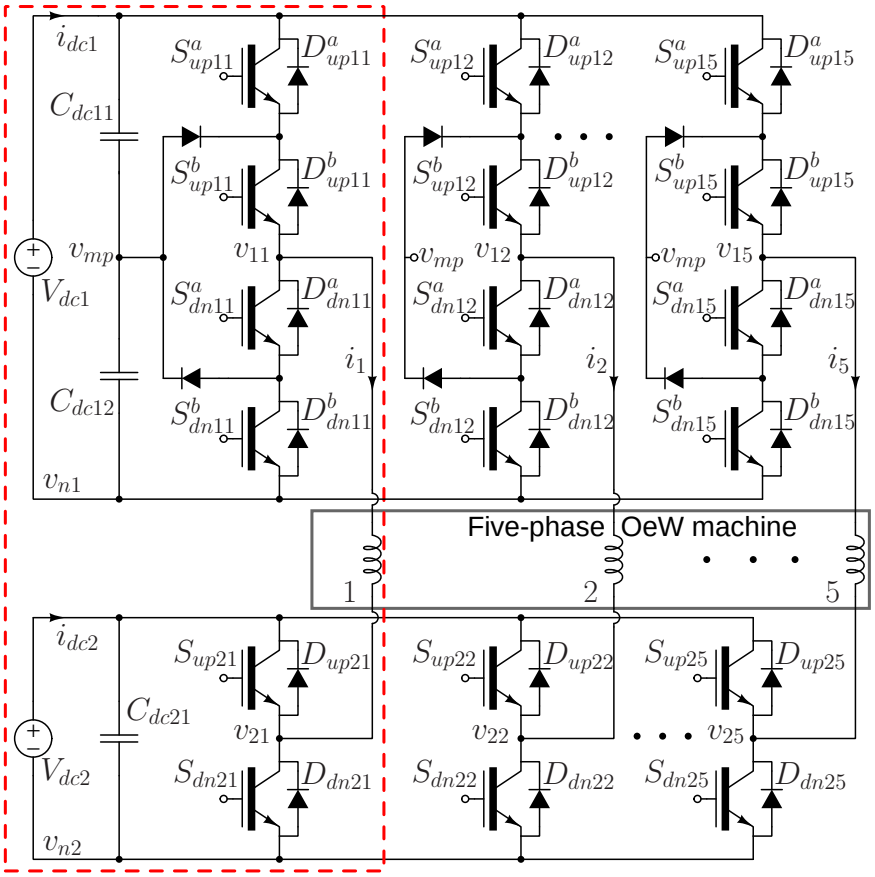


Fig. 4.1. Five-phase multilevel open-end winding drive with one three-level inverter and one two-level inverter (3L-OeW-2L topology). Equivalent model is denoted with dashed red line.

Regardless of the chosen modulation strategy and rest of the drive, it is clear from Fig. 4.1 that the output voltage of VSI$_1$ (i.e. v_{1k} with respect to v_{n1}) is determined with S^a_{1k} and S^b_{1k}:

- S^a_{1k} = 1 and S^b_{1k} = 1 results in $v_{1k} = V_{dc1}$;
- S^a_{1k} = 0 and S^b_{1k} = 1 results in $v_{1k} = v_{mp} = V_{dc1}/2$;
- S^a_{1k} = 1 and S^b_{1k} = 0 results in v_{1k} = Z;
- S^a_{1k} = 0 and S^b_{1k} = 0 results in v_{1k} = 0;

The third switching combination listed above results in the off state of S^b_{up1k} and S^a_{dn1k}, meaning that the NPC leg output voltage is in this case determined by conduction of antiparallel diodes and phase current sign. This is referred as a high impedance state (*Z*). Switching between 0 and $V_{dc1}/2$ is referred to in the rest of the text as low-side PWM operation, while high-side PWM corresponds with switching between $V_{dc1}/2$ and V_{dc1}.

The equivalent drive model, depicted in Fig. 4.2, shows that there are $2^3 = 8$ possible switching combinations. This is summarised in Table 4.1 using the individual dc-link voltage values and in Table 4.2, where voltages are normalised with V_{dc}. Inspection of Table 4.2 shows that the 3L-OeW-2L drive is capable of producing up to six voltage levels. For some values of r however, similarly to the 2L-OeW-2L case, certain switching combinations result in the same phase voltage level, which effectively leads to a reduction of the overall number of voltage levels. For $r = 1$, switching combinations 2 and 7 (Table 4.1 and 4.2) result in the same voltage level. For $r = 2$, voltage levels of $V_{dc}/(r + 1)$ and 0 can be obtained using two different switching combinations. This is a direct consequence of the dc-link voltage ratio, since $V_{dc1} = 2 \cdot V_{dc2}$ results in equivalence $v_{mp} = V_{dc1}/2 = V_{dc2}$ (Fig. 4.1).

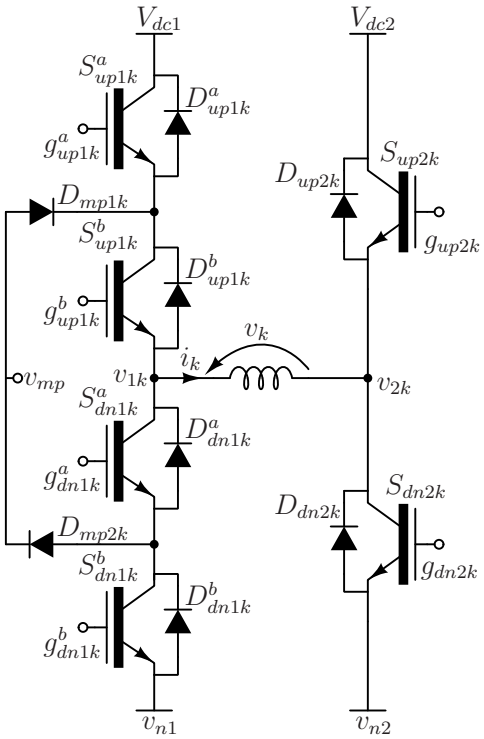


Fig. 4.2. Equivalent model of 3L-OeW-2L drive.

Table 4.1. Relationship between switching states and leg and phase voltages.

N	S^a_{1k}	S^b_{1k}	S_{2k}	v_{1k} [V]	v_{2k} [V]	Equivalent v_k [V]
1	1	1	0	V_{dc1}	0	$V_{dc1} - 0$
2	1	1	1	V_{dc1}	V_{dc2}	$V_{dc1} - V_{dc2}$
3	1	0	0	Z	0	$Z - 0 = Z$
4	1	0	1	Z	V_{dc2}	$Z - V_{dc2}$
5	0	1	0	$V_{dc1}/2$	0	$V_{dc1}/2 - 0$
6	0	1	1	$V_{dc1}/2$	V_{dc2}	$V_{dc1}/2 - V_{dc2} = 0$
7	0	0	0	0	0	0
8	0	0	1	0	V_{dc2}	$0 - V_{dc2} = -V_{dc2}$

As with the other OeW drive topologies, the overall dc-link voltage supply is equal to $V_{dc} = V_{dc1} + V_{dc2}$. This is clear from the equivalent drive model, where in the case of $v_{n1} = v_{n2}$ one would find that maximal and minimal equivalent phase voltage are equal to V_{dc1} and $-V_{dc2}$, respectively. Maximal voltage amplitude across the load is equal to $(V_{dc1} + V_{dc2})/2$.

Table 4.2. Relationship between switching states, normalised leg and phase voltages.

N	S^a_{1k}	S^b_{1k}	S_{2k}	v_{1k}/V_{dc}	v_{2k}/V_{dc}	Equivalent v_k/V_{dc}
1	1	1	0	$r/(r + 1)$	0	$r/(r + 1)$
2	1	1	1	$r/(r + 1)$	$1/(r + 1)$	$(r - 1)/(r + 1)$
3	1	0	0	Z	0	Z
4	1	0	1	Z	$1/(r + 1)$	Z
5	0	1	0	$r/(r + 1)/2$	0	$r/(r + 1)/2$
6	0	1	1	$r/(r + 1)/2$	$1/(r + 1)$	$(r/2 - 1)/(r + 1)$
7	0	0	0	0	0	0
8	0	0	1	0	$1/(r + 1)$	$-1/(r + 1)$

As in the case of the 2L-OeW-2L drive, the distance between minimal and maximal voltage levels is always equal (if normalisation with V_{dc} is used, while v_{n1} is considered as the zero potential). These two voltage levels define the co-domain for phase voltage reference, in the case of CB PWM. Development of coupled PWM methods is based on the normalised voltage level analysis, where the minimal voltage level of $-r/(r+1)$ corresponds with 0, the maximal voltage level $r/(r+1)$ corresponds with 1 while inner voltage levels are situated in between. Due to the existence of an additional voltage level on the VSI_1 side ($v_{mp} = V_{dc1}/2$) the inner voltage levels formation is more dependent on r than in the case of the 2L-OeW-2L drive. Using the equivalent models of the two drives (Figs. 3.2 and 4.2) and switching state combinations in Tables 3.2 and 4.2 one is able to calculate equivalent voltage levels for different values of r. Voltage level dependencies on r are depicted in Fig. 4.3, for both topologies. Voltage levels are denoted with $l_{1..6}$ and can be calculated using the following expressions for the 2L-OeW-2L topology (Fig. 4.3a):

$$\begin{aligned} l_1 &= 0 \\ l_2 &= 1/(r+1) \\ l_3 &= r/(r+1) \\ l_4 &= 1 \end{aligned} \tag{4.1}$$

On the other hand, the 3L-OeW-2L voltage levels require more complex calculations (Fig. 4.3b):

$$\begin{aligned} l_1 &= 0 \\ l_2 &= \begin{cases} 1/2 \cdot r/(r+1), & \text{if } r < 2 \\ 1/(r+1), & \text{if } r \geq 2 \end{cases} \qquad l_3 = \begin{cases} 1/(r+1), & \text{if } r < 2 \\ 1/2 \cdot r/(r+1), & \text{if } r \geq 2 \end{cases} \\ l_4 &= \begin{cases} 1 - 1/2 \cdot r/(r+1), & \text{if } r < 2 \\ 1 - 1/(r+1), & \text{if } r \geq 2 \end{cases} \qquad l_5 = \begin{cases} 1 - 1/(r+1), & \text{if } r < 2 \\ 1 - 1/2 \cdot r/(r+1), & \text{if } r \geq 2 \end{cases} \\ l_6 &= 1 \end{aligned} \tag{4.2}$$

Fig. 4.3a indicates that 2L-OeW-2L drive has at most two inner voltage levels and that they are produced using the same switching combinations, regardless of r. Fig. 4.3b shows that 3L-OeW-2L has four inner voltage levels, which are produced differently for $r < 2$ and $r \geq 2$. Clearly, for $r = 1$, l_3 and l_4 are equal, while $r = 2$ results in $l_2 = l_3$ and $l_4 = l_5$. Although carrier signals are time dependent variables, their amplitudes are determined with r. In order to visualise the influence of the dc-link voltage ratio on carriers' distribution, they are represented with triangular signals in the background. Using (4.2), one may conclude that the 3L-OeW-2L drive with $r = 1$, 2 and 4 results in configurations that operate with equidistant voltage levels. Based on the findings from the Chapter 3, it is expected that these cases are optimal, regarding harmonic quality of the phase voltages and currents throughout the whole modulation index range. Values of r lower than 1 are not examined since it does not seem beneficial from the semiconductor voltage stress point of view, to supply a two-level inverter with higher dc-link voltage than the three-level VSI. Clearly, only $r = 2$ results in the same voltage stress of all semiconductor devices in the drive, due to $v_{mp} = V_{dc2}$. However, since other dc-link voltage ratios lead to different performance, especially in the case of coupled CB PWM schemes, a wider range of r is examined further.

Projections of two VSI voltage space vectors on α-β and x-y planes are shown in Fig. 4.4 for different values of r. Resulting phase voltage space vectors are obtained using (3.6) and depicted in Fig. 4.5. In the case of $r = 1$ (Fig. 4.4a) VSI_1 and VSI_2 are producing different space vectors, which result in five-level operation, with equidistant voltage levels. From the overall number of switching states, only $5^5 - 4^5 = 2101$ result in unique phase voltage space vectors, which have 122 different magnitudes. Six-level configuration with $r = 1.5$ results in $6^5 - 5^5 = 4651$ unique phase voltage space vectors and 356 different magnitudes. With $r = 2$, the 3L-OeW-2L is equivalent to a four-level drive, with the same phase voltage space vector distribution as a 2L-OeW-2L with the same dc-link voltage ratio. The number of available phase

voltage space vectors is again 781, resulting in 51 different magnitudes, the same as in Fig. 3.4c. Equivalent voltage levels are equidistant. The second six-level configuration, obtained with r = 4, again results in 4651 unique phase voltage space vectors. Equidistant voltage levels lead to a more uniform distribution of space vectors in Fig. 4.5d, which cover the two planes more evenly then in the six-level case shown in Fig. 4.5b (i.e. r = 1.5). This can be concluded from the comparison of radial lines in the first sectors which correspond to different space vector magnitudes. In the case of r = 4 the overall number of available magnitudes is 245.

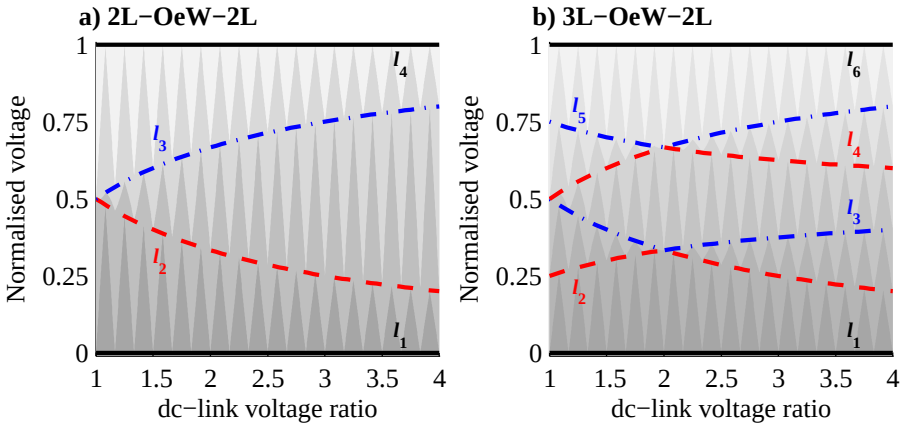


Fig. 4.3. Equivalent phase voltage levels against r for 2L-OeW-2L (a) and 3L-OeW-2L (b).

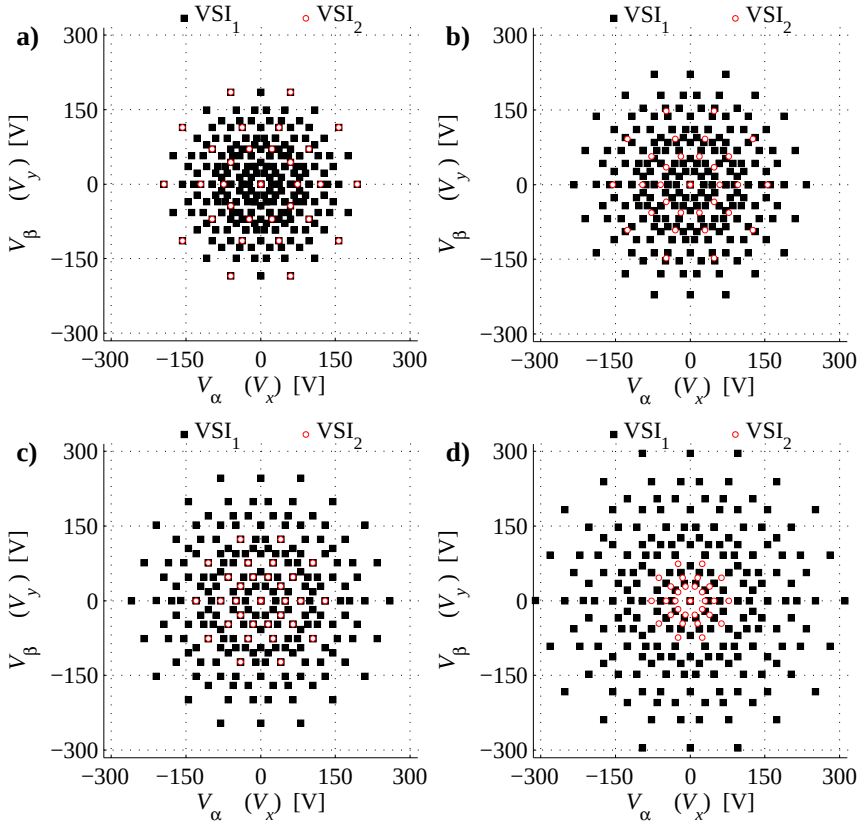


Fig. 4.4. Leg voltage space vectors of the inverters obtained with: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

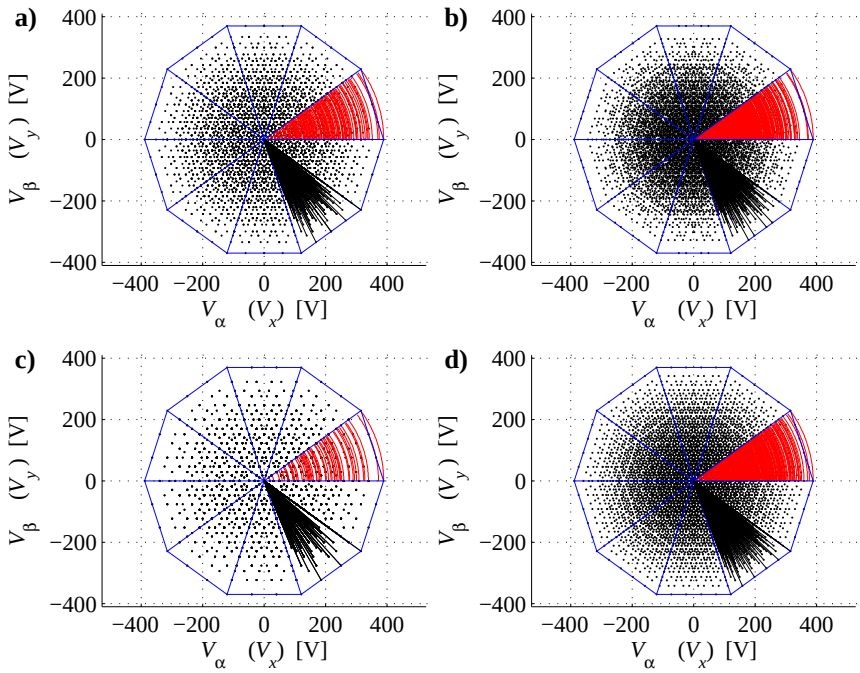


Fig. 4.5. Resulting phase voltage space vectors, obtained with (3.6), for: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d). Red radial lines in the first sector and black lines in ninth sector lines that correspond to unique vectors are used to indicate the plane coverage.

4.3. COUPLED CARRIER BASED MODULATION METHODS

4.3.1. PRELIMINARY ANALYSIS

In this section, two LS CB PWM schemes are derived for a 3L-OeW-2L drive. Carrier arrangements for different dc-link voltage ratios are shown in Figs. 4.6 and 4.7, for PD and APOD PWM, respectively, during one fundamental period (T). Denoted voltage levels are calculated under the assumption that the overall dc-link voltage is 600 V.

With r = 1, the 3L-OeW-2L drive operates as a five-level single-sided VSI. Carrier arrangements in Figs. 4.6a and 4.7a show that for M lower than $M_{max}/2 = 0.525$, the drive will naturally operate in three-level mode, since the phase voltage reference will be situated within reference zones 2 and 3 only. Clearly, this opens the possibility of using only VSI_1 for $M < M_{max}/2$, which will result in the same three-level modulation.

In the case of r = 1.5, V_{dc1} = 360 V and V_{dc2} = 240 V. It is clear from the voltage levels illustrated in Figs. 4.6b and 4.7b that two-level operation will take place for $M < 0.2$. However, using only VSI_2 in this modulation index range is not optimal, since PWM should be performed between 0 and 120 V. With this configuration, four-level operation will take place for $0.2 < M < 0.4$. For $M > 0.4$ full six-level operation is utilised. The lowest number of voltage levels is obtained when r = 2. For $M \leq 0.35$, the phase voltage reference is situated within the reference zone 2 only, leading to the two-level operation, which can be performed in single-sided mode, using VSI_2. When $M > 0.35$, four-level operation takes place.

While r = 4 and r = 1.5 result in a six-level configuration, comparison of the two cases shows that two VSIs operate differently, due to differences in formation of the $l_{2..4}$ voltage levels. Also, r = 4 results in equidistant voltage levels and two-level operation for $M < 0.2$ can be performed using VSI_2 only, without any drawbacks in harmonic performance, since V_{dc2} = 120 V.

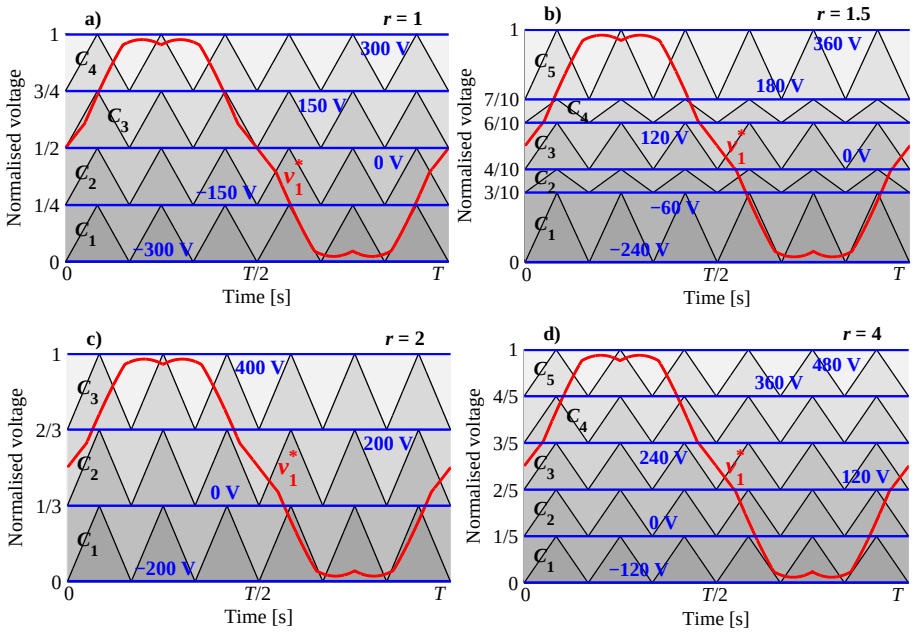


Fig. 4.6. Phase voltage reference with min-max injection and carrier signals for PD PWM for: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

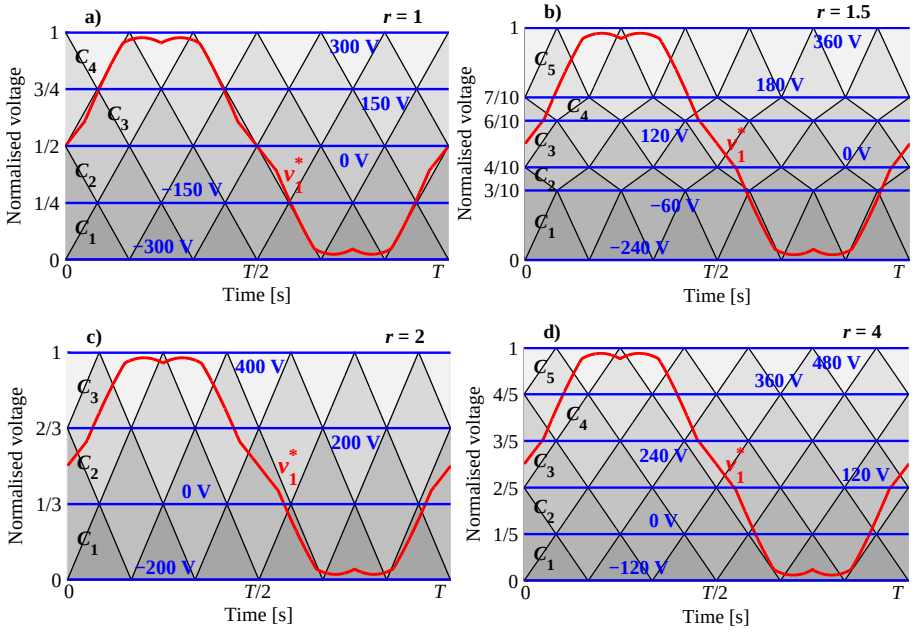


Fig. 4.7. Phase voltage reference with min-max injection and carrier signals for APOD PWM for: r = 1 (a), r = 1.5 (b), r = 2 (c), r = 4 (d).

4.3.2. MODULATION ALGORITHMS

With r = 1 the 3L-OeW-2L topology operates as a five-level drive and the phase voltage reference has to be compared with four carrier signals ($C_{1..4}$ in Figs. 4.6a and 4.7a). Since VSI_1 has two and VSI_2 one complementary IGBT+D pair, transitions between certain phase voltage levels are based on simultaneous switching of the inverters. Tables 4.1 and 4.2 show that in the case of V_{dc} = 600 V ($V_{dc1} = V_{dc2}$ = 300 V) obtainable phase voltage levels in equivalent model are of –300 V, –150 V, 0 V, 150 V and 300 V. Relations between A_{ik} (i stands for carrier signal and k for the drive phase number) and final switching states (S^a_{1k}, S^b_{1k} and S_{2k}) are derived and summarised in Table 4.3. The overall number of combinations is 2^4 = 16, but only 5 of them can be triggered in practice. This is because the phase

voltage reference cannot be smaller than C_i and higher then C_{i+h}, where i and h are positive integers. From Karnaugh maps in Tables 4.4, 4.5 and 4.6 the final expressions for S_{1k}^a, S_{1k}^b and S_{2k} are obtained in the *sums of products* form:

$$\begin{aligned} S_{1k}^a &= A_{4k} \\ S_{1k}^b &= A_{3k} + \overline{A}_{2k} \cdot A_{1k} \\ S_{2k} &= \overline{A}_{2k} \end{aligned} \tag{4.3}$$

Table 4.3. CB PWM for 3L-OeW-2L five-level configuration (r = 1) in state machine form.

Inputs				Resulting voltages			Resulting switching states		
A_{1k}	A_{2k}	A_{3k}	A_{4k}	v_k	v_{1k}	v_{2k}	S_{1k}^a	S_{1k}^b	S_{2k}
0	0	0	0	$-V_{dc2}$	0	V_{dc2}	0	0	1
1	0	0	0	$V_{dc1}/2 - V_{dc2}$	$V_{dc1}/2$	V_{dc2}	0	1	1
1	1	0	0	$0 - 0\ (V_{dc1} - V_{dc2})$	$0\ (V_{dc1})$	$0\ (V_{dc2})$	0 (1)	0 (1)	0 (1)
1	1	1	0	$V_{dc1}/2$	$V_{dc1}/2$	0	0	1	0
1	1	1	1	V_{dc1}	V_{dc1}	0	1	1	0

Table 4.4. Karnaugh map for S_{1k}^a (r = 1).

A_{1k} A_{2k} \ A_{3k} A_{4k}	0 0	0 1	1 1	1 0
00	0	X	X	X
01	X	X	X	X
11	0	X	1	0
10	0	X	X	X

Table 4.5. Karnaugh map for S_{1k}^b (r = 1).

A_{1k} A_{2k} \ A_{3k} A_{4k}	0 0	0 1	1 1	1 0
00	0	X	X	X
01	X	X	X	X
11	0	X	1	1
10	1	X	X	X

Table 4.6. Karnaugh map for S_{2k} (r = 1).

A_{1k} A_{2k} \ A_{3k} A_{4k}	0 0	0 1	1 1	1 0
00	1	X	X	X
01	X	X	X	X
11	0	X	0	0
10	1	X	X	X

The inverter operations in the reference zones are summarised in Table 4.7. It is clear from equations (4.3) that operation of VSI_1 in low- and high-side PWM switching is not symmetrical, meaning that S_{1k}^a is constant in the lower three reference zones, while S_{2k}^b is constant only in the reference zone 4. This means that switching of VSI_1 side between 0 and $V_{dc1}/2$ is more frequent then switching between $V_{dc1}/2$ and V_{dc1}. This requires a more complex controllable dc source on the NPC side, in order to keep voltages across C_{dc11} and C_{dc12} in balance, as discussed in Chapter 5. The second important conclusion is that both VSI_1 and VSI_2 operate in PWM mode in reference zone 2, which leads to dead-time spikes, as discussed in subsection 4.2.3.

Table 4.7. Operation of the VSIs vs. reference zone for r = 1.

Reference zone (i)	Range in Figs. 4.6a and 4.7a	VSI_1 operation	VSI_2 operation
1	0 to $1/(r + 1)$	low-side PWM	holds V_{dc2}
2	$1/(r + 1)$ to $1/2 \cdot r/(r + 1)$	low-side PWM	PWM
3	$1/2 \cdot r/(r + 1)$ to $1 - 1/2 \cdot r/(r + 1)$	low-side PWM	holds 0
4	$1 - 1/2 \cdot r/(r + 1)$ to 1	high-side PWM	holds 0

With $1 < r < 2$ the same topology operates as a six-level drive. Switching states in state machine form for this case are given in Table 4.8, while relevant Karnaugh maps are given in Tables 4.9, 4.10 and 4.11. The relationships between A_{ik} and the switching states are as follows:

$$\begin{aligned} S_{1k}^{a} &= A_{5k} + \overline{A}_{4k} \cdot A_{3k} \\ S_{1k}^{b} &= A_{3k} + \overline{A}_{2k} \cdot A_{1k} \\ S_{2k} &= \overline{A}_{4k} \cdot A_{3k} + \overline{A}_{2k} \end{aligned} \tag{4.4}$$

Only six out of 36 A_{ik} combinations are possible. The drive performs simultaneous switching in reference zones 2, 3 and 4, which means that dead-time spikes are more frequent. It follows that the additional voltage level will not lead to lower harmonic distortion of the produced waveforms, since the impact of the dead-time low-order current harmonics is increased, especially for lower modulation index values.

Table 4.8. CB PWM for 3L-OeW-2L six-level configuration ($1 < r < 2$) in state machine form.

Inputs					Resulting voltages			Resulting switching states		
A_{1k}	A_{2k}	A_{3k}	A_{4k}	A_{5k}	v_k	v_{1k}	v_{2k}	S_{1k}^{a}	S_{1k}^{b}	S_{2k}
0	0	0	0	0	$-V_{dc2}$	0	V_{dc2}	0	0	1
1	0	0	0	0	$V_{dc1}/2 - V_{dc2}$	$V_{dc1}/2$	V_{dc2}	0	1	1
1	1	0	0	0	$0 - 0$	0	0	0	0	0
1	1	1	0	0	$V_{dc1} - V_{dc2}$	V_{dc1}	V_{dc2}	1	1	1
1	1	1	1	0	$V_{dc1}/2$	$V_{dc1}/2$	0	0	1	0
1	1	1	1	1	V_{dc1}	V_{dc1}	0	1	1	0

Table 4.9. Karnaugh map for S_{1k}^{a} ($1 < r < 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	0	X	X	X
001	X	X	X	X
011	X	X	X	X
		X	X	X
		X	X	X
101	X	X	X	X
111	1	X	1	0
110	0	X	X	X

Table 4.10. Karnaugh map for S_{1k}^{b} ($1 < r < 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	0	X	X	X
001	X	X	X	X
011	X	X	X	X
010	X	X	X	X
100	1	X	X	X
101	X	X	X	X
111	1	X	1	1
110	0	X	X	X

Table 4.11. Karnaugh map for S_{2k} ($1 < r < 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	1	X	X	X
001	X	X	X	X
011	X	X	X	X
010	X	X	X	X
100	1	X	X	X
101	X	X	X	X
111	1	X	0	0
110	0	X	X	X

Table 4.12. Operation of two VSIs vs. reference zone for $1 < r < 2$.

Reference zone (i)	Range in Figs. 4.6b and 4.7b	VSI_1 operation	VSI_2 operation
1	0 to $1/(r+1)$	low-side PWM	holds V_{dc2}
2	$1/(r+1)$ to $1/2{\cdot}r/(r+1)$	low-side PWM	PWM
3	$1/2{\cdot}r/(r+1)$ to $1-1/2{\cdot}r/(r+1)$	rail-to-rail PWM	PWM
4	$1-1/2{\cdot}r/(r+1)$ to $r/(r+1)$	high-side PWM	PWM
5	$r/(r+1)$ to 1	high-side PWM	holds 0

With $r = 2$, the 3L-OeW-2L topology is capable of producing only four voltage levels, since four out of eight combinations in Table 4.2 are feasible. Using the same overall dc-link voltage of $V_{dc} = 600$ V as in Chapter 3, results in $V_{dc1} = 400$ V and $V_{dc2} = 200$ V and voltage levels of –200 V, 0 V, 200 V and 400 V, with respect to v_{n1} in the equivalent model (Fig. 4.2). Carrier arrangements for this special case are shown in Figs. 4.6c and 4.7c. In this case, v_{mp} is equal to V_{dc2}, which means that several switching combination will result in the same equivalent voltage level, as summarised in the Table 4.13. Due to the lower number of carrier signals and reduced complexity of the inverters' operation, Karnaugh maps (Tables 4.14, 4.15 and 4.16) result in much simpler final expressions for the switching states:

$$\begin{aligned} S_{1k}^{a} &= A_{3k} \\ S_{1k}^{b} &= A_{1k} \\ S_{2k} &= \overline{A}_{2k} \end{aligned} \tag{4.5}$$

Clearly, two inverters never operate in PWM mode at the same time, as shown in Table 4.17, meaning that simultaneous switching and dead-time spikes do not exist in this drive configuration. Also, PWM operation between 0 and $V_{dc1}/2$ and $V_{dc1}/2$ and V_{dc1} is symmetrical, due to symmetry that comes from expressions for S_{1k}^{a} and S_{1k}^{b}.

Table 4.13. CB PWM for 3L-OeW-2L four-level configuration ($r = 2$) in state machine form.

Inputs			Resulting voltages			Required switching states (outputs)		
A_{1k}	A_{2k}	A_{3k}	v_k	v_{1k}	v_{2k}	S_{1k}^{a}	S_{1k}^{b}	S_{2k}
0	0	0	$-V_{dc2}$	0	V_{dc2}	0	0	1
1	0	0	$V_{dc1}/2 - V_{dc2}$ (0 – 0)	0	V_{dc2} (0)	0 (0)	1 (0)	1 (0)
1	1	0	$V_{dc1}/2 - 0$ ($V_{dc1} - V_{dc2}$)	$V_{dc1}/2$ (V_{dc1})	0 (V_{dc2})	0 (1)	1 (1)	0 (1)
1	1	1	V_{dc1}	V_{dc1}	0	1	1	0

Table 4.14. Karnaugh map for S_{1k}^{a} ($r = 2$).

A_{1k} \ A_{2k} A_{3k}	0 0	0 1	1 1	1 0
0	0	X	X	X
1	0	X	1	0

Table 4.15. Karnaugh map for S_{1k}^{b} ($r = 2$).

A_{1k} \ A_{2k} A_{3k}	0 0	0 1	1 1	1 0
0	0	X	X	X
1	1	X	1	1

Table 4.16. Karnaugh map for S_{2k} ($r = 2$).

A_{1k} \ A_{2k} A_{3k}	0 0	0 1	1 1	1 0
0	0	X	X	X
1	0	X	1	1

Table 4.17. Operation of two VSIs vs. reference zone for $r = 2$.

Reference zone (i)	Range in Figs. 4.6c and 4.7c	VSI_1 operation	VSI_2 operation
1	0 to $1/(r+1)$	PWM	holds V_{dc2}
2	$1/(r+1)$ to $r/(r+1)$	holds $V_{dc1}/2$	PWM
3	$r/(r+1)$ to 1	PWM	holds 0

In contrast to the previously presented six-level operation for $r > 2$, (Figs. 4.6d and 4.7d), v_{mp} is greater than V_{dc2}. Switching states are summarised in Table 4.18. Again, only six out of 32 A_{ik} combinations are possible. However, due to differences in inner voltage levels formation (Fig. 4.3b) the switching pattern is different, resulting in symmetrical VSI_1 low- and high-side PWM operation. This is clear from the final expressions for switching states, which are derived using Karnaugh maps in Tables 4.19, 4.20 and 4.21:

$$\begin{aligned} S_{1k}^{a} &= A_{4k} \\ S_{1k}^{b} &= A_{2k} \\ S_{2k} &= \overline{A}_{5k} \cdot A_{4k} + \overline{A}_{3k} \cdot A_{2k} + A_{1k} \end{aligned} \tag{4.6}$$

The inverters operate simultaneously in PWM mode only in reference zones 2 and 4, Table 4.22. In this case V_{dc} = 600 V results in V_{dc1} = 480 V, V_{dc2} = 120 V, and voltage levels of –120 V, 0 V, 120 V, 240 V, 360 V and 480 V with respect to v_{n1}.

Table 4.18. CB PWM for 3L-OeW-2L six-level configuration ($r > 2$) in state machine form.

Inputs					Resulting voltages			Resulting switching states		
A_{1k}	A_{2k}	A_{3k}	A_{4k}	A_{5k}	v_k	v_{1k}	v_{2k}	S_{1k}^{a}	S_{1k}^{b}	S_{2k}
0	0	0	0	0	$-V_{dc2}$	0	V_{dc2}	0	0	1
1	0	0	0	0	0 – 0	0	0	0	0	0
1	1	0	0	0	$V_{dc1}/2 - V_{dc2}$	$V_{dc1}/2$	V_{dc2}	0	1	1
1	1	1	0	0	$V_{dc1}/2$	$V_{dc1}/2$	0	0	1	0
1	1	1	1	0	$V_{dc1} - V_{dc2}$	V_{dc1}	V_{dc2}	1	1	1
1	1	1	1	1	V_{dc1}	V_{dc1}	0	1	1	0

Table 4.19. Karnaugh map for S_{1k}^{a} ($r > 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	0	X	X	X
001	X	X	X	X
011	X	X	X	X
010	X	X	X	X
100	0	X	X	X
101	X	X	X	X
111	0	X	1	1
110	0	X	X	X

Table 4.20. Karnaugh map for S_{1k}^{b} ($r > 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	0	X	X	X
001	X	X	X	X
011	X	X	X	X
010	X	X	X	X
100	0	X	X	X
101	X	X	X	X
111	1	X	1	1
110	1	X	X	X

Table 4.21. Karnaugh map for S_{2k} ($r > 2$).

$A_{1k}\,A_{2k}\,A_{3k}$ \ $A_{4k}\,A_{5k}$	0 0	0 1	1 1	1 0
000	1	X	X	X
001	X	X	X	X
011	X	X	X	X
010	X	X	X	X
100	0	X	X	X
101	X	X	X	X
111	0	X	0	1
110	1	X	X	X

Table 4.22. Operation of the VSIs vs. reference zone for $r > 2$.

Reference zone (i)	Range in Figs. 4.6b and 4.7d	VSI_1 operation	VSI_2 operation
1	0 to $1/(r + 1)$	holds 0	PWM
2	$1/(r + 1)$ to $1/2 \cdot r/(r + 1)$	PWM	PWM
3	$1/2 \cdot r/(r + 1)$ to $1 - 1/2 \cdot r/(r + 1)$	holds $V_{dc1}/2$	PWM
4	$1 - 1/2 \cdot r/(r + 1)$ to $r/(r + 1)$	PWM	PWM
5	$r/(r + 1)$ to 1	holds V_{dc1}	PWM

4.3.3. SIMULATION RESULTS

Simulation results are shown in Figs. 4.8-4.10 for conventional PD and APOD PWM. Both five- and six-level operation suffer from dead-time spikes. With $r = 1$, spikes are only present in the reference zone 2, while $r = 4$ results in dead-time spikes in zones 2 and 4. From shown cases, only four-level configuration ($r = 2$) is completely free from dead-time spikes, since in this case the inverters never simultaneously operate in PWM mode.

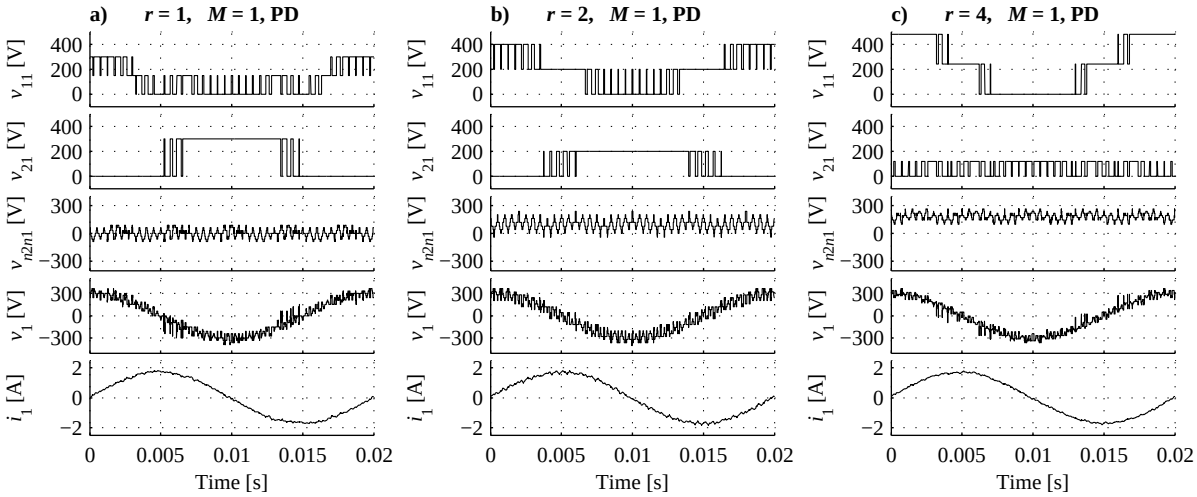


Fig. 4.8. Simulation results: conventional PD PWM for $M = 1$ and $r = 1$ (a), $r = 2$ (b), $r = 4$ (c).

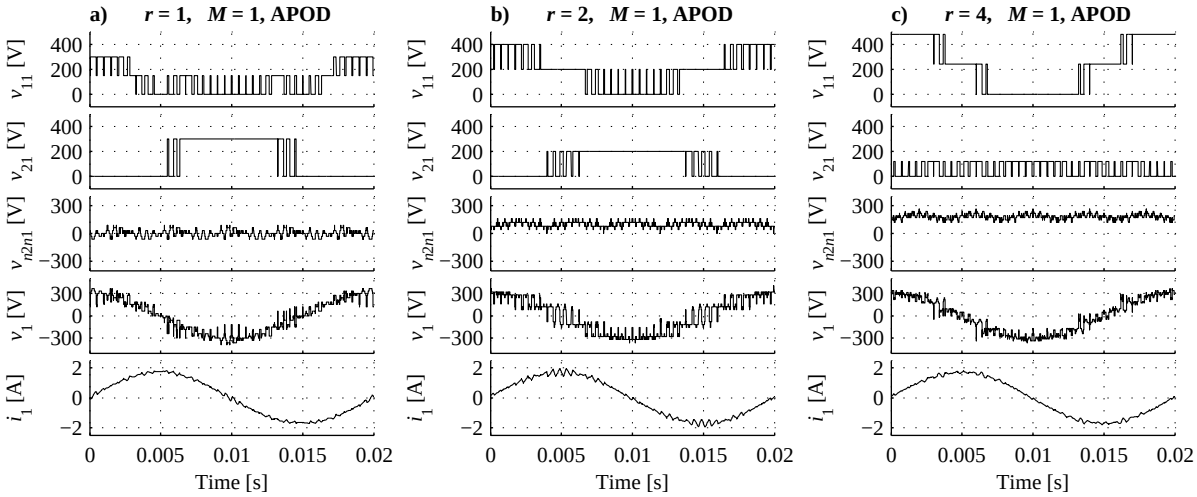


Fig. 4.9. Simulation results: conventional APOD PWM for $M = 1$ and $r = 1$ (a), $r = 2$ (b), $r = 4$ (c).

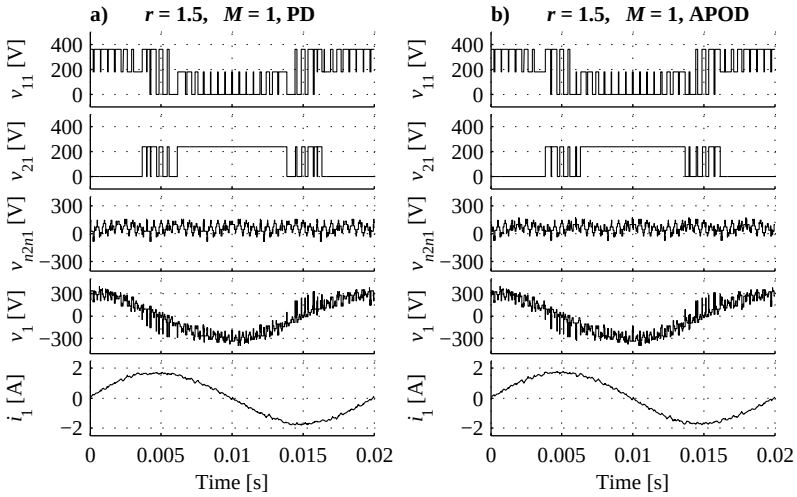


Fig. 4.10. Simulation results: six-level operation with PD PWM (a) and APOD PWM (b) for $M = 1$ and $r = 1.5$.

Comparison of these waveforms with those produced by a 2L-OeW-2L drive with the same dc-link voltage ratios shows that dead-time spike issue is less relevant for 3L-OeW-2L topology, since the magnitude of the spikes is several times smaller. Hence, their influence on current low-order harmonics is also reduced. Proposed PWM scheme modifications that lead to dead-time spike elimination (SAR and SRA) can be applied here as explained in the next subsection. As already explained, the 3L-OeW-2L topology is capable of operating in six-level mode with two different configurations, with $r < 2$ and $r > 2$. Simulation results for $r = 1.5$ are depicted in Fig. 4.10 for both PD and APOD PWM and $M = 1$. Clearly, dead-time spikes are more frequent when compared with six-level operation in Figs. 4.8c and 4.9c, resulting in worse harmonic performance. Hence, for six-level operation $r > 2$ seems to be more suitable than $1 < r < 2$.

4.3.4. DEAD-TIME SPIKES

As already explained, only one of the presented configurations ($r = 2$) does not suffer from dead-time spikes issue. Hence, straightforward implementation of the algorithm given with equation (4.5) can be used in this case, as shown in block diagram in Fig. 4.11.

In all other cases, one has to apply SRA on conventional PD and APOD PWM schemes, in order to achieve expected drive harmonic performance. When combined with SAR, this again leads to complete elimination of the dead-time spikes throughout the modulation index range. The same approach, presented in subsection 3.3.5 can be used for the 3L-OeW-2L drive, and so only the final expressions for Δv are given, for different cases, in Table 4.23. Final calculations of Δv_{1k} and Δv_{2k} based on the phase current sign and switching instant during one switching period remains the same as for the 2L-OeW-2L drive. The values are used in block diagrams in Figs. 4.12 and 4.13 where final CB PWM algorithms are shown for five- and six-level configurations. SRA algorithm for six-level operation with $1< r < 2$ is somewhat more complex than for the other cases, since one has to apply different Δv values in different reference zones. In zones 2 and 4, value Δv' should be used, while Δv" should be applied in the reference zone 3. This is because of the differences in voltage level formation, since simultaneous switching in reference zone 3 requires VSI_1 PWM operation between V_{dc1} and 0 (i.e. v_{mp} is not used) in order to utilise PWM between $V_{dc1} - V_{dc2}$ and $0 - 0$ equivalent voltage levels. This makes SRA implementation difficult, due to increased number of switching transitions that have to be synchronised, while SAR operation is not practical as already explained. Hence, this kind of six-level configuration is not experimentally verified. Additionally, SAR implementation is considered as well, but only for the five-level configuration, since other two configurations naturally employ VSI_2 only, for $M < M_{max}/(r + 1)$.

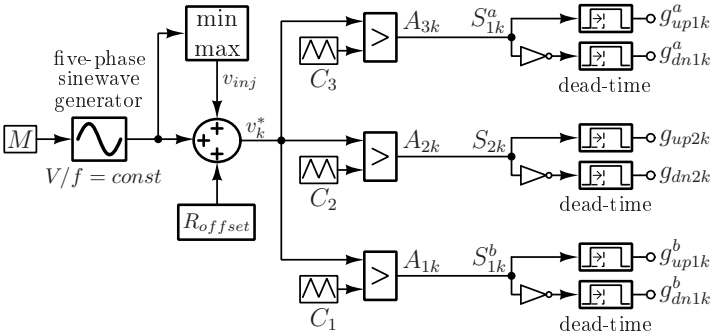


Fig. 4.11. Coupled CB PWM algorithm for the four-level configuration with the 3L-OeW-2L drive (r = 2).

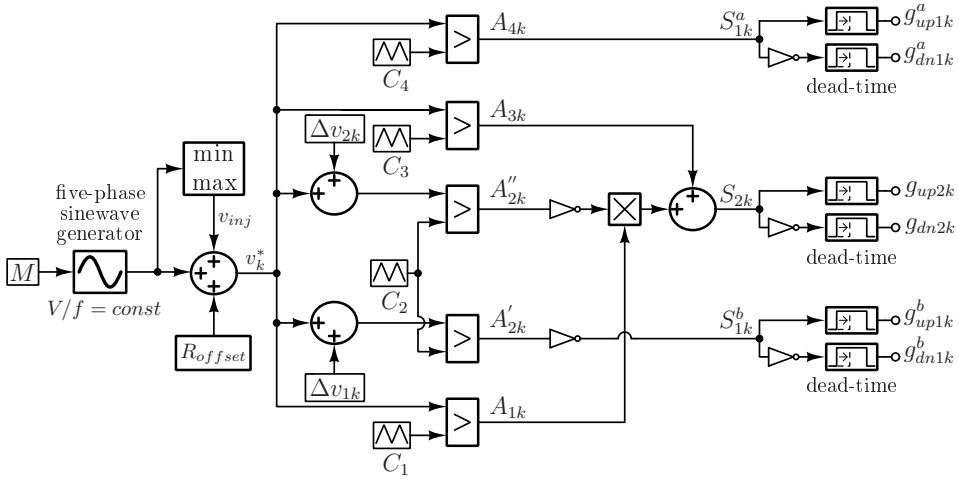


Fig. 4.12. Coupled CB PWM algorithm for the five-level configuration with the 3L-OeW-2L drive (r = 1).

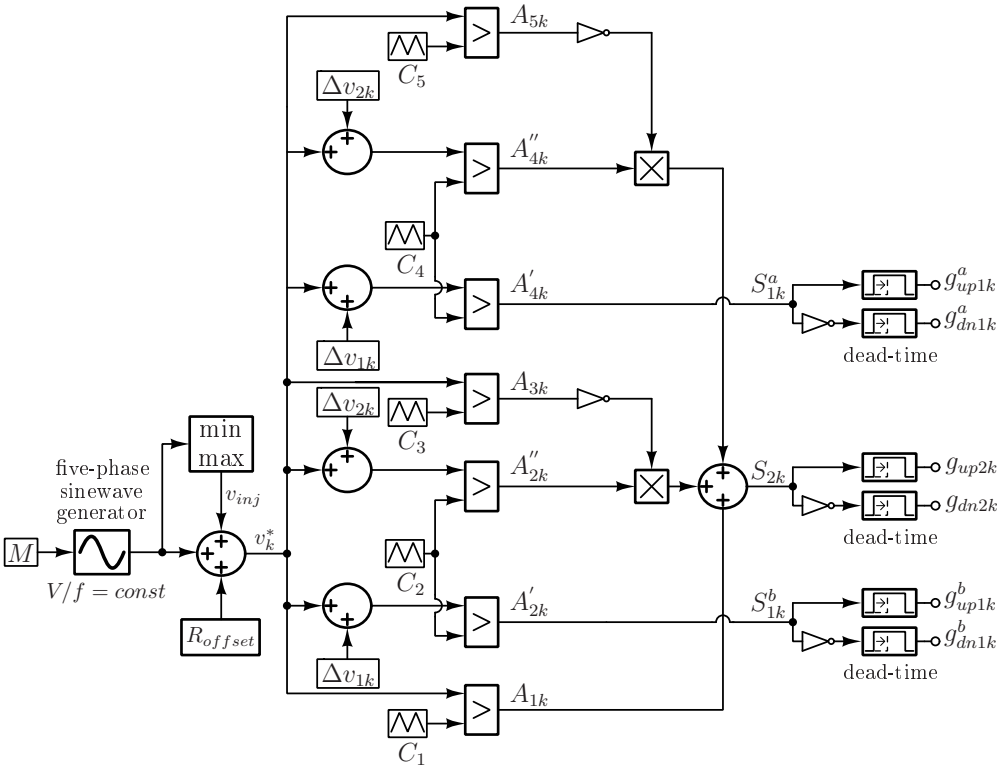


Fig. 4.13. Coupled CB PWM algorithm for the six-level configuration with the 3L-OeW-2L drive (r > 2).

Table 4.23. Operation of two VSIs vs. reference zone for $r > 2$.

The dc-link voltage ratio	Affected reference zones	Reference offset for dead-time spikes elimination	
$r = 1$	2	$\Delta v = 2\cdot(1 - r/2)/(r + 1)$	
$1 < r < 2$	2, 3, 4	$\Delta v' = 2\cdot(1 - r/2)/(r + 1)$	$\Delta v'' = 2\cdot(r - 1)/(r + 1)$
$r > 2$	2, 4	$\Delta v = 2\cdot(r/2 - 1)/(r + 1)$	

4.3.5. INFLUENCE OF THE DC-LINK VOLTAGE RATIO ON DRIVE HARMONIC PERFORMANCE

In the previous analysis, it was shown that the 3L-OeW-2L drive should not be used with $1 < r < 2$ for six-level configuration, since the same number of voltage levels can be obtained with $r > 2$, where unwanted effects caused by inevitable simultaneous switching are easier to eliminate. However, in order to find the most suitable dc-link voltage ratio, one has to analyse the other cases as well, and to compare harmonic performance obtained with different configurations. Firstly, this is done using numerical simulations. In Fig. 4.14 THD(M) dependencies are plotted for PD and APOD PWM, for several values of r. Clearly, SAR and SRA implementation lead to a great reduction of harmonic distortion, especially in the case of the five-level ($r = 1$) configuration with APOD PWM. In general, expectations that increased number of voltage levels will lead to lower THD are fulfilled only if SAR and SRA are used. A six-level configuration obtained using $r = 3$ results in higher harmonic distortion than $r = 4$. Three different configurations are chosen for further analysis: four-level ($r = 2$), five-level ($r = 1$) and six-level ($r = 4$).

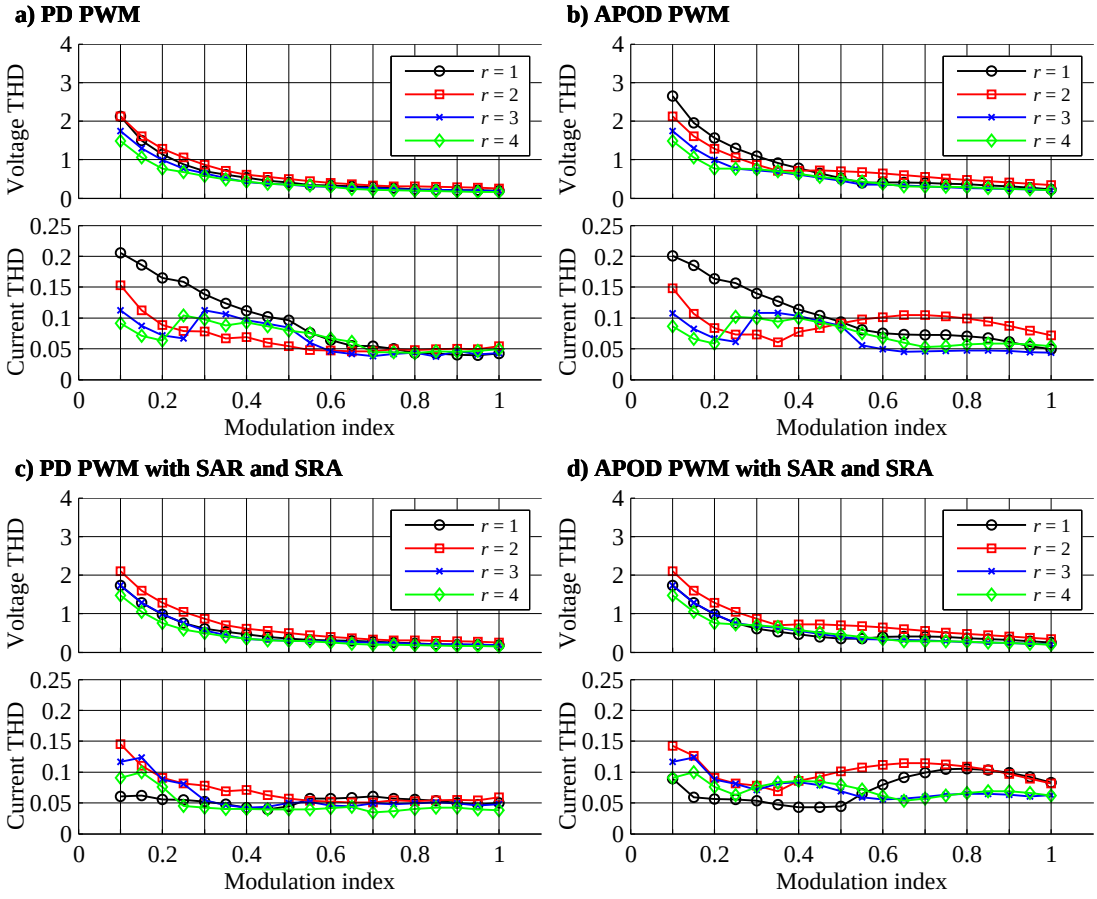
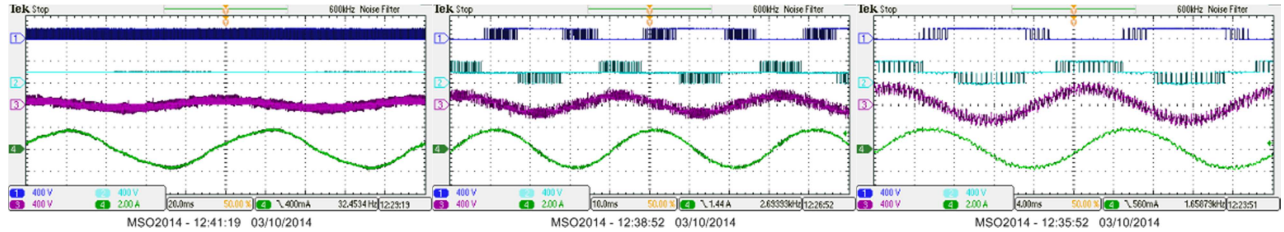


Fig. 4.14. Simulation results: phase voltage and phase current THD(M) for conventional PD and APOD (a, b) and with SAR and SRA (c, d), with different dc-link voltage ratios.

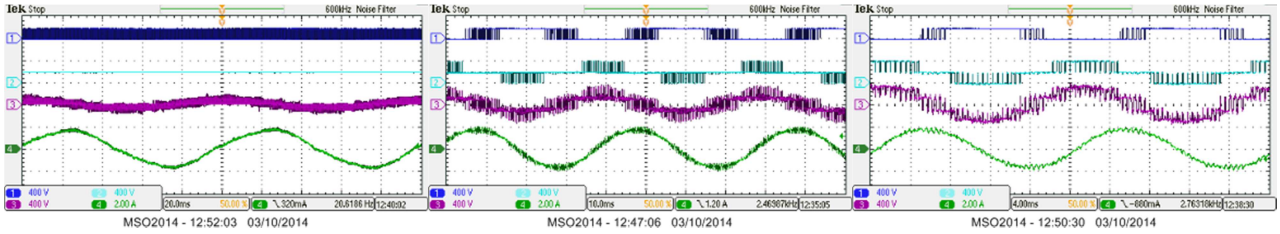
4.3.6. EXPERIMENTAL RESULTS FOR THE FOUR-LEVEL CONFIGURATION

Experimentally obtained waveforms for the 3L-OeW-2L drive with $r = 2$ in Figs. 4.15 and 4.16 show v_{21} (CH1), v_{11} (CH2), v_1 (CH3) and i_1 (CH4) for three modulation index values. Both modulation strategies naturally employ only VSI_2 for $M < 0.35$, while VSI_1 in this case (see Figs. 4.15a and 4.16a) holds all its leg voltages at the v_{mp} voltage level. In the rest of the modulation index range, four-level operation takes place. Contrary to the 2L-OeW-2L case, the inverters never operate at the same time, which eliminates any need for SRA implementation. Operation of VSI_1 in low- and high-side is symmetrical, meaning that there is no need for additional capacitor voltage balancing, which is a known issue for NPC converters. Comparison of obtained spectra and THD(M), shown in Figs. 4.17 - 4.19 with the results reported in Chapter 3 (Figs. 3.30 - 3.34), shows that both modulation strategies have the same performance as their counterparts with SAR and SRA in the case of 2L-OeW-2L drive with $r = 2$.



a) b) c)

Fig. 4.15. Experimental results: PD PWM waveforms for $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 4.16. Experimental results: APOD PWM waveforms for $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

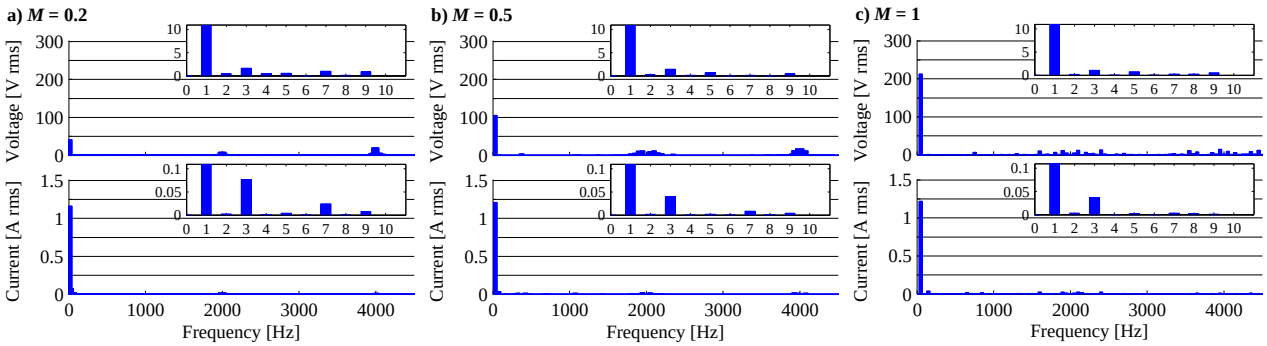


Fig. 4.17. Experimental results: PD PWM v_1 and i_1 spectra for $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

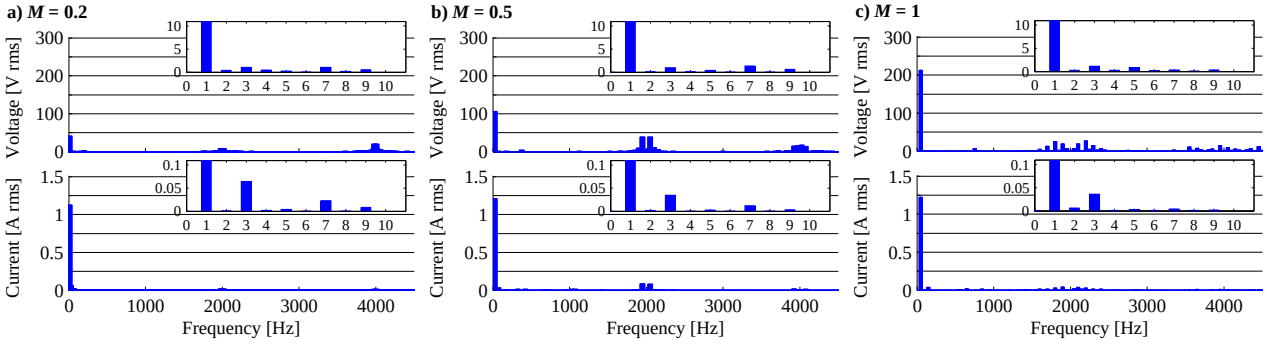


Fig. 4.18. Experimental results: APOD PWM v_1 and i_1 spectra for $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

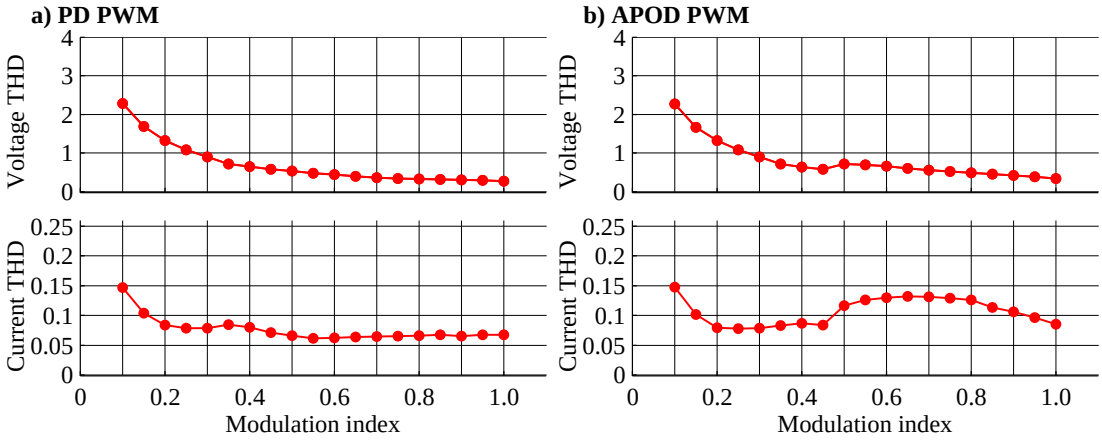
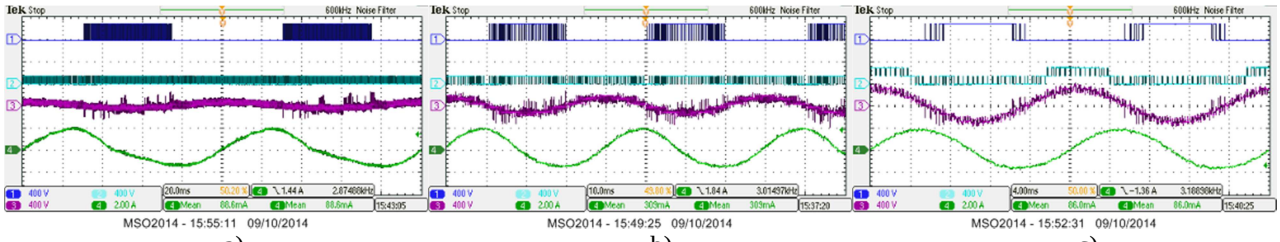


Fig. 4.19. Experimental results: phase voltage and phase current THD(*M*) for PD (a) and APOD (b) for *r* = 2.

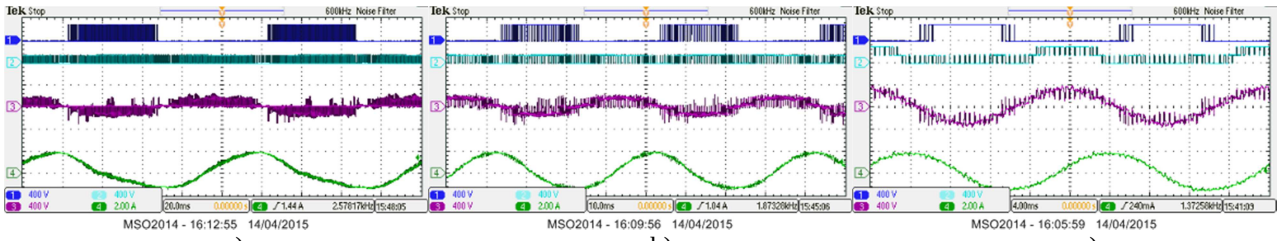
4.3.7. EXPERIMENTAL RESULTS FOR THE FIVE-LEVEL CONFIGURATION

With *r* = 1, the 3L-OeW-2L drive operates in five-level configuration. Recorded waveforms are shown in Figs. 4.20 and 4.21 for conventional PD and APOD PWM. The results show that when $M < 0.525$ there is asymmetrical operation of VSI_1, since only low-side PWM is performed. At the same time, VSI_2 operates during only one half of the fundamental period when the reference is in the zone 2. This leads to simultaneous switching, i.e. dead-time spikes and increased energy losses, making SAR implementation necessary. Figs. 4.22 and 4.23 show results with SRA and SAR implementation for PD PWM and APOD PWM, respectively. For $M > 0.525$, the drive operates in the full five-level mode, but again with asymmetrical low- and high-side operation of VSI_1. The influence of this phenomenon will be analysed in detail in the next chapter, together with other issues related to capacitor balancing in OeW drives. Regarding the harmonic performance (Figs. 4.24 - 4.27), it is clear that conventional CB PWM suffers from dead-time spikes leading to third and seventh current harmonics. This is a direct consequence of the dead-time spikes, which are causing higher harmonic distortion when compared to a four-level configuration with 2L-OeW-2L drive and *r* = 2.



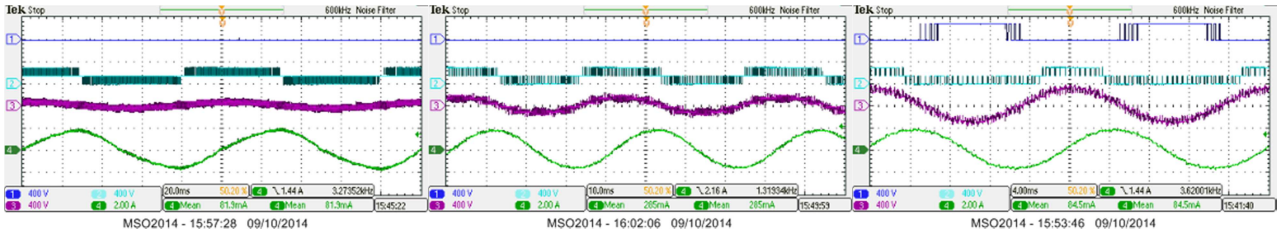
a) b) c)

Fig. 4.20. Experimental results: PD PWM waveforms for *r* = 1, with *M* = 0.2 (a), *M* = 0.5 (b), *M* = 1 (c).



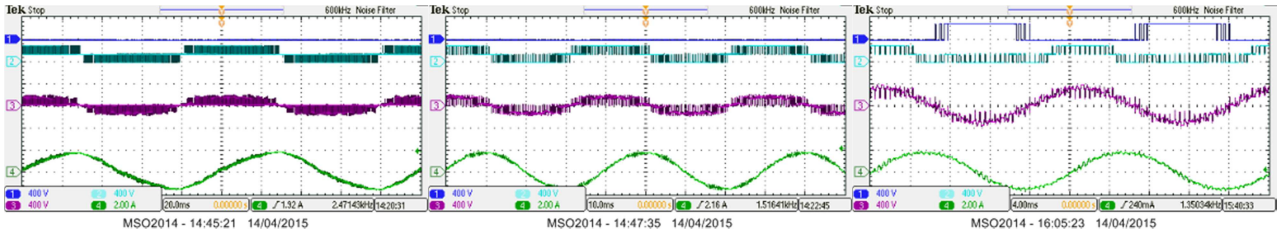
a) b) c)

Fig. 4.21. Experimental results: APOD PWM waveforms for *r* = 1, with *M* = 0.2 (a), *M* = 0.5 (b), *M* = 1 (c).



a) b) c)

Fig. 4.22. Experimental results: PD PWM with SAR/SRA waveforms for r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).



a) b) c)

Fig. 4.23. Experimental results: APOD PWM with SAR/SRA waveforms for r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

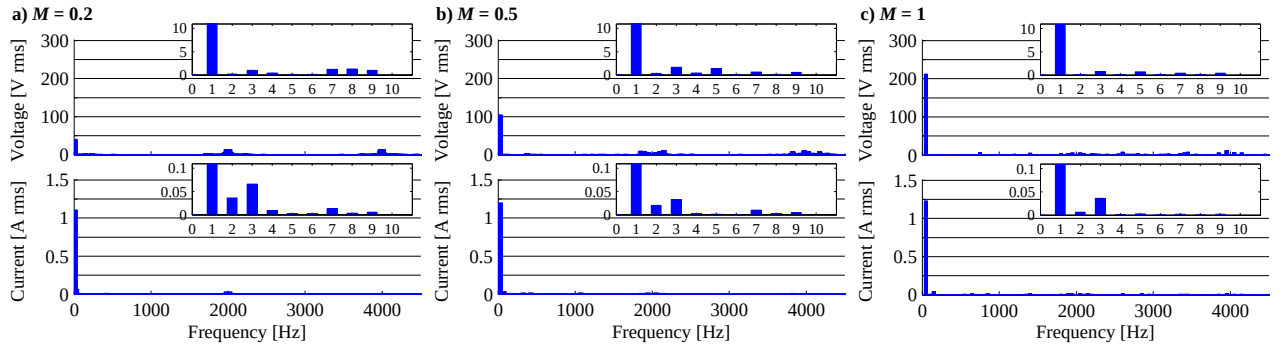


Fig. 4.24. Experimental results: PD PWM v_1 and i_1 spectra for r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

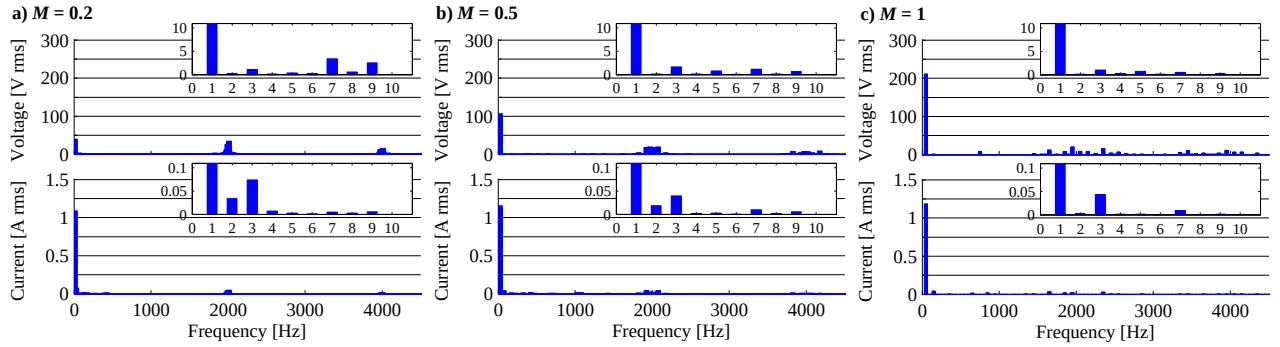


Fig. 4.25. Experimental results: APOD PWM v_1 and i_1 spectra for r = 1, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

Comparison of the results in Figs. 4.20 and 4.21, with those in Figs. 3.26 and 3.27, shows that spikes have lower amplitude in the case of 3L-OeW-2L drive, but also that their presence is asymmetrical. Hence, only one part of the current waveform is affected with additional ripple (see Figs. 3.12 and 3.18), which causes somewhat higher distortion. This asymmetry has no effect on the phase voltage THD, as can be concluded from Fig. 4.28, where THD(M) dependencies are shown. Since SAR is applied for M up to 0.525, THD(M) dependencies for both modulation strategies confirm that single-sided three level operation leads to great reduction of phase current harmonic content. As expected, due to lower amplitude of dead-time spikes, their influence on THD is lower, when compared to the case of 2L-OeW-2L four-level configuration. It can be also concluded that differences in harmonic performances of PD and APOD PWM are lower for the five-level operation (Fig. 4.28) than for four- (Figs. 4.19 and 3.34) or three-level (Fig. 3.25) operation.

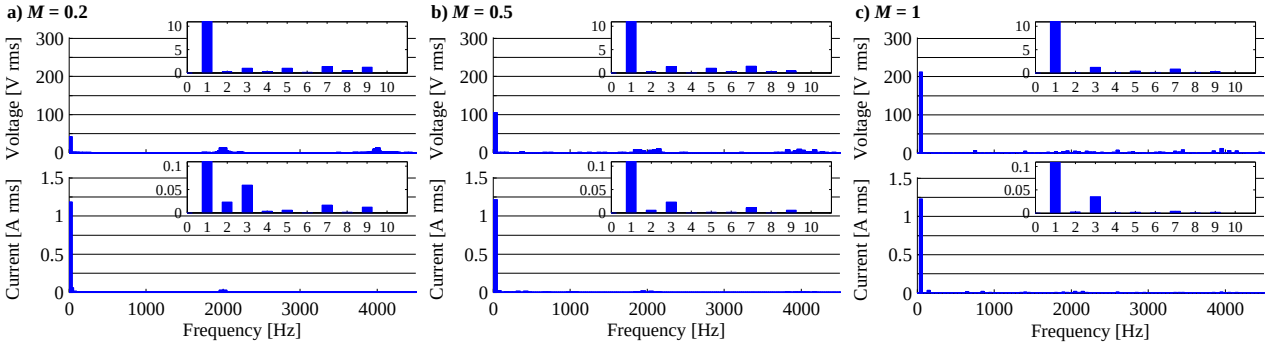


Fig. 4.26. Experimental results: PD PWM with SAR/SRA v_1 and i_1 spectra for $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

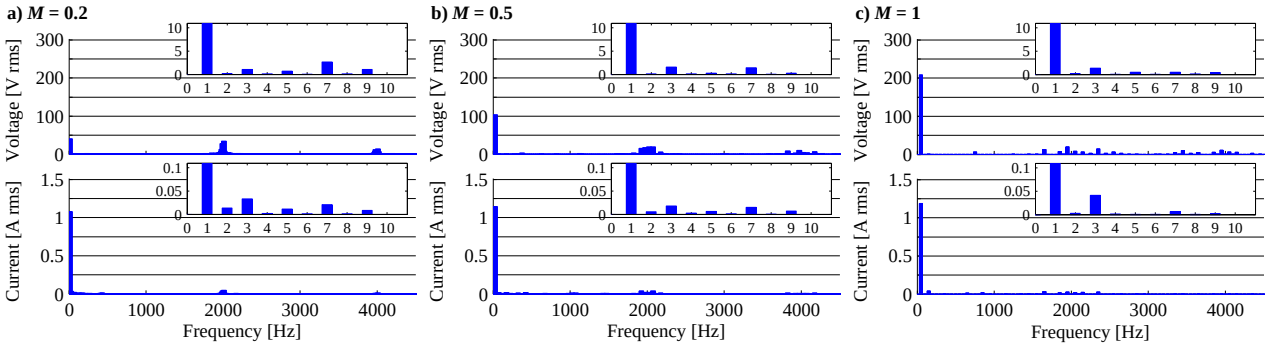


Fig. 4.27. Experimental results: APOD PWM with SAR/SRA v_1 and i_1 spectra for $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

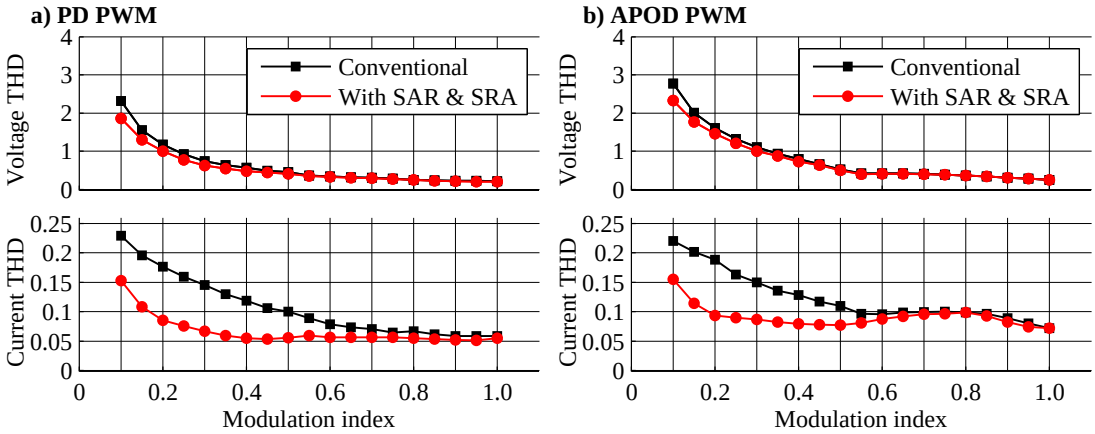
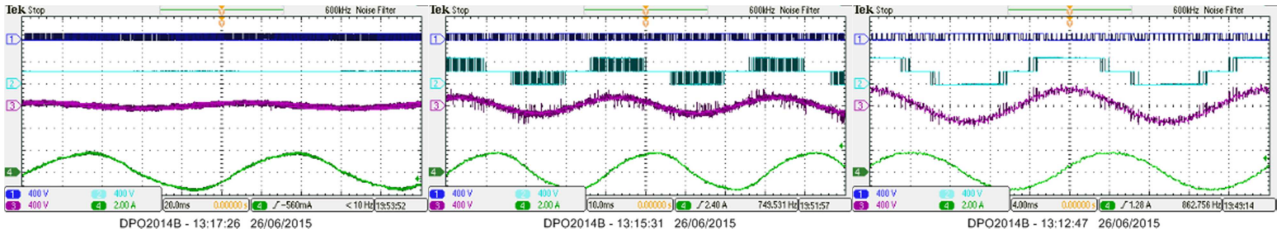


Fig. 4.28. Experimental results: phase voltage and phase current THD(M) for PD (a) and APOD (b) for $r = 1$.

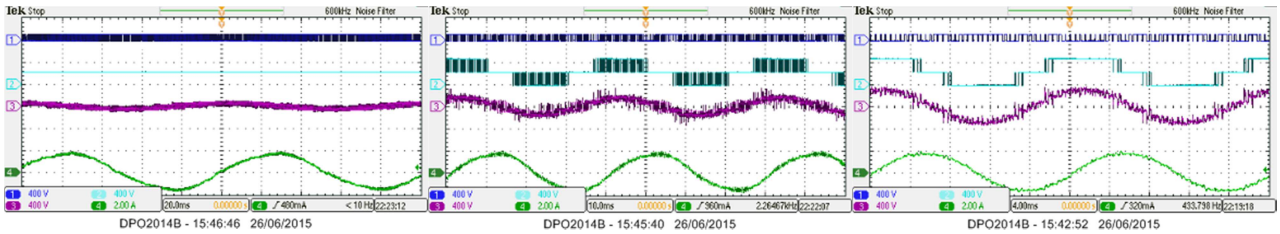
4.3.8. EXPERIMENTAL RESULTS FOR THE SIX-LEVEL CONFIGURATION

In this case ($r = 4$, $V_{dc1} = 480$ V, $V_{dc2} = 120$ V), two-level operation takes place when $M \leq 0.2$, which is performed using VSI_2 only, without any modulation scheme modification (SAR is not needed). For $0.2 < M \leq 0.4$, the drive operates in four-level mode, while all six voltage levels are used in the rest of the modulation index range. The low-side of VSI_1 operates in PWM mode when the phase voltage reference is in zone 2, while the high-side is in PWM mode in zone 4. VSI_2 operates in PWM mode in all reference zones, which means that SRA should be applied in zones 2 and 4. Obtained waveforms for conventional PD and APOD, shown in Figs. 4.29 and 4.30, confirm the existence of dead-time spikes in these two zones. Results for both PD PWM and APOD PWM with SRA are shown in Figs. 4.31 and 4.32, respectively.



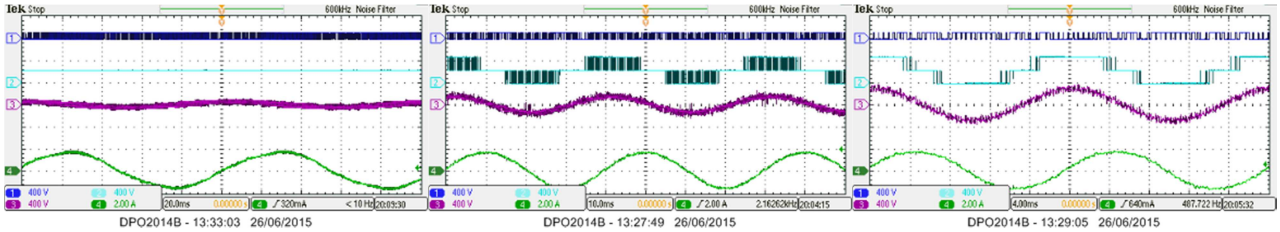
a) b) c)

Fig. 4.29. Experimental results: PD PWM waveforms for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



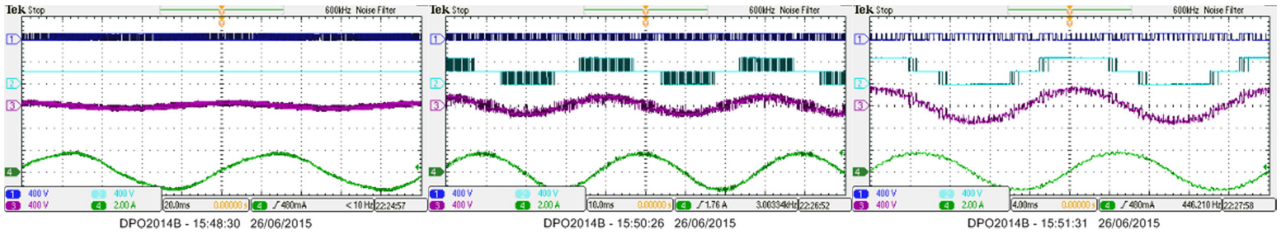
a) b) c)

Fig. 4.30. Experimental results. APOD PWM waveforms for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 4.31. Experimental results: PD PWM with SRA waveforms for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 4.32. Experimental results: APOD PWM with SRA waveforms for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

Due to the low precision of current sensors around current zero crossings, the phase current sign is not always correctly determined, which explains a few remaining spikes in Figs. 4.31b and 4.32b. Comparison of corresponding spectra in Figs. 4.33 - 4.36 shows that this has no influence on the overall improvement when SRA is applied, since low-order current harmonics are reduced despite the remaining spikes for $M = 0.5$. THD versus M dependencies are shown in Fig. 4.37. SRA implementation leads again to reduced harmonic distortion, especially for $0.2 < M < 0.4$ where dead-time spikes are the most frequent. Only for APOD around $M = 1$ SRA leads to somewhat higher current THD, which can be corrected using closed-loop current control. Voltage THD(M) is similar for schemes with and without SRA, mainly because of the high number of voltage levels, and lower dead-time spike amplitudes, when compared to the four-level operation with thes 2L-OeW-2L drive. For the same reasons, differences between harmonic performances of PD and APOD are also smaller than in the case of the drives with the lower number of voltage levels.

With the 2L-OeW-2L drive in three- and four-level configurations, APOD PWM resulted in much lower ripple in v_{n2n1} waveforms. Simulation results in Figs. 4.8b and 4.9b show that the 3L-OeW-2L CMV for $r = 2$ is the same as the 2L-OeW-2L drive in four-level configuration (Figs. 3.16 and 3.17). For configurations with higher number of voltage

levels, v_{n2n1} ac components amplitudes are vastly reduced, as is the differences between PD and APOD regarding CMV performance.

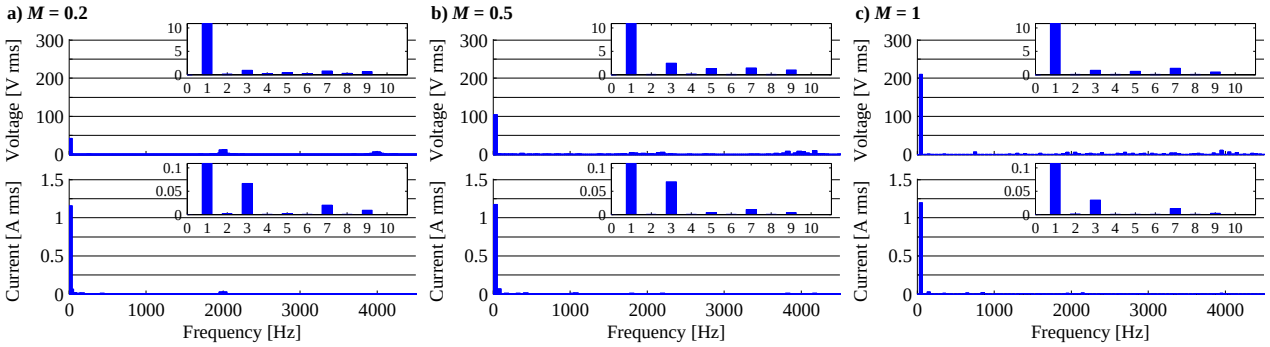


Fig. 4.33. Experimental results: PD PWM v_1 and i_1 spectra for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

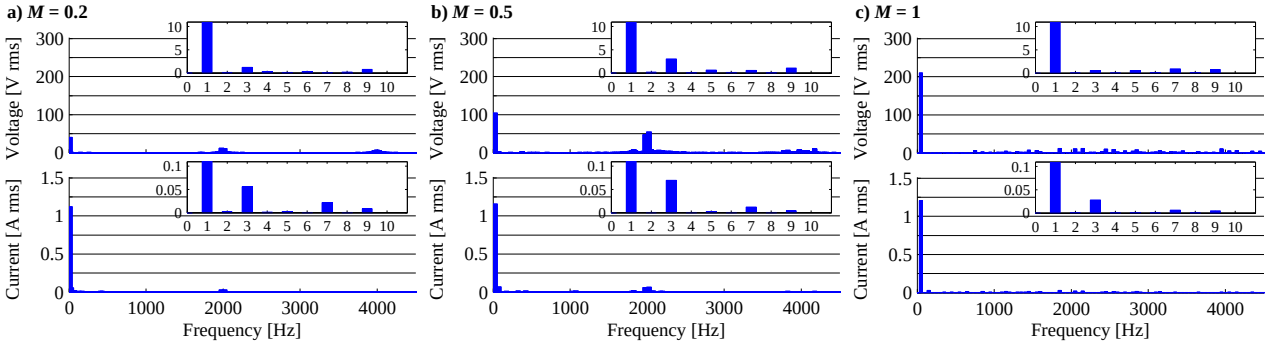


Fig. 4.34. Experimental results: APOD PWM v_1 and i_1 spectra for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

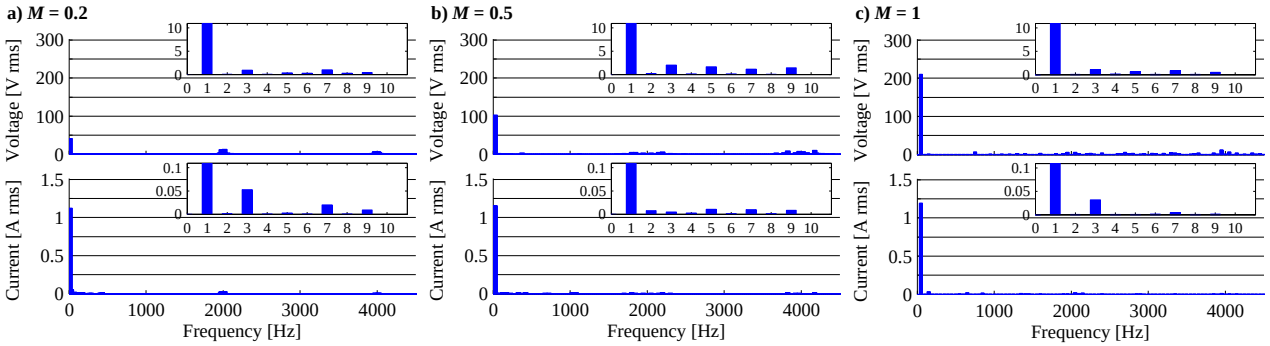


Fig. 4.35. Experimental results: PD PWM with SRA v_1 and i_1 spectra for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

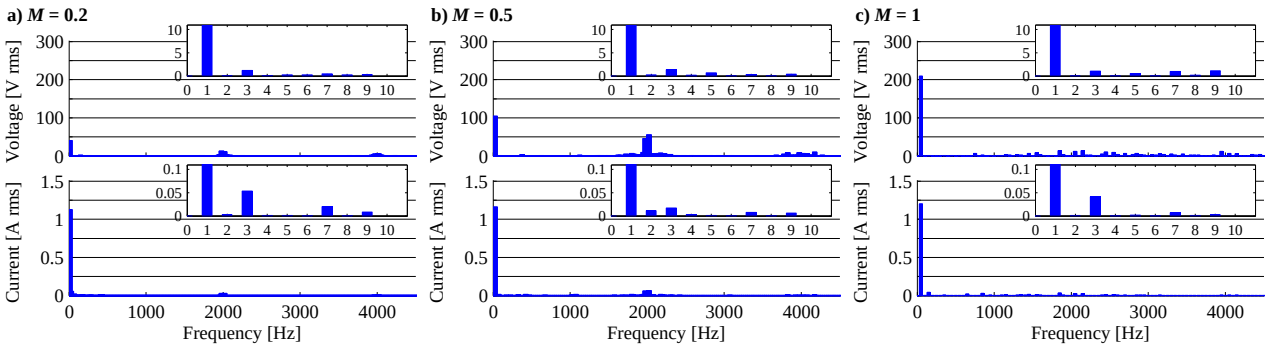


Fig. 4.36. Experimental results: APOD PWM with SRA v_1 and i_1 spectra for $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

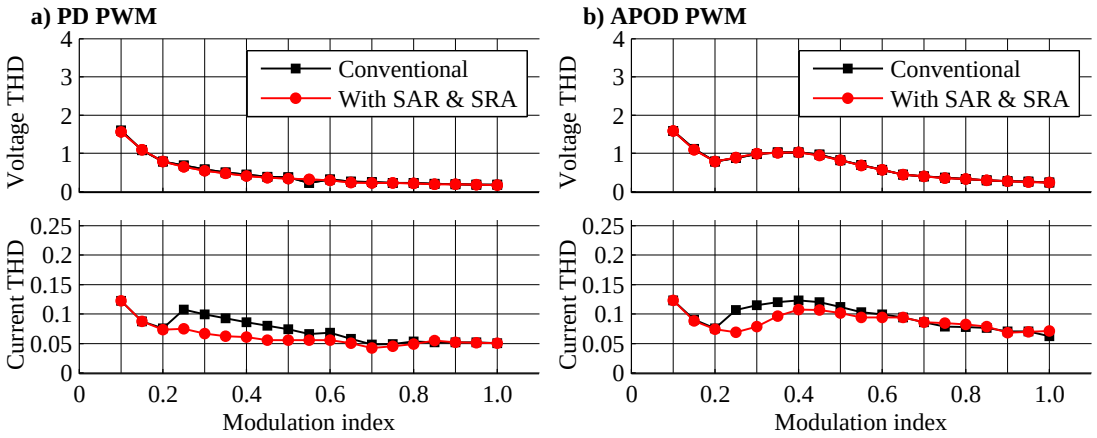


Fig. 4.37. Experimental results: phase voltage and phase current THD(*M*) for PD (a) and APOD (b) for *r* = 4.

4.4. DECOUPLED CARRIER BASED MODULATION METHODS

4.4.1. PRELIMINARY ANALYSIS

In this section, harmonic performances of URS1 and URS2 are investigated for the 3L-OeW-2L drive. Due to the algorithm simplicity, phase voltage reference sharing is performed in the same manner as for the 2L-OeW-2L drive, using equations (3.16) and (3.17). The final modulation scheme requires modifications at the VSI_1 side, since two carrier signals are needed for three-level operation of the NPC inverter. The final modulation scheme diagram is shown in Fig. 4.38, where VSI_1 carriers are denoted with C_{11} and C_{12}, while C_{21} stands for VSI_2 carrier signal. Alternatively, one may find that different carrier arrangments for VSI_1 can be used. Based on the findings from [Dordevic (2013)], C_{11} and C_{12} in-phase disposition are used for both URS strategies, since this configuration leads to the lowest harmonic distortion in the waveforms produced by the three-level inverter. Formation of the VSIs references is depicted in Fig. 4.39, for two different cases. Since URS1 and URS2 use only VSI_2 in PWM mode for modulation indices up to $M_{max}/(r+1)$, multilevel operation will take place over a wider range of *M* for higher values of *r*.

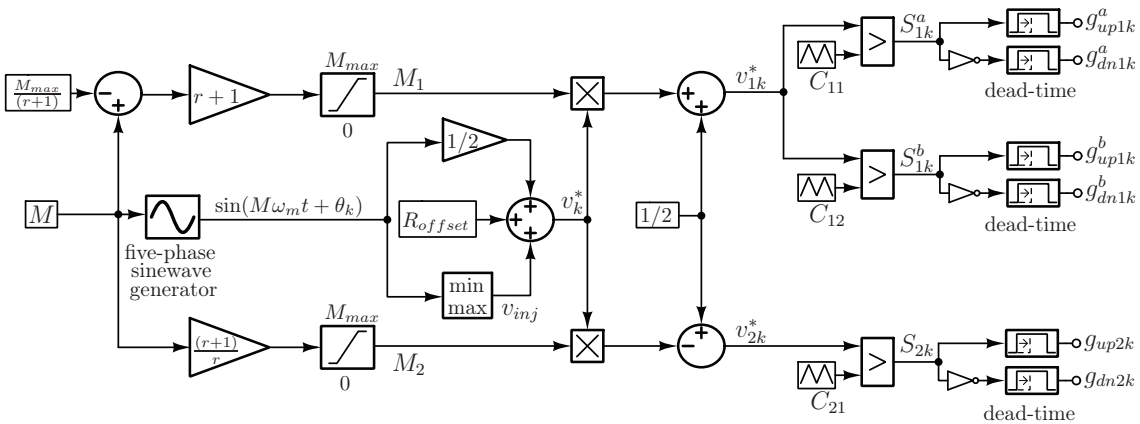


Fig. 4.38. Decoupled URS algorithm block diagram for the 3L-OeW-2L drive: The modulation scheme is based on (3.8) with R_{offset} = 0 for the initial phase voltage reference formation and (3.16) and (3.17) for obtaining final VSI_1 and VSI_2 references.

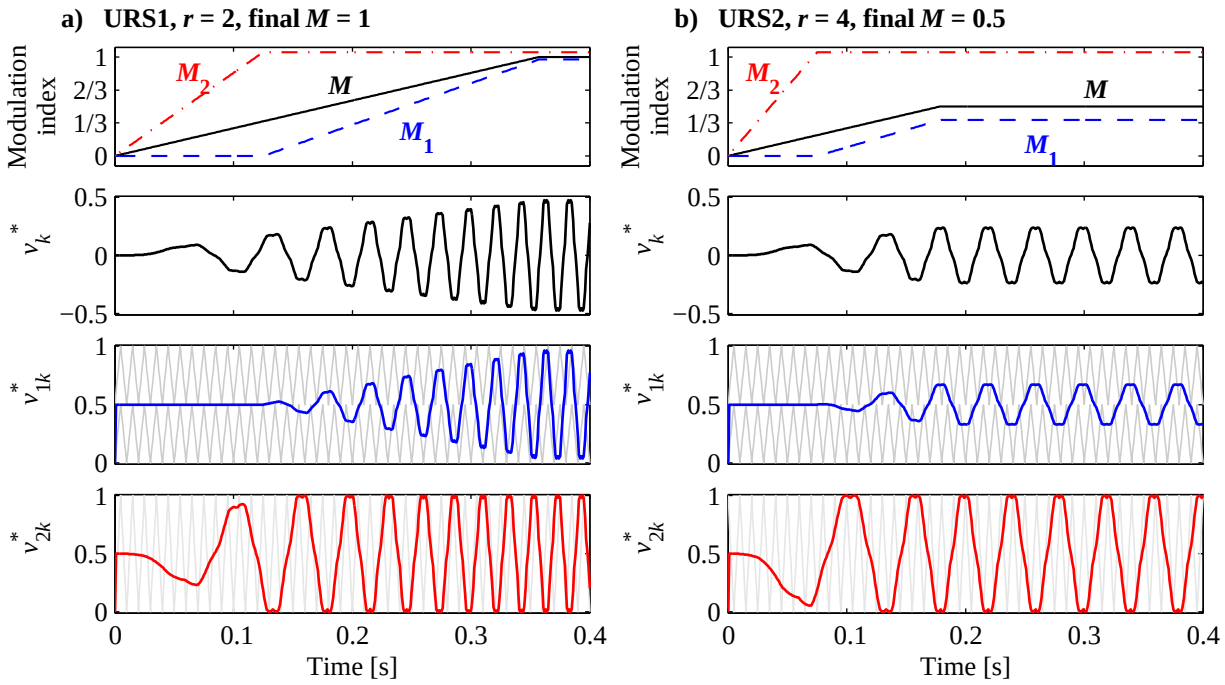


Fig. 4.39. Formation of the VSIs voltage references using algorithm in Fig. 4.38: *V/f* acceleration with URS1, $r = 2$ and final M value equal to 1 (a) and with URS2, $r = 4$ and final M value equal to 0.5 (b). Difference between URS1 and URS2 is only in carrier signal disposition (C_{11}, C_{12} and C_{21} frequencies are reduced to 100 Hz, for better visualisation).

4.4.2. SIMULATION RESULTS

Decoupled methods are firstly validated using numerical simulations and the parameters given in Appendix 1. Simulation results, shown in Figs. 4.40 and 4.41 for URS1 and URS2, confirm that the produced phase voltage waveforms are more sinusoidal than in the case of the 2L-OeW-2L drive, due to three-level operation of VSI_1. Similarly to the 2L-OeW-2L case, phase voltages do not contain dead-time spikes, while the output waveforms are less sinusoidal than those produced using the coupled PWM methods.

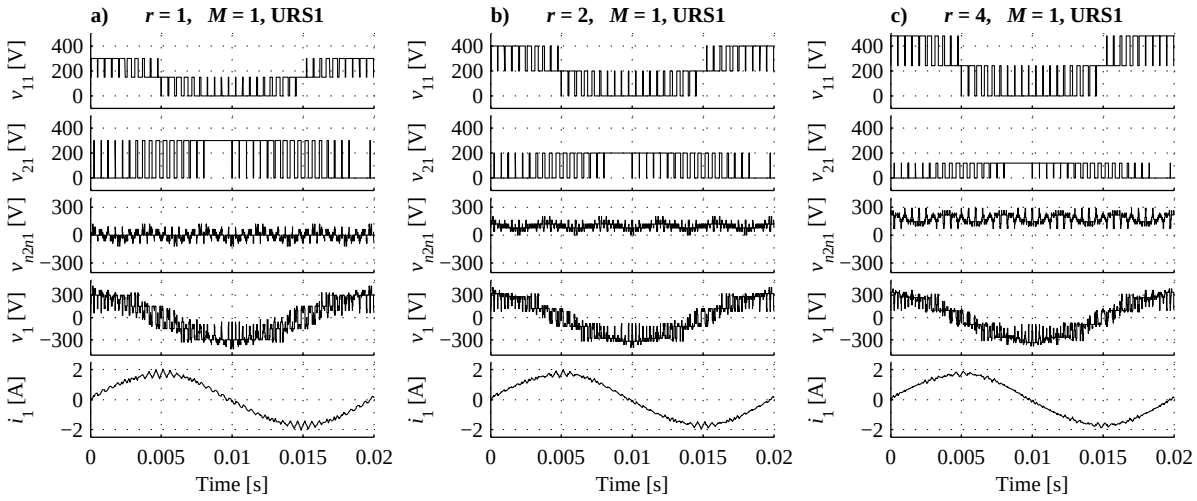


Fig. 4.40. Simulation results: URS1 waveforms for $M = 1$ and $r = 1$ (a), $r = 2$ (b) and $r = 4$ (c).

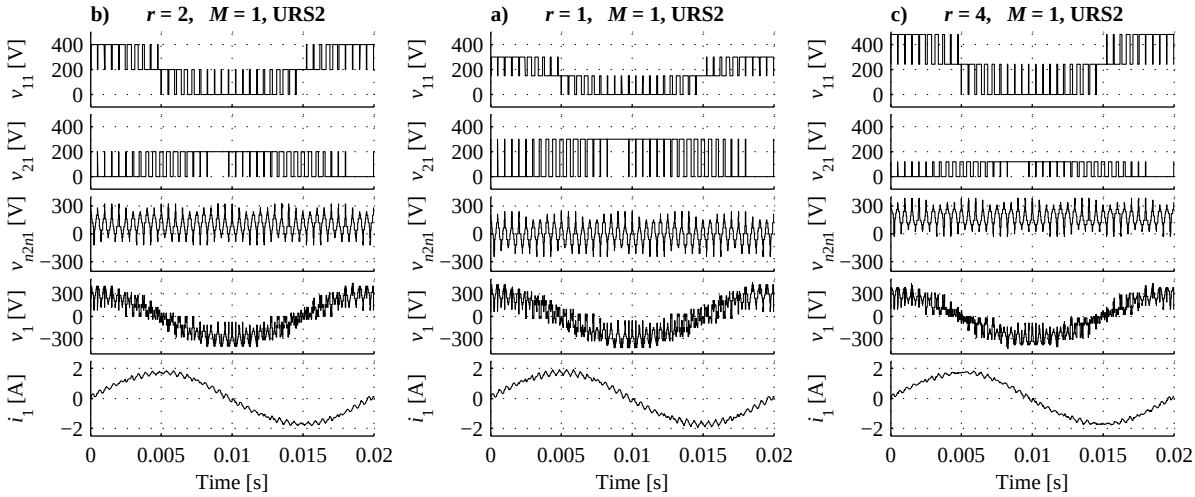


Fig. 4.41. Simulation results: URS2 waveforms for $M = 1$ and $r = 1$ (a), $r = 2$ (b) and $r = 4$ (c).

Analysis of the leg voltage waveforms shows that VSI_2 operates with pulse dropping, due to the dead-time effects. This effect is eliminated during experimental verification in the same manner as in Section 3.4, by reducing the maximal value of M_2 to 1.03. The phase current ripple is much lower in the case of URS1, especially for $r = 4$. This can be explained by the fact that $r = 4$ leads to the highest number of voltage levels among those shown in Fig. 4.40 and 4.41. Nevertheless, detailed analysis of harmonic performance is needed in order to find the optimal dc-link voltage ratio, which is the focus of the next section. CMV ac components are reduced, when compared to the 2L-OeW-2L drive with decoupled modulation schemes. URS1 is again superior, resulting in lower CMV ripple.

4.4.3. INFLUENCE OF THE DC-LINK VOLTAGE RATIO ON DRIVE HARMONIC PERFORMANCE

THD(M) dependencies, obtained by simulation, are shown in Fig. 4.42. Compared to the 2L-OeW-2L case (Fig. 3.39), current THD around the border between two-level and multilevel modes is lower, due to the increased number of levels of VSI_1. Higher values of r result in lower harmonic distortion.

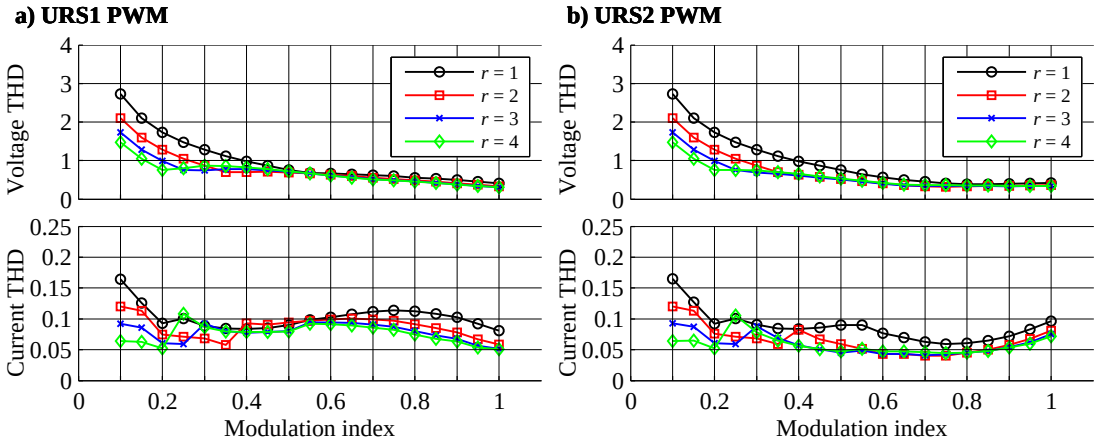
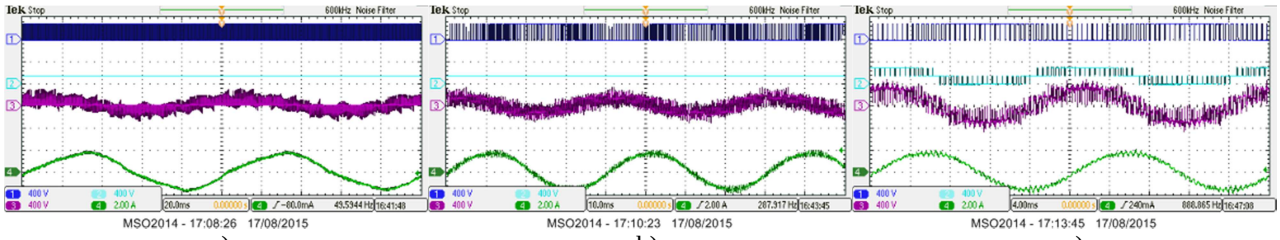


Fig. 4.42. Phase voltage and phase current THD(M) for URS2 (b) with different dc-link voltage ratios.

4.4.4. EXPERIMENTAL RESULTS

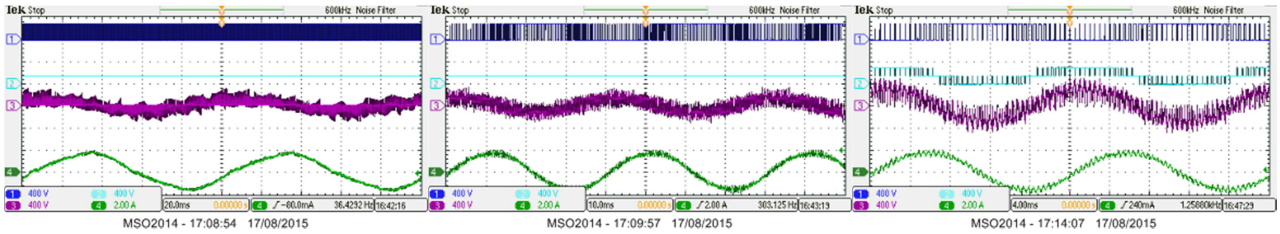
Experimental setup parameters are the same as in Section 3.3 (Appendix 2). Recorded waveforms of v_{21} (CH1), v_{11} (CH2), v_1 (CH3) and i_1 (CH4) for different values of M and r are shown in Figs. 4.43-4.48. With $r = 1$, the 2L-OeW-2L and 3L-OeW-2L drives produce identical waveforms with both modulation strategies up to $M = 0.525$, since only VSI_2 is used (Figs. 3.40, 3.41, 4.43 and 4.44). This seems to be a waste of hardware in the case of the 3L-OeW-2L topology. At the same time, waveforms for $M = 1$ in Figs. 4.43 and 4.44 are very similar to the corresponding ones in Figs. 3.40 and 3.41. This fact reinforces the starting impression (based on the topology analysis and semiconductor ratings), that low r values are not of interest for the 3L-OeW-2L drive. From that point of view, if decoupled CB PWM has to be applied for the OeW drive with $r = 1$ (due to application requirements), the 2L-OeW-2L drive seems to be the superior option.

When $r > 1$, decoupled methods with the 3L-OeW-2L drive result in more sinusoidal phase voltages and currents in multilevel modes. As expected, due to the nature of decoupled modulation, suboptimal modulation is performed, compared to the waveforms obtained with the same r values and coupled methods. As already explained, both 2L-OeW-2L and 3L-OeW-2L topologies are able to produce four phase voltage levels if $r = 2$ is applied. However, due to the existence of additional voltage level on VSI_1 side, phase voltage waveforms are finer in the case of decoupled methods and the 3L-OeW-2L drive. Examination of the leg and phase voltage waveforms in Figs. 4.45 and 4.46 for $M = 0.5$ and 1 shows that, for the negative and positive phase voltage, different voltage levels on VSI_1 side are in use (0 and $V_{dc1}/2$ and $V_{dc1}/2$ and V_{dc1}, respectively), while both VSIs are switching with the PWM steps of 200 V. This effectively eliminates some of the unwanted transitions in the phase voltages that are present in waveforms obtained with a 2L-OeW-2L drive under the same conditions.



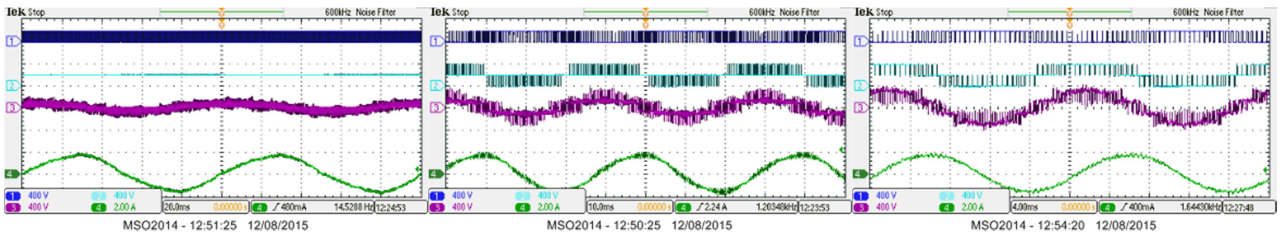
a) b) c)

Fig. 4.43. Experimental results: waveforms with URS1 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

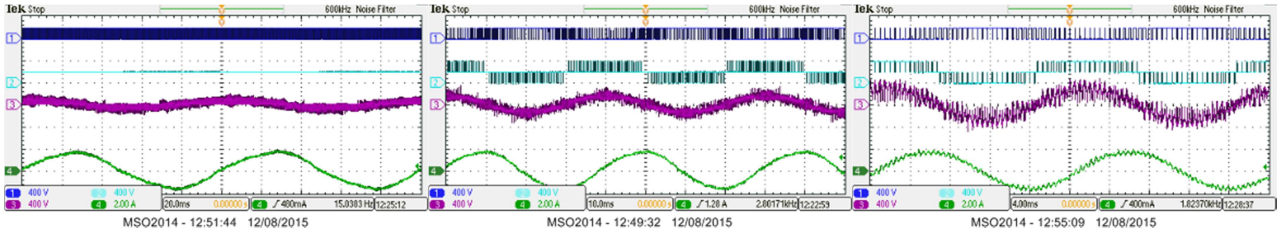
Fig. 4.44. Experimental results: waveforms with URS2 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

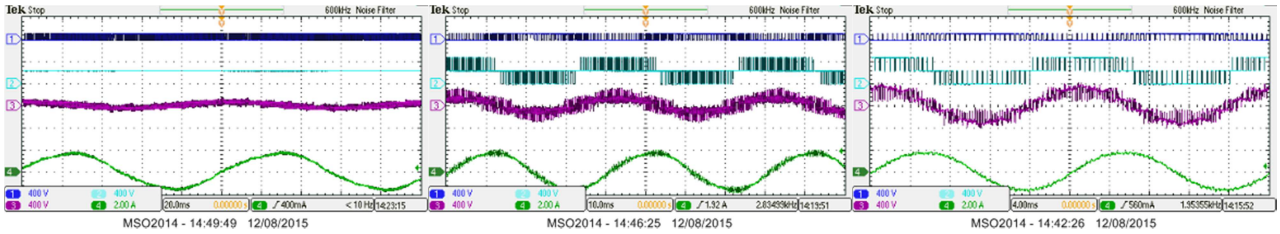
Fig. 4.45. Experimental results: waveforms with URS1 PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

With $r = 4$, the drive is theoretically equivalent to a six-level single-sided drive. Hence, waveforms in Figs. 4.47 and 4.48 are more sinusoidal than those in Figs. 4.45 and 4.46. The drive operates in two-level mode when $M \leq 0.2$. For $M = 0.5$ URS2 results in a more sinusoidal phase voltage waveform than URS1.



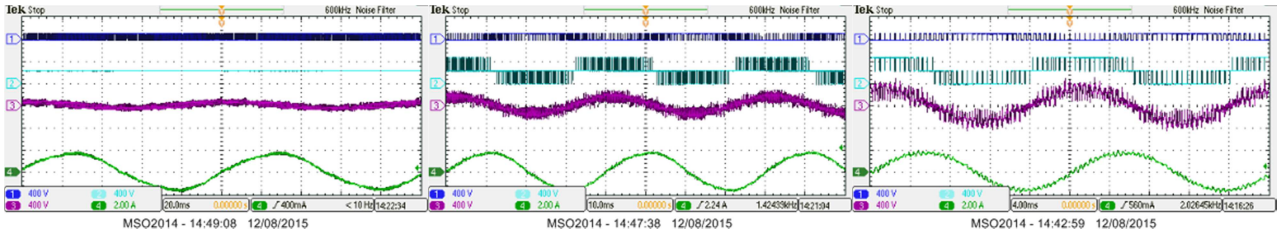
a) b) c)

Fig. 4.46. Experimental results: waveforms with URS2 PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 4.47. Experimental results: waveforms with URS1 PWM and $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).



a) b) c)

Fig. 4.48. Experimental results: waveforms with URS2 PWM and $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

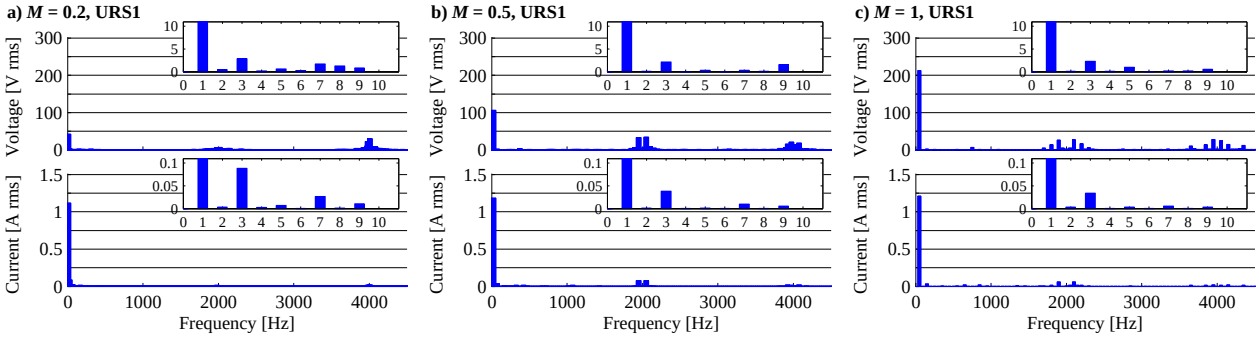


Fig. 4.49. Experimental results: v_1 and i_1 spectra for URS1 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

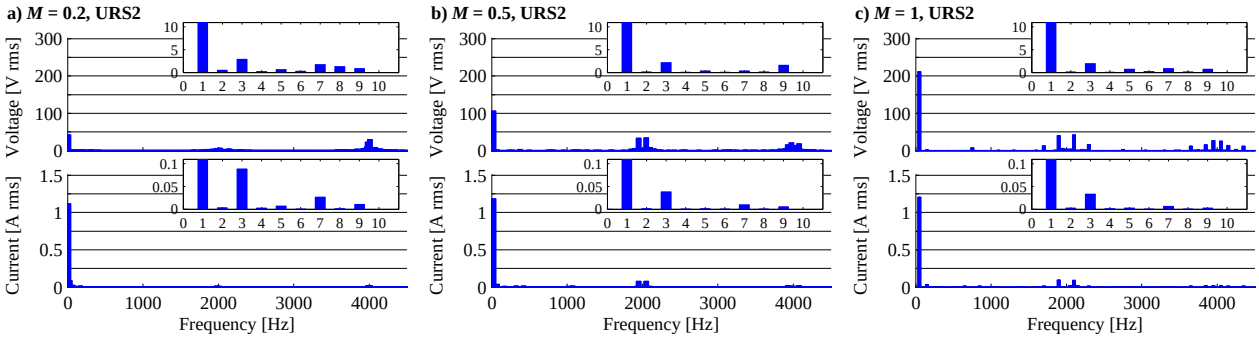


Fig. 4.50. Experimental results: v_1 and i_1 spectra for URS2 PWM and $r = 1$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

The drive performance can be further verified by detailed analysis of the obtained phase voltage and current spectra, shown in Figs. 4.49-4.54 and THD(*M*) dependencies, shown in Fig. 4.55. With $M = 0.2$, the best performance is obtained with $r = 4$. In that case $M_1 = 0$ and $M_2 = 1$, which leads to an optimal VSI_2 modulation. In multiphase operation, the phase voltage spectra are similar for the same *M* and different values of *r*, regardless of which URS scheme is applied. URS2 has better harmonic performance for modulation indices around 0.5, while URS1 results in lower phase current THD around $M = 1$. This is different to the 2L-OeW-2L case, where URS1 was superior regardless of *M*.

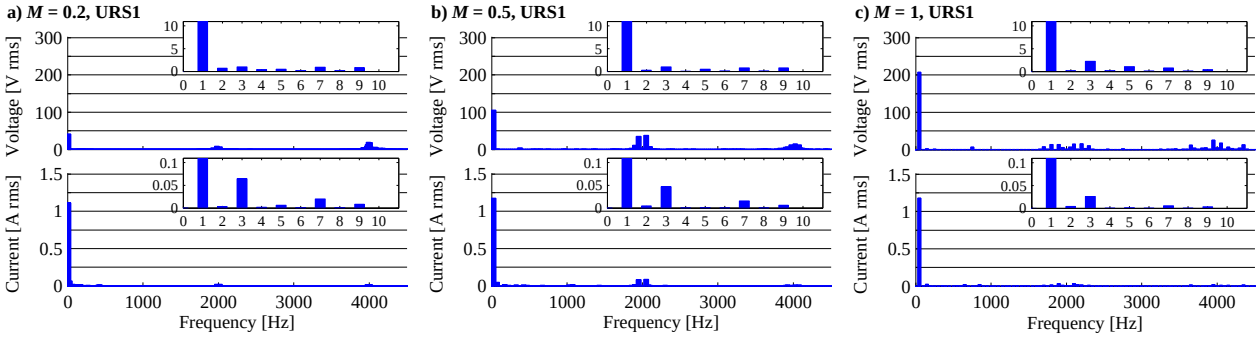


Fig. 4.51. Experimental results: v_1 and i_1 spectra for URS1 PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

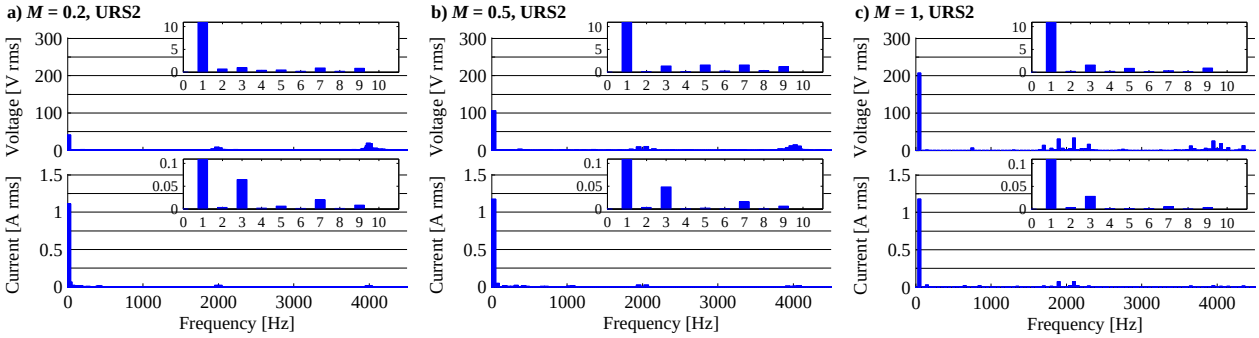


Fig. 4.52. Experimental results: v_1 and i_1 spectra for URS2 PWM and $r = 2$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

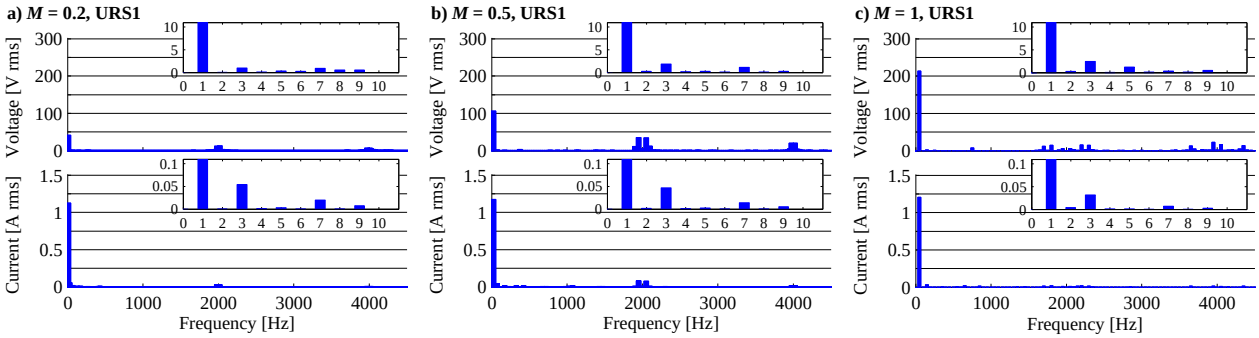


Fig. 4.53. Experimental results: v_1 and i_1 spectra for URS1 PWM and $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

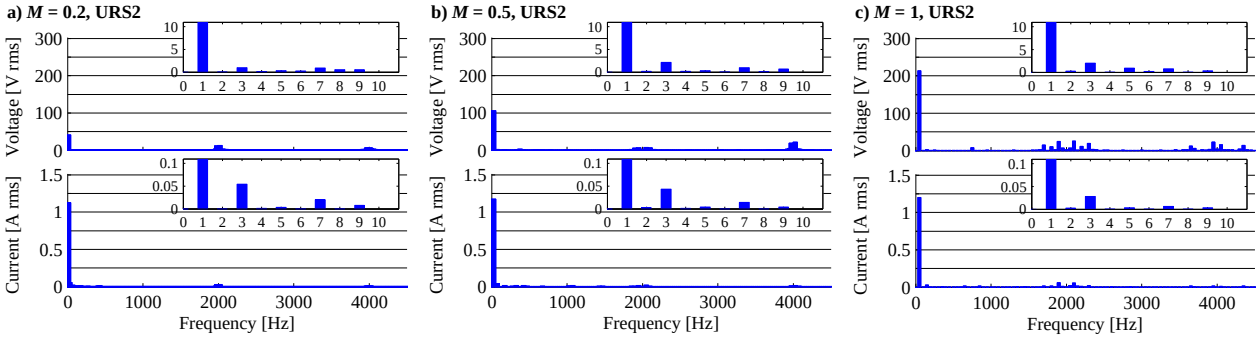


Fig. 4.54. Experimental results: v_1 and i_1 spectra for URS2 PWM and $r = 4$, with $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c).

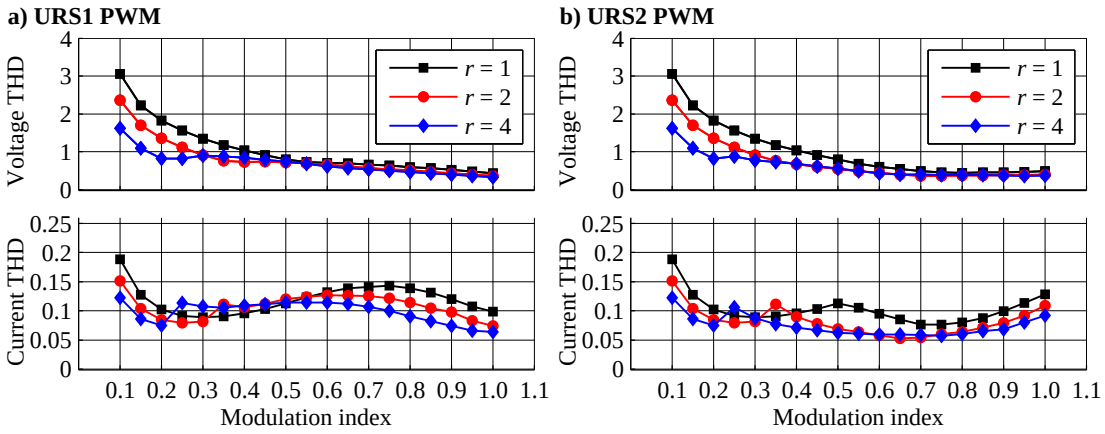


Fig. 4.55. Experimental results: THD(*M*) for URS1 (a) and URS2 (b).

4.5. SUMMARY

A novel multilevel five-phase open-end winding drive is analysed in this chapter. The drive consists of a five-phase induction machine with open-end windings, supplied from two voltage source inverters, with isolated dc-links. The inverter with the higher dc-link voltage is a three-level neutral-point clamped VSI. The other side of the machine windings is supplied from a two-level VSI. It is shown that this drive configuration can operate as a four-, five- or six-level single sided five-phase drive. The number of equivalent voltage levels depends on the ratio between dc-link voltages that are used to supply the two inverters. Detailed analysis of coupled and decoupled CB PWM methods and their harmonic performance versus dc-link voltage ratio is presented, in order to narrow down the number of possible drive configurations that might be of interest for high-power applications. Similarly to the findings in Chapter 3, dc-link voltage ratios that result in equidistant voltage levels lead to the best harmonic performance when coupled CB PWM methods are applied. Again, only the four-level configuration (dc-link voltage ratio 2:1) does not lead to simultaneous switching of the inverters, which is identified in Chapter 3 as the reason for dead-time spikes. This problem is encountered in five- and six-level configuration cases. Although being less severe than in the case of the topology analysed in Chapter 3, it is clearly shown that dead-time spikes again increase phase current harmonic distortion and practically eliminate all the benefits from a higher number of voltage levels. In order to eliminate these issues, the same CB PWM modifications, proposed in Chapter 3, are applied in the affected reference zones. The final modulation strategies are experimentally verified. Regarding five- and six-level configurations, PD and APOD result in similar harmonic performance, since differences introduced by different carrier arrangements are suppressed by the influence of an increased number of voltage levels. The same conclusion can be derived for CMV performance.

Decoupled modulation strategies are analysed next. It is shown that almost the same modulation scheme from Chapter 3 can be applied, regardless of the dc-link voltage ratio. The only difference in implementation comes from the different structure of the inverter with a higher dc-link voltage level, where two carrier signals are required for three-level modulation. Despite the simple implementation, it is shown that this difference in topology structure leads to great improvement of harmonic performance, when compared to the case where decoupled CB PWM schemes are applied to the topology with two two-level inverters. The analysis of total harmonic distortion shows that these two modulation methods have different performance in different modulation index ranges. The idea that optimal decoupled modulation should switch between URS1 and URS2, to optimise the harmonic performance, as a function of instantaneous modulation index value, is briefly discussed in Chapter 8, together with other topics which might be interesting for future work.

Chapter 5

ANALYSIS OF DC-LINK VOLTAGE STABILITY IN OPEN-END WINDING DRIVES

5.1. INTRODUCTION

In general, dc-link capacitor voltage balancing is an important topic for all multilevel voltage source topologies [Rodriguez et al. (2009), Kouro et al. (2012)]. This issue has high importance since development of modulation methods usually assumes that the dc-link voltages are nearly constant. Besides, capacitors are the primary energy storage components in voltage source inverters and any unexpected voltage variation across their terminals may lead to an overvoltage, and ultimately breakdown.

In traditional single-sided two-level drives, the dc-link voltage is usually formed using an ac-dc converter with a single capacitor bank placed in between two dc-link rails. The capacitor voltage is constant and stable during regular operation and only a braking process leads to dc-link voltage increase (referred to here as overcharging phenomenon). This is usually overcome using a braking chopper and dissipating the excess power in a braking resistor. For applications in which braking or speed reversal are frequent, more complex solutions are developed, in order to enable regenerative braking [Wilamowski and Irwin (2011), Kouro et al. (2012)].

In the case of multilevel single-sided drives, the capacitor voltage balancing problem is usually manifested as unbalanced discharge of capacitor banks, which leads to unexpected variations of voltage levels. In the oldest variant of a multilevel inverter topology, CHB, separate and isolated dc voltage sources for every capacitor bank are required [Kouro et al. (2012)]. This practically means that unbalanced discharge of the capacitors leads to unbalanced power consumption from different dc voltage sources. In many other cases, such as NPC, FC and MMC topologies, capacitor voltage balancing is one of the primary tasks during the modulation strategy design, since all voltage levels are formed from a single dc source and split among different capacitor banks in the pre-charge process [Kouro et al. (2012)]. The NPC has a single capacitor bank per voltage level, shared between all drive phases, while FC and MMC have separate capacitor banks in each drive phase. This difference does not have any consequences on the overall volume and cost of capacitor bank components, often considered as important parameter in the drive design, but it leads to simpler hardware solutions for capacitor balancing issue in the case of NPC, when compared to FC and MMC topologies, due to the centralised energy storage.

In all multilevel drive cases the possibility of capacitor voltage unbalance has to be taken into account during the hardware design stage, since discharge of one capacitor bank may lead to overvoltage of the other capacitor banks. A straightforward solution to this problem is to choose capacitors and semiconductor components that are able to withstand the overall dc-link voltage. As in any other case of overrating, this increases the overall cost and lowers the power density of the drive. The second approach is to use auxiliary circuits, similar to the braking choppers in two-level VSIs, in order to limit capacitor voltage rise above the certain level. In that case unbalanced capacitor discharge causes additional energy losses, due to surplus energy dumping. A software approach, i.e. modification of the modulation strategy, is less costly and more elegant solution, but it always represents a trade-off between harmonic quality of produced waveforms and capacitor voltage balancing. Often, it cannot be realised without additional sensors, which is still much cheaper when compared to hardware modifications at the power stage of the application.

This chapter is dedicated to the analysis of this problem with regard to open-end winding drives. Although five-phase OeW drives are considered, the presented modelling and analysis approach can be applied to the drive with an arbitrary number of phases. Probably the most relevant attempts to analyse dc-link capacitor voltage balancing in OeW drives are reported in [Ewanchuk and Salmon (2010), Reddy et al. (2011), Somasekhar and Reddy (2011), Ewanchuk et al. (2013), Jones et al. (2014), Chowdhury et al. (2015)]. All of them can be classified as voltage-based dc-link capacitor voltage analysis, since they rely on the Kirchhoff's voltage law and the analysis of space vector application times and their impact on the dc-link capacitor voltages. However, they can be applied only in special cases, for which proposed control algorithms are developed, since parameters such as the number of voltage levels, number of drive phases and dc-link voltage ratio define the phase voltage space vectors distribution, while their influence on the dc-link capacitor voltages is defined under the assumption that current flow in all drive phases is always the same when a specific vector is applied. This last condition drastically limits the number of cases in which voltage-based analysis can be used, since phase angle between stator phase voltage and stator phase current is a variable load-dependent parameter.

In this chapter, a novel approach to dc-link capacitor voltage unbalance analysis, partly reported in [Darijevic et al. (2015a), Darijevic et al. (2015c)] is explained for 2L-OeW-2L and 3L-OeW-2L in Sections 5.2 and 5.3, respectively. It is shown that complete analysis of dc-link capacitor charging and discharging processes can be performed using only the Kirchhoff's current law, regardless of the desired (projected) number of the phase voltage levels and number of phases. This approach is referred to as current-based dc-link capacitor voltage analysis. Firstly, impacts of drive and modulation strategy parameters on dc-link capacitor voltages are analysed using a simplified and then linearized drive model, which does not include pulse width modulation and relies on a sinusoidal approximation, i.e. the harmonic content of all ac signals in the circuitry is neglected. Results from this analysis are verified using numerical simulations, based on the models used in [Darijevic et al. (2015c), Darijevic et al. (2015d)], where only PD PWM is analysed. Here, models are extended to other modulation strategies from Chapters 3 and 4.

It is shown that, in some cases, the modulation strategy naturally keeps all voltage levels constant. Unfortunately, this is not the case when the dc-link voltage ratio is used in combination with simultaneous switching of two inverters. As reported in [Reddy and Somasekhar (2013), Jones et al. (2014)], the 2L-OeW-2L four-level drive suffers from a dc-link capacitor overcharging issue. Application of the derived modelling approach and analysis methods to two drive configurations ($r = 1$ and $r = 2$), considering all modulation methods presented in Chapter 3, shows that the overcharging phenomenon exist only if coupled modulation is applied to the four-level configuration ($r = 2$). Unfortunately, this case is identified as optimal, with regard to harmonic performance in Chapter 3. Combination of the results from Chapter 3 and Section 5.2 leads to a conclusion that a trade-off between harmonic performance and dc-link capacitor voltage balancing is necessary for the 2L-OeW-2L topology.

Section 5.3 provides the analysis of the dc-link capacitor voltage balancing for the 3L-OeW-2L drive case. Although this case is more complex, the conclusions are similar to those drawn from the analysis of the 2L-OeW-2L drive. That is, the 3L-OeW-2L drive suffers from unstable dc-link voltages if coupled modulation methods are applied to drive configurations where the dc-link voltage ratio is used to increase the overall number of voltage levels. As known from Section 4.3, such modulation strategies always employ simultaneous switching of two VSIs, which enables utilisation of additional voltage level(s). It is important to emphasise here that the dc-link voltage ratio is not the cause of problem. Comparison of the results obtained with coupled and decoupled PWM methods, applied for the same dc-link voltage ratio, shows that the main cause of dc-link capacitor voltage unbalance or overcharging comes from the modulation strategy properties.

Experimental verification presented in this chapter, based on the comparison of measured dc-link currents for various OeW configurations, effectively demonstrates the impact of the overcharging phenomenon on the drive overall energy consumption. These findings, in combination with the harmonic performance analysis reported in Chapters 3 and 4, lead to important conclusions about how the OeW drive should be modulated when different configurations are used.

5.2. STABILITY ANALYSIS OF THE 2L-OEW-2L DRIVE DC-LINK VOLTAGES

5.2.1. PRELIMINARY ANALYSIS

The extended equivalent model, shown in Fig. 5.1, is used in this analysis instead of the drive circuitry in Fig. 3.1. Two dc sources, denoted with green dashed rectangles represent the simplest dc-link voltage formation, based on three-phase diode rectifiers with suppressed output voltage ripple. Inputs of these two dc-sources are mutually isolated using three-phase transformers. Voltages of ac sources v_{ac11}, v_{ac12} and v_{ac13} represent a symmetrical three-phase system with 120° mutual phase shift and amplitudes determined with the desired output voltage $v_{cdc1} = V_{dc1}$. Similarly, the second three-phase diode bridge is supplied from v_{ac21}, v_{ac22} and v_{ac23}, whose amplitudes are adjusted according to V_{dc2}. Dashed lines in continuation of dc-link rails suggest that all five drive phases are connected to them. For the purpose of this analysis, voltages across dc-link capacitors are denoted with v_{cdc1} and v_{cdc2}, indicating that they are treated as time-dependent variable voltages (with dominant dc component). Clearly, in regular conditions the two capacitors' voltages have a dominant dc component and negligible ripple: $v_{cdc1} = V_{dc1}$ and $v_{cdc2} = V_{dc2}$.

A limitation of the presented solution is related to power flow, which has great significance for the following analysis. Due to diode bridge structure, it is clear that i_{dc1} and i_{dc2} can be only positive. This is in agreement with the expected behaviour of the whole drive system: since voltages V_{dc1} and V_{dc2} are positive, i_{dc1} and i_{dc2} should be positive as well, in order to provide (i.e. source) power to the inverters and finally machine, which is in motoring regime. However, during braking and speed reversal, the rectifier structure disables the opposite power flow, i.e. so-called regenerative braking or power recuperation. This means that a braking chopper is necessary, actually two of them in the case of 2L-OeW-2L topology.

Using the Kirchhoff's current law, on the upper dc-link contours, which include all upper inverter-leg nodes in Fig. 5.1, one can determine dc-link currents for the 2L-OeW-2L drive:

$$\begin{aligned} i_{cdc1}(t) &= i_{dc1}(t) - i_{dclink1}(t) \\ i_{cdc2}(t) &= i_{dc2}(t) - i_{dclink2}(t) \end{aligned} \tag{5.1}$$

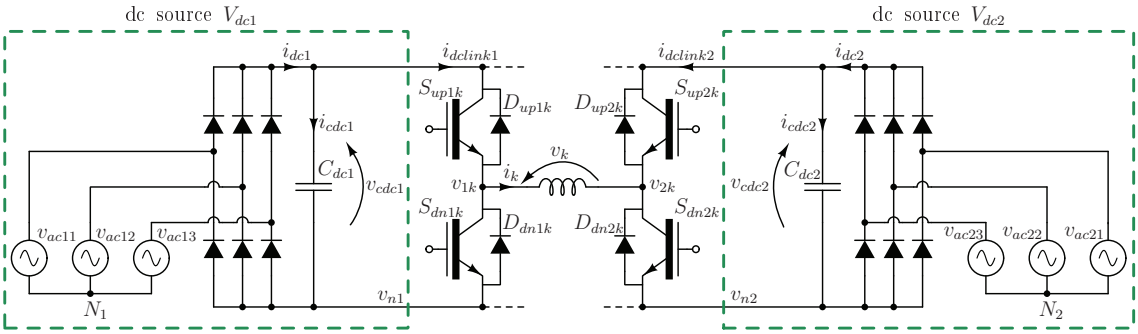


Fig. 5.1. Extended equivalent model for the 2L-OeW-2L topology. Example of dc-link voltage formation with three-phase diode rectifiers with suppressed output voltage ripple.

Currents $i_{dclink1}$ and $i_{dclink2}$ can be calculated only if the inverters' operation and conductance of each semiconductor device is known. An upper IGBT in phase k in VSI_1 (S_{up1k}) will conduct when its gating signal is on and if the phase current i_k is positive. Naturally, diode D_{up1k} is turned off in this situation. For the negative phase current and the same gating signal high level, freewheeling diode D_{up1k} conducts the phase current, while S_{up1k} is turned off. The same reasoning can be applied for the lower IGBT+D pair in VSI_1. During the dead time interval, both S_{up1k} and S_{dn1k} are turned off, which means that only D_{up1k} will conduct for $i_k < 0$, and D_{dn1k} for $i_k > 0$. Relations between conduction states and phase current sign are opposite for VSI_2. Hence, S_{up2k} conducts only if its gating signal is on the high level and $i_k < 0$, while D_{up2k} can only conduct if phase current is positive. Symmetrically, S_{dn2k} is turned on when its gating signal is on and if $i_k > 0$, while D_{dn2k} conducts only negative phase current. Analysis of semiconductor states for the condition $i_k = 0$ is not of interest for this model since this case has no influence on dc-link capacitor charge. Using definitions of switching states from Chapter 3, it is clear that the overall dc-link currents can be calculated as a sum of all phase currents, multiplied with the switching state of the corresponding upper IGBT+D pair:

$$\begin{aligned} i_{dclink\ 1}(t) &= \sum_{k=1}^{5} \left(S_{1k}(t) \cdot i_k(t) \right) \\ i_{dclink\ 2}(t) &= -\sum_{k=1}^{5} \left(S_{2k}(t) \cdot i_k(t) \right) \end{aligned} \tag{5.2}$$

General relationship between capacitor voltage and current are:

$$\begin{aligned} v_{cdc1}(t_2) &= \frac{1}{C_{dc1}} \int_{t1}^{t2} i_{cdc1}(t) \cdot \mathrm{d}t + v_{cdc1}(t_1) \\ v_{cdc2}(t_2) &= \frac{1}{C_{dc2}} \int_{t1}^{t2} i_{cdc2}(t) \cdot \mathrm{d}t + v_{cdc2}(t_1) \end{aligned} \tag{5.3}$$

where $v_{dc1}(t_1)$ and $v_{dc2}(t_1)$ are, respectively, C_{dc1} and C_{dc2} voltage levels at $t = t_1$. The same expressions can be written in extended form, which shows the relationship between switching states and instantaneous dc-link capacitor voltage value. Using (5.1) and (5.2) to calculate i_{cdc1} and i_{cdc2} in (5.3) one gets:

$$\begin{aligned} v_{cdc1}(t_2) &= \frac{1}{C_{dc1}} \int_{t1}^{t2} \left(i_{dc1}(t) - \sum_{k=1}^{5} S_{1k}(t) \cdot i_k(t) \right) \cdot \mathrm{d}t + v_{cdc1}(t_1) \\ v_{cdc2}(t_2) &= \frac{1}{C_{dc2}} \int_{t1}^{t2} \left(i_{dc2}(t) + \sum_{k=1}^{5} S_{2k}(t) \cdot i_k(t) \right) \cdot \mathrm{d}t + v_{cdc2}(t_1) \end{aligned} \tag{5.4}$$

Analysis of (5.4) shows that the capacitor voltage remains constant only if the integral summand is zero. Since it is already concluded that i_{dc1} and i_{dc2} cannot be negative, this condition comes down to: v_{cdc1} and v_{cdc2} are constant only if $i_{dclink1}$ and $i_{dclink2}$ are positive. Obviously, the 2L-OeW-2L topology cannot suffer from capacitor discharge problem as long as the rest of the dc voltage sources are able to deliver additional charge fast enough. However, if the drive behaviour, caused by the chosen switching pattern and/or for any other reason, is such that $i_{dclink1}$ and/or $i_{dclink2}$ are negative, some additional charge will be added to the dc-link capacitors, even if the corresponding dc-link source current is equal to zero. From that point of view, it seems sufficient to analyse $i_{dclink1}$ and $i_{dclink2}$, in order to understand what conditions lead to dc-link capacitor overcharging problem (if any).

5.2.2. LINEARIZED DRIVE MODEL AND SINUSOIDAL APPROXIMATION

Under analysis the 2L-OeW-2L drive is in steady state operation. Phase currents are assumed to be purely sinusoidal:

$$i_k(t) = I_m \cdot \sin\left(\omega_m \cdot t - (k-1) \cdot 2 \cdot \pi/5 - \phi\right) \tag{5.5}$$

where I_m stands for expected phase current amplitude and k stands for phase number. In order to simplify calculations, I_m = 1 A is used in this analysis as well as in Section 5.3. Phase angle, calculated with respect to the corresponding phase voltage, is denoted with ϕ. Angular frequency $\omega_m = 2 \cdot \pi \cdot f_n \cdot M$ is utilised in (5.5) in order to model frequency of the currents produced under the *V/f* law (equation 3.8). This simplifies the model, since approximately constant phase current amplitude in steady state operation is expected throughout the modulation index range. Simplified phase voltage references are used, without min-max injection and with always constant reference offset:

$$v_k^*(t) = \frac{1}{2} + \frac{M}{2} \cdot \sin(\omega_m \cdot t - (k-1) \cdot 2 \cdot \pi / 5) \tag{5.6}$$

Based on the phase voltage reference and modulation algorithms, duty ratios of S_{up1k}, D_{up1k}, S_{up2k} and D_{up2k} are defined as the time of their conduction during one switching period. In order to eliminate PWM side-effects related to dead-time influence on low-order harmonic and high-order harmonic components, all semiconductor devices are considered as ideal, under the assumption of very high switching frequency. This enables further simplification of the circuit, where each IGBT+D pair can be considered as an ideal four-quadrant switch (although only current bidirectional flow is of interest for this analysis). As a consequence, a single duty ratio parameter can be assigned to S_{up1k} and D_{up1k}, referred to as d_{1k}. The same applies to S_{up2k} and D_{up2k} pair, which together form S_{2k} switch that has duty ratio d_{2k}. The final 2L-OeW-2L equivalent model under sinusoidal approximation is shown in the Fig. 5.2. Currents $i_{dclink1k}$ and $i_{dclink2k}$ represent contributions of the k^{th} drive phase to $i_{dclink1}$ and $i_{dclink2}$, respectively.

Careful inspection of the model and its representation in Fig. 5.2 poses several questions, which should be addressed before further analysis. Firstly it is clear that infinite switching frequency leads to infinitely small switching period, which makes terms such as duty ratio senseless. However, switching frequency is only considered to be high enough so that all switching effects can be neglected in the analysis. At the same time, duty ratio becomes a continuous time domain function, specified with modulation strategy algorithm. Since all switching effects are eliminated from the analysis, while phase current is purely sinusoidal, this also means that there are no ac components in the common mode voltage. However, Chapter 3 analysis leads to a conclusion that for $r > 1$, the CMV has non-zero dc component, which is clearly disregarded in Fig. 5.2. In the real drive model, this dc component is a consequence of sinusoidal phase voltage, produced by modulation of two inverters with unequal dc-links, which leads to almost sinusoidal phase currents. In this model however, phase currents are considered to be always sinusoidal, regardless of the modulation of two inverters, which means that the dc CMV component has no impact on the analysis. The same can be concluded for other dc voltages in Fig. 5.2. V_{dc1} and V_{dc2} are shown only to give the meaning of $i_{dclink1k}$ and $i_{dclink2k}$ currents. Since all parameters and variables in the above described model have form of piecewise linear functions, the circuit in Fig. 5.2 can be presented in linear form, shown in Fig. 5.3. Two ideal transformers are used to model the relations between the three drive stages: VSI_1, machine and VSI_2.

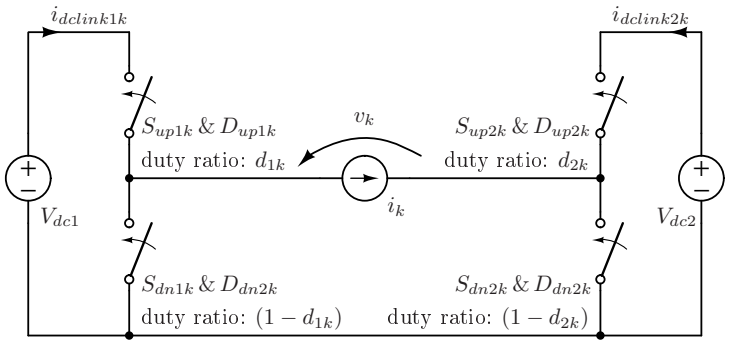


Fig. 5.2. Equivalent model of ideal 2L-OeW-2L topology under the sinusoidal phase current approximation. For simplicity, only k^{th} drive phase is shown.

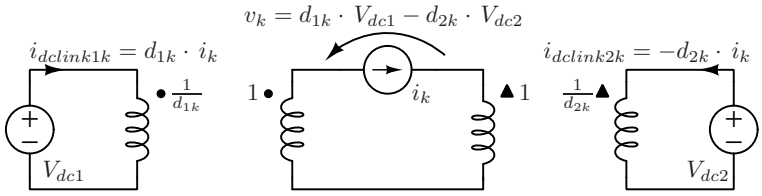


Fig. 5.3. Linearized equivalent model of ideal 2L-OeW-2L topology under the sinusoidal phase current approximation.

Numbers of turns of individual windings are related to duty ratios of two inverters. The aim of this model is to provide insight into the phase current and modulation strategy influence on dc-link voltage balancing. From this point of view, it is practical to consider phase currents and duty ratios as system inputs, while dc-link currents are treated as system outputs.

5.2.3. ANALYSIS FOR DC-LINK VOLTAGE RATIO 1:1

The first case under analysis is the 2L-OeW-2L drive with $r = 1$, i.e. three-level configuration. Having in mind basic principles of carrier based PWM and two inverters operation defined with (3.10), duty ratios can be analytically expressed, using phase voltage reference and equivalent voltage levels ($l_1 = 0$, $l_2 = 1/2$ and $l_3 = 1$ in Figs. 3.5a and 3.6a and 4.3a). Any duty ratio in the circuit may take an instantaneous value between 0 and 1. However, since phase voltage reference and carriers do not have the same amplitude and range, some numerical manipulations of the phase voltage reference are needed, in order to obtain duty ratios in expected range. In order to eliminate the offset introduced by carriers' minimal value different from 0, one has to subtract the lower reference zone border from v_k^*, in the corresponding reference zone (see Figs. 3.5a and 3.6a). For example, if the reference belongs to the reference zone 1 in Fig.3.5a, then v_k^* has to be used in further calculations, since the lower reference zone border is $l_1 = 0$, i.e. $v_k^*(t) - l_1 = v_k^*(t)$. Secondly, negation in the final expressions for switching states based on A_{ik}, like in (3.10), means that the phase voltage reference has to be subtracted from the upper voltage level that defines that reference zone. This rule transforms the output from the previous example to $(l_2 - v_k^*(t))$. Finally, the span of the reference zone versus the overall phase voltage reference range defines a multiplication factor, which ensures that the overall duty ratio range is between 0 and 1. If equidistant voltage levels are used, this factor is always $(r + 1)$, which comes from (4.1) and Fig. 4.3a. Thus, final expression for d_{2k} in the reference zone 1 is: $2 \cdot (l_2 - v_k^*(t))$. The same reasoning is applied to the other cases presented in this chapter. In the case of this drive configuration (3.10) yields that VSI_1 operates in PWM mode if v_k^* belongs to the reference zone 2. Using the above rules, the final expression for $l_2 < v_k^*(t) \leq l_3$ for d_{1k} is $2 \cdot (v_k^*(t) - l_2)$, i.e. $l_2 = 1/2$, has to be subtracted from $v_k^*(t)$, since l_2 is the lower border of the corresponding reference zone. A complete list of expressions for duty ratios is provided in Table 5.1, for $r = 1$.

Table 5.1. Duty ratio calculations for the 2L-OeW-2L three-level configuration with coupled PWM methods.

Condition	$d_{1k}(t)$	$d_{2k}(t)$
$l_1 \leq v_k^*(t) \leq l_2$	0	$2 \cdot (l_2 - v_k^*(t))$
$l_2 < v_k^*(t) \leq l_3$	$2 \cdot (v_k^*(t) - l_2)$	0

Using the expressions for phase current and duty ratios, contributions of the k^{th} drive phase to the $i_{dclink1}$ and $i_{dclink2}$ can be calculated, based on the model in Fig. 5.3. Using phase voltage reference and phase current waveforms, as model inputs, VSIs duty ratios and resulting contributions of each inverter leg to the dc-link currents are obtained. Resulting waveforms are shown in Fig. 5.4, for different modulation indices and phase angles, for the first drive phase. Horizontal blue lines in the first subplot from the top represent reference zone borders (l_1, l_2 and l_3), as in Figs. 3.5a and 3.6a. The

upper two subplots represent model inputs, i.e. v_k^* and i_k, which is shown for three different ϕ values in (5.5). Contributions of k^{th} drive phase to $i_{dclink1}$ and $i_{dclink2}$ are: $i_{dclink1k}(t) = d_{1k}(t)\cdot i_k(t)$ and $i_{dclink2k}(t) = -d_{2k}(t)\cdot i_k(t)$, respectively. These are considered as final model outputs, shown in the lower two subplots in Fig. 5.4. Obtained waveforms show that phase shift between i_k and v_k^* has a strong influence on $i_{dclink1k}$ and $i_{dclink2k}$. This comes from the fact that duty ratios d_{1k} and d_{2k} are determined using v_k^* only (Table 5.1), while final dc-link currents are influenced by i_k as well. For example, during $0 < t \leq T/2$, v_k^* is in the reference zone 2, which results in $d_{1k}(t) = 2\cdot(v_k^*(t) - l_2)$, i.e. VSI_1 operates in PWM mode, while VSI_2 holds constant voltage level v_{n2}, $d_{2k} = 0$. However, phase current sign changes between $0 < t < T/4$ for $\phi < 90°$, which means that D_{up1k} conducts longer than S_{up1k}, resulting in $i_{dclink1k} > 0$ for a longer period of time, when compared to the interval when $i_{dclink1k} \leq 0$. Application of superposition principle gives the final expression for the mean values of $i_{dclink1}$ and $i_{dclink2}$ currents, during one fundamental period:

$$\overline{i_{dclink1}} = \frac{1}{T}\int_0^T \left(\sum_{k=0}^{5} \left(d_{1k}(t)\cdot i_k(t) \right) \right) \cdot \mathrm{d}t$$
$$\overline{i_{dclink2}} = \frac{1}{T}\int_0^T \left(\sum_{k=0}^{5} \left(-d_{2k}(t)\cdot i_k(t) \right) \right) \cdot \mathrm{d}t \tag{5.7}$$

Symmetry arguments and fact that d_{1k} and d_{2k} are equal to zero in one half of the fundamental period result in ($k = 1$):

$$\overline{i_{dclink11}} = \frac{M\cdot I_m}{T}\cdot \int_0^{T/2} \left(\sin^2(\omega_m\cdot t)\cdot\cos(\phi) + \sin(\omega_m\cdot t)\cdot\cos(\omega_m\cdot t)\cdot\sin(\phi) \right)\cdot \mathrm{d}t \tag{5.8}$$

$$\overline{i_{dclink21}} = -\frac{M\cdot I_m}{T}\cdot \int_{T/2}^{T} \left(\sin^2(\omega_m\cdot t)\cdot\cos(\phi) + \sin(\omega_m\cdot t)\cdot\cos(\omega_m\cdot t)\cdot\sin(\phi) \right)\cdot \mathrm{d}t \tag{5.9}$$

Using the fact that integral of the sum is equal to the sum of the integrals, the $i_{dclink1}$ and $i_{dclink2}$ mean values can be obtained multiplying solutions of (5.8) and (5.9) with the number of phases. Final expressions for mean dc-link current values are:

$$\overline{i_{dclink\ 1}} = \overline{i_{dclink\ 2}} = \frac{5\cdot M\cdot I_m\cdot\cos(\phi)}{4} \tag{5.10}$$

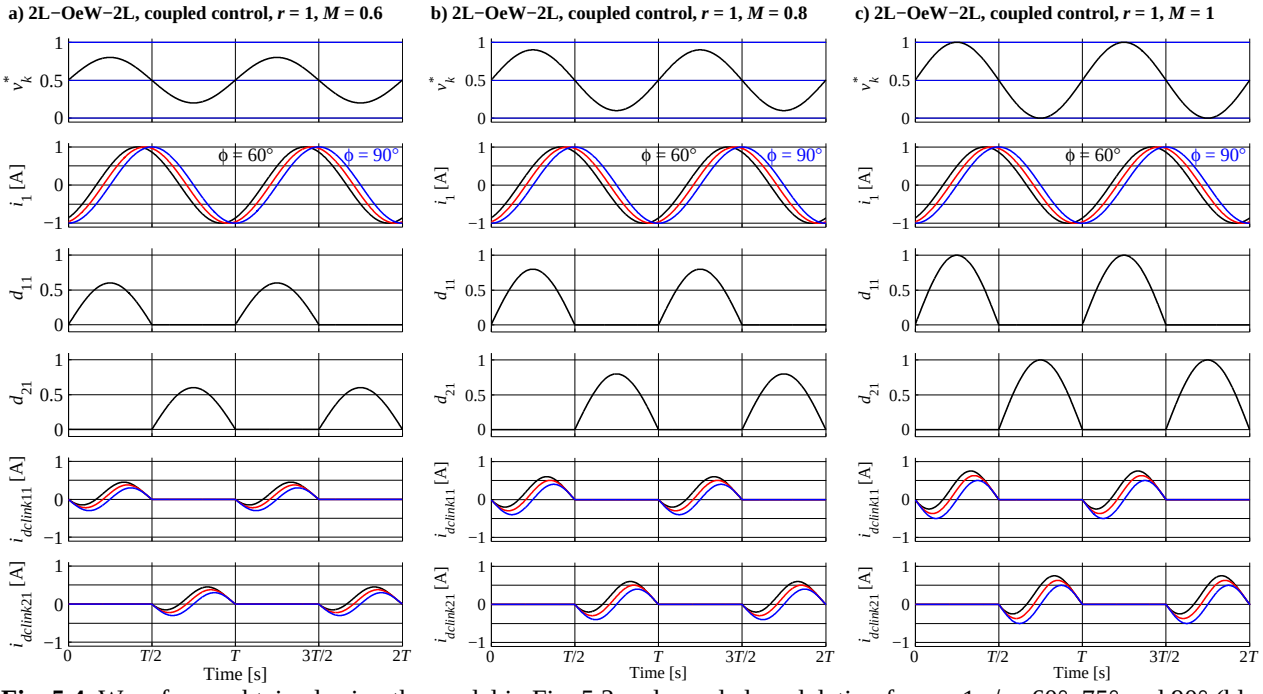


Fig. 5.4. Waveforms obtained using the model in Fig. 5.3 and coupled modulation for $r = 1$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

Expressions for both dc-link currents are the same, which is expected since VSI_1 and VSI_2 operate symmetrically, each in one half of the fundamental period, regardless of M. The most important conclusion is that both currents are always positive, since $\cos(\phi)$ is always greater than 0 for $0 \leq \phi \leq 90°$.

The same 2L-OeW-2L configuration ($r = 1$) can be modulated with decoupled CB PWM. Obtained waveforms are shown in Fig. 5.5. In multilevel operation mode, duty ratios of two VSIs are equal to the corresponding phase voltage references, given with (3.16) and (3.17). Using (3.17) and (5.5) for the phase current calculations (5.7), one gets:

$$\overline{i_{dclink\,1}} = \frac{5 \cdot I_m \cdot \cos(\phi)}{4} \cdot (2 \cdot M - 1) \tag{5.11}$$

$$\overline{i_{dclink\,2}} = \frac{5 \cdot I_m \cdot \cos(\phi)}{4} \tag{5.12}$$

Obtained expressions are very similar to those for the coupled modulation case. VSI_2 is sourcing the same amount of current from its dc-link source, when the drive works in multilevel mode, regardless of M. Both dc-link currents always have positive mean value, regardless of M and ϕ. These findings are confirmed numerically in Matlab for the full range of ϕ and M. Results are shown in Fig. 5.6.

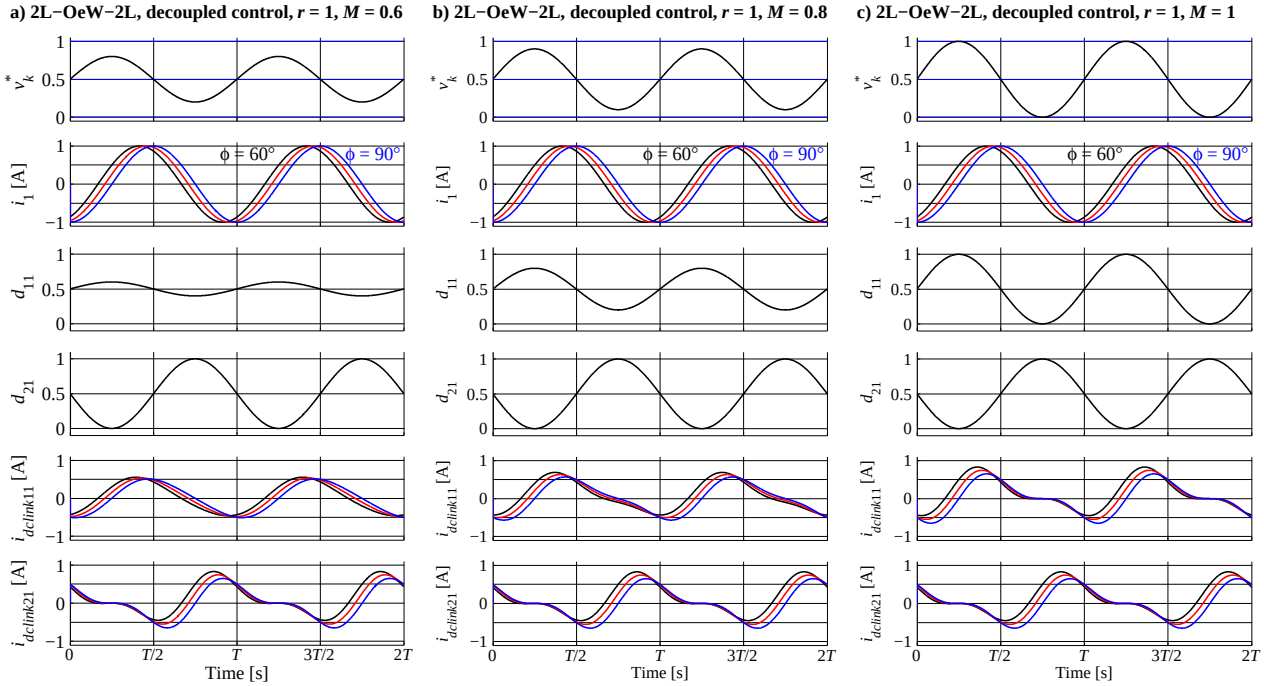


Fig. 5.5. Waveforms obtained using the model in Fig. 5.3 and decoupled modulation for $r = 1$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

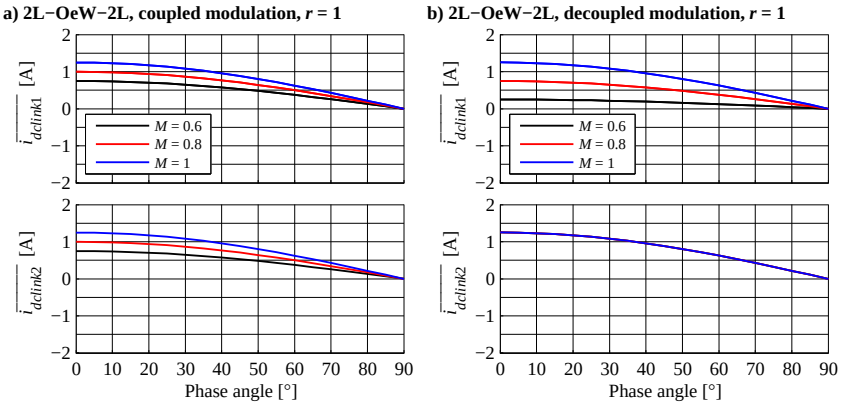


Fig. 5.6. Phase angle influence on the dc-link current mean values in the 2L-OeW-2L three-level configuration with coupled (a) and decoupled (b) modulation.

5.2.4. ANALYSIS FOR DC-LINK VOLTAGE RATIO 2:1

The second case of interest is the four-level configuration of the 2L-OeW-2L drive, with equidistant voltage levels ($r = 2$). Expressions for d_{1k} and d_{2k} are more complex for this configuration, since they depend on the modulation index and dc-link voltage ratio. Based on Table 3.4 and Figs. 3.5c and 3.6c, one may conclude that there are three different expressions for both duty ratios, due to the existence of three reference zones. They are summarised in Table 5.2 and depicted in Fig. 5.7 for the first drive phase, together with resulting dc-link currents contributions. Currents $i_{dclink1k}$ have similar properties as in the case of coupled methods for the three-level configuration, i.e. $\phi < 90°$ always results in longer positive intervals than negatives, which means that the drive sinks current from the VSI_1 dc source. The situation is more complex on the lower dc-link voltage side. For the shown cases, phase current is around its peak values when v_k^* belongs to reference zone 2. The presented waveforms show that the phase angle influence in this range on $i_{dclink2k}$ is low, while it's more dominant in reference zones 1 and 3. Modulation index in this case also has a strong influence on VSI legs contributions to dc-link currents. Hence, analysis of mean values has to be performed, in order to find under which conditions drive operates with $i_{dclink2} > 0$.

Table 5.2. Duty ratio calculations for the 2L-OeW-2L four-level configuration and coupled PWM methods.

Condition	$d_{1k}(t)$	$d_{2k}(t)$
$l_1 \le v_k^*(t) \le l_2$	0	$3\cdot(l_2 - v_k^*(t))$
$l_2 < v_k^*(t) \le l_3$	$3\cdot(v_k^*(t) - l_2)$	$3\cdot(v_k^*(t) - l_2)$
$l_3 < v_k^*(t) \le l_4$	1	$3\cdot(l_4 - v_k^*(t))$

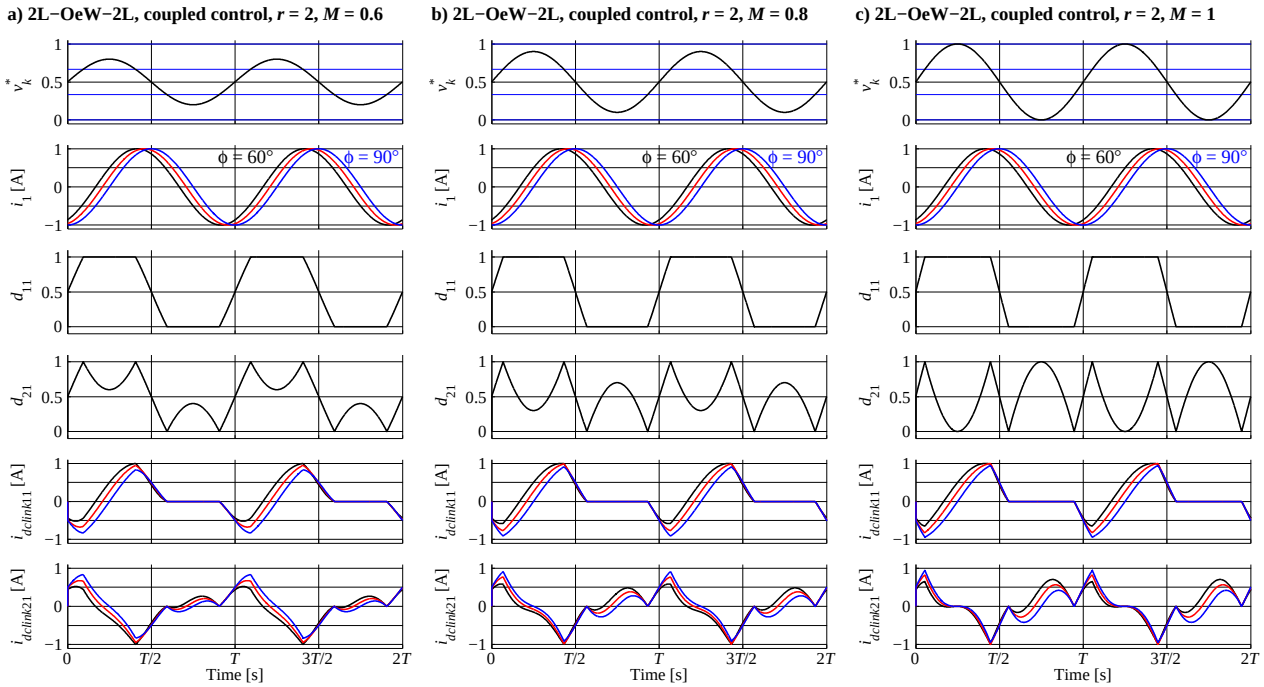


Fig. 5.7. Waveforms obtained using the model in Fig. 5.3 and coupled modulation for $r = 2$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

Detailed analysis of this case and analytical derivation of dc-link current mean values are given in Appendix 3. Clearly, this case is much more complex, when compared to the three-level configuration, not only because of the number of necessary integrations, but also due to *M*-dependent integration borders. The final expressions, obtained using wxMaxima (an open-source computer algebra systems software) and used for further computations are:

$$\overline{i_{dclink1}} = \frac{5 \cdot I_m}{4 \cdot \pi} \cdot \left\{ 8 \cdot \cos\left(\arcsin\left(\frac{1}{3 \cdot M} \right) \right) \cdot \cos(\phi) + \right.$$
$$\left. + M \cdot \left[6 \cdot \cos(\phi) \cdot \arcsin\left(\frac{1}{3 \cdot M} \right) - 3 \cdot \sin\left(2 \cdot \arcsin\left(\frac{1}{3 \cdot M} \right) \right) \cdot \sin(\phi) \right] \right\} \tag{5.13}$$

$$\overline{i_{dclink2}} = -\frac{5 \cdot I_m}{4 \cdot \pi} \cdot \left\{ (4 \cdot \cos\left(\arcsin\left(\frac{1}{3 \cdot M} \right) \right) \cdot \cos(\phi) + \right.$$
$$\left. + M \cdot \left[6 \cdot \cos(\phi) \cdot \arcsin\left(\frac{1}{3 \cdot M} \right) - 3 \cdot \cos\left(2 \cdot \arcsin\left(\frac{1}{3 \cdot M} \right) \right) \cdot \sin(\phi) - \frac{1}{2} \cdot \pi \cdot \cos(\phi)) \right] \right\} \tag{5.14}$$

Although being very complex, (5.13) and (5.14) have similar form and only differences are in the leading sign and the existence of $-1/2\ \pi \cdot \cos(\phi)$ term in the last summand in (5.14). In order to find under which conditions (i.e. M and ϕ values) the drive does not operate with positive dc-link currents, one would have to derive two $M(\phi)$ functions from (5.13) and (5.14) equal to zero, by equalizing both dc-link current mean values with zero. Finally, $M(\phi)$ roots need to be found.

Since it is clear the expressions are very complex, numerical iterative analysis is performed in Matlab. It showed that for any ϕ and M expression (5.13) returns a positive value, while the dc-link current of VSI_2 has a negative mean value for $0.33 < M < 0.825$. The lower border represents the minimal M for which 2L-OeW-2L with $r = 2$ operates in four-level mode (using both VSIs), while the upper border is determined by numerical analysis of (5.14). Situations in which only one inverter is used (i.e. $M < M_{max}/3$) are not of practical interest for this analysis, since in this case the dc-link capacitor voltages are kept constant by the rest of the power supply circuitry. Obtained results lead to several important conclusions, which can be applied to the real drive case. The phase angle has influence only on the amount of charge that is going to be added to the C_{dc2}, but not on the dc-link current sign, which depends on M.

The second interesting case for analysis with regard to 2L-OeW-2L drive with $r = 2$, is modulation with decoupled CB PWM. Expressions for d_{1k} and d_{2k} are again equal to VSI_1 and VSI_2 phase voltage references, which leads to almost identical final expressions for mean values of the two dc-link currents, when compared to the previously analysed configuration:

$$\overline{i_{dclink1}} = \frac{5 \cdot I_m \cdot \cos(\phi)}{6} (3 \cdot M - 1) \tag{5.15}$$

$$\overline{i_{dclink2}} = \frac{5 \cdot I_m \cdot \cos(\phi)}{6} \tag{5.16}$$

Obtained waveforms for decoupled modulation are shown in Fig. 5.8. Comparison with Fig. 5.5 confirms that the two cases are very similar, which is expected from the analysis in Chapter 3, where very low dependence of drive harmonic performance on r is observed.

Dependencies of dc-link current mean values for coupled and decoupled modulation of 2L-OeW-2L four-level configuration are shown in Fig. 5.9. In both cases VSI_1 operates with positive dc-link current, regardless of ϕ, sourcing the current to the drive. Negative dc-link current on VSI_2 side suggests that the inverter has the opposite power flow in the case of coupled modulation when $0.33 < M < 0.825$. In the case of decoupled modulation, the same inverter operates processing the same current, since M_2 is always constant in the multilevel operation range.

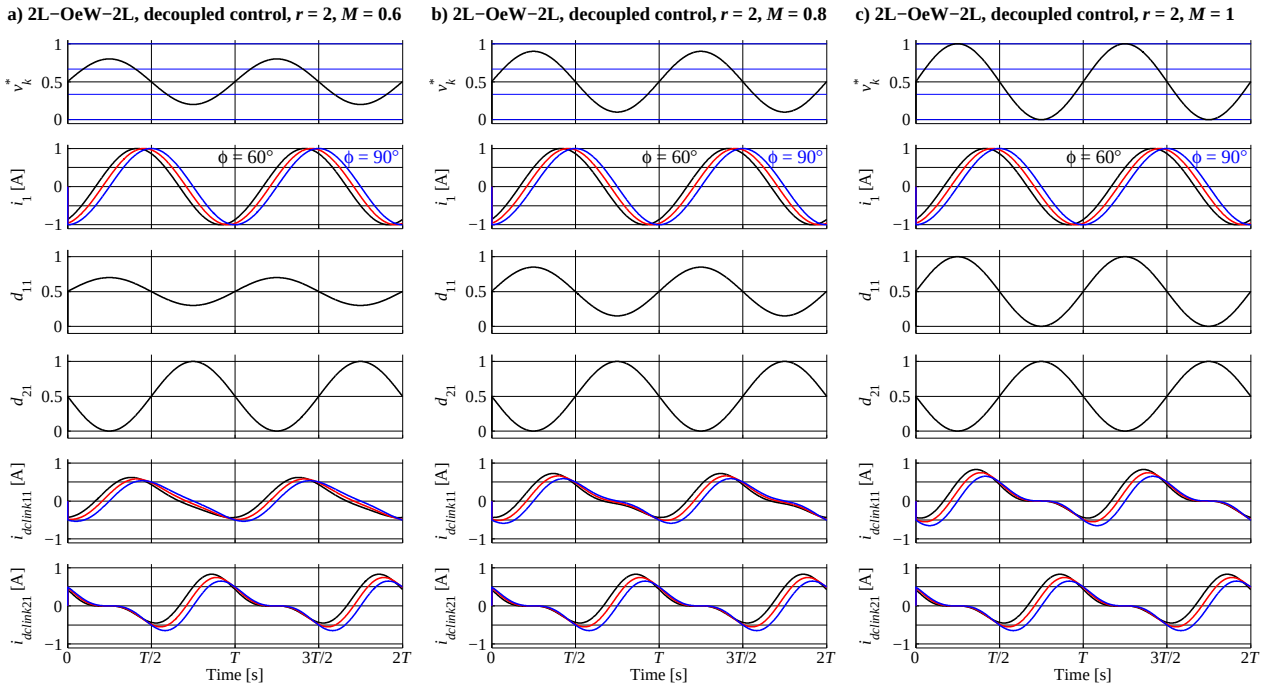


Fig. 5.8. Waveforms obtained using model in Fig. 5.3, decoupled modulation for $r = 2$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

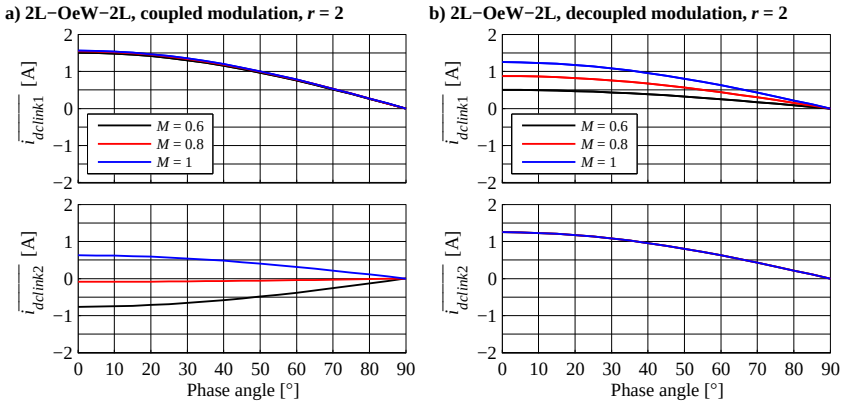


Fig. 5.9. Phase angle influence on the dc-link current mean values for a 2L-OeW-2L four-level configuration with coupled (a) and decoupled (b) modulation.

The presented analysis shows that in the case of coupled PWM schemes ($r = 2$) V_{dc2} has to be realised using current bidirectional power source and explains in what conditions this is necessary. Together with analysis in Chapter 3, this leads to a conclusion that the superior harmonic performance of 2L-OeW-2L four-level configuration is traded for additional complexity in hardware and additional energy losses, since simple solutions for dc sources (like in Fig. 5.1) cannot be used. In order to fully investigate what the exact impact of C_{dc2} overcharging is, detailed numerical simulations are performed, as well as experimental verification. This is presented in the next section.

5.2.5. SIMULATION AND EXPERIMENTAL RESULTS

Ideal dc source models that are used in numerical simulations in Chapter 3 are replaced with three-phase diode rectifiers, fed from two three-phase ac sources with an adjustable amplitude and frequency $f_g = 50$ Hz. The additional components are modelled according to the Appendix 1. Preliminary analysis showed that carrier arrangements have no

influence on the voltage stability of the dc-link capacitors, which is expected from the analysis in the previous section. In other words, IGBT and antiparallel diode in the upper IGBT+D pairs contribute to the dc-link capacitor charge in the same way, regardless of the carrier arrangement. Fig. 5.10 shows dc-link voltages in the case of PD PWM and URS1 PWM, representing coupled and decoupled modulation, respectively. In order to isolate the influence of switching pattern on dc-link voltages, simulation is performed in the following manner: in the first 0.5 s the drive is in transient and ideal dc-link sources are used. When steady state is reached the ideal dc sources are replaced with three-phase rectifier models. As reported in [Reddy and Somasekhar (2013), Jones et al. (2014)], PD PWM in the case of a dc-link voltage ratio 2:1 (i.e. $r = 2$) suffers from C_{dc2} overcharging. In particular, this phenomenon is observed in the modulation index range $0.35 < M < 0.825$, which is in agreement with findings from the previous section. However, it is clear that exact rate of overcharging depends on the phase angle. This conclusion comes from the Fig. 5.9, where the same modulation index results in different dc-link current mean values, for different ϕ. In this case, the drive is considered to be under no load, which means that demonstrated overcharging corresponds to ϕ value very close to 90°. In other words, the presented case is the best possible, where overcharging rate for $0.35 < M < 0.825$ is the lowest.

This narrows down the number of possible applications in which dc-link voltage ratio can be used in order to utilise the additional voltage level in combination with optimal four-level modulation. Namely, since dc-link voltage ratio is considered to be constant, increase of V_{dc2} leads to improper modulation. This is clear from the waveforms shown in Fig. 5.11, for the last 0.2 s of simulation run time. All the expected benefits from multilevel operation are eliminated in the case of $M = 0.6$ and $M = 0.8$, due to increase of V_{dc2}.

The second important observation is related to the overcharging rate when $r = 2$. One may notice that the $i_{dclink2k}$ mean value in Fig. 5.9a for $M = 0.8$ is very close to zero, meaning that the expected overcharging rate should be very slow. However, simulation results in Fig. 5.10b suggest that the overcharging rate is only 50% lower than in the case of $M = 0.6$. This is a consequence of overcharging influence on phase current low-order harmonics. Namely, the simplified model considers the phase currents as purely sinusoidal, which does not hold for the waveforms shown in Fig. 5.11, for $M = 0.6$ and 0.8. Additional distortion of the phase currents that comes from improper phase voltage waveform (a consequence of unbalanced dc-link voltages) introduces additional phase current low-order harmonic components, which lead to a different rate of overcharging, when compared to that expected based on the linear approximation. However, if the drive is aimed to operate only at its nominal speed (i.e. $M = 1$, Fig. 5.11c) or more precisely at speeds that correspond to for $M > 0.825$, then the 2L-OeW-2L with $r = 2$ can be modulated with PD or APOD PWM for any load (e.g. phase angle), even if the simplest power supply realisation is utilised. However, for variable speed-drives, it seems more appropriate to use $r = 1$ or decoupled modulation strategies.

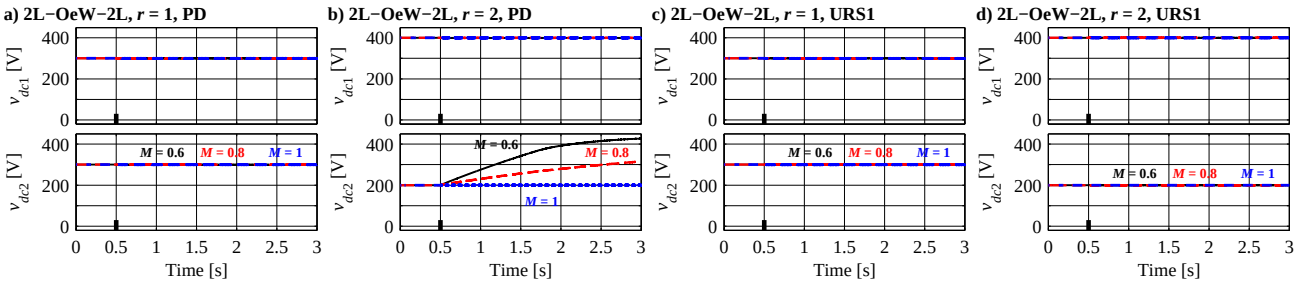


Fig. 5.10. Simulation results: 2L-OeW-2L drive dc-link voltages for PD PWM $r = 1$ (a), $r = 2$ (b), URS1 PWM $r = 1$ (c) and $r = 2$ (d).

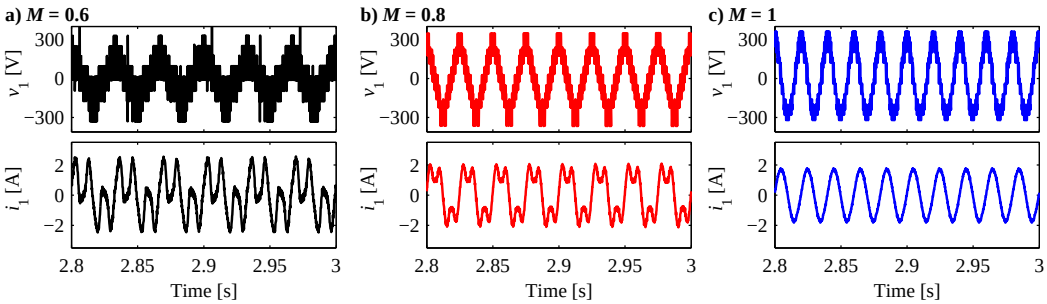


Fig. 5.11. Simulation results: 2L-OeW-2L drive with PD PWM, $r = 2$ steady state v_1 and i_1 for $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

Experimental verification of the dc-link capacitor overcharging problem is complex, since an uncontrollable increase of dc-link voltage can cause capacitor breakdown, often followed with further hardware damage. Therefore, a controllable four-quadrant voltage source is used during the examination of the 2L-OeW-2L four-level configuration, modulated with coupled CB PWM schemes. Experimental results for *V*/*f* control are shown in Fig. 5.12, for all analysed cases. The modulation index is linearly increased from 0 to 1, which corresponds with linear drive acceleration from 0 to 1500 rpm. Speed estimation, based on modulation index, is shown in Fig. 5.12, obtained via a dSpace D/A acquisition board, directly connected to the oscilloscope, which helped later synchronisation of measurements. This also results in the staircase shape of speed waveform due to low number of utilised quantization levels. The signals shown in Fig. 5.12 are highly filtered, in order to eliminate switching ripple and EMI noise. Due to the hardware configuration, it is only possible to measure i_{dc1} and i_{dc2} since dc-link voltage capacitors are incorporated within the inverters. This has no negative impact on the analysis, since the voltage sources are keeping constant dc-link voltages and measurements of their output currents (i_{dc1} and i_{dc2}) provide all needed information. In all cases, i_{dc1} is zero for two-level modulation. In the same range ($M < 0.35$), VSI_2 has positive dc-link current, which means that it is sourcing power to the drive. In multilevel regime, three-level configuration with coupled modulation and both configurations with decoupled modulation result in both i_{dc1} and i_{dc2} being positive. This means that the overall drive power is formed by combination of V_{dc1} and V_{dc2}. However, for $r = 2$, coupled modulation leads to negative i_{dc2} in the first part of the multilevel range. Grey area between two curves in the lowest subplot in Fig. 5.12a shows additional energy loss, caused by the overcharging phenomenon.

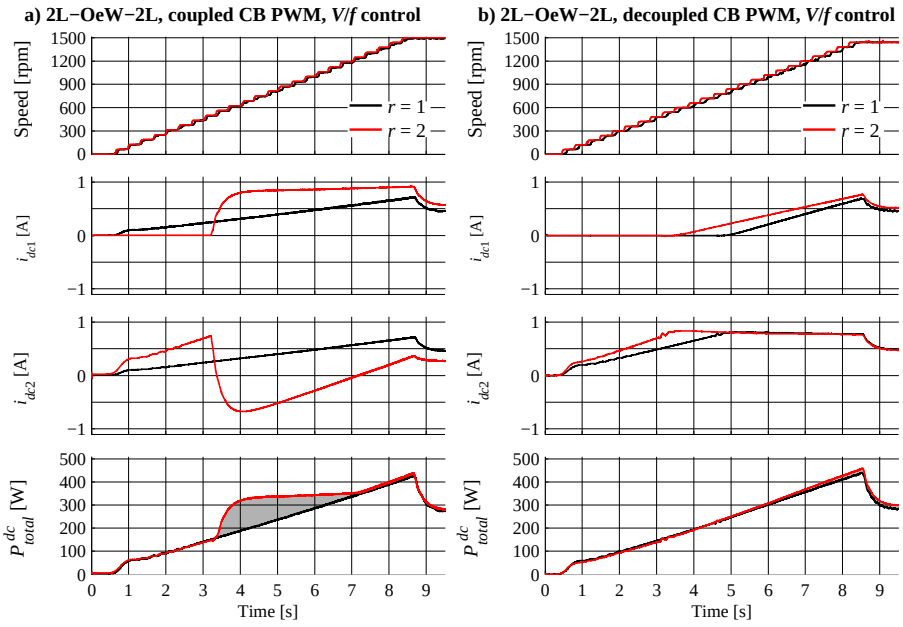


Fig. 5.12. Experimental results: 2L-OeW-2L dc-link currents and total drive power during *V*/*f* acceleration, for PD PWM (a) and URS1 PWM (b) with $r = 1$ and $r = 2$.

Since the inverters are supplied from the controllable dc sources, this means that total power is calculated as:

$$P_{total}^{dc} = \begin{cases} \overline{v_{dc1}(t) \cdot i_{dc1}(t)} + \overline{v_{dc2}(t) \cdot i_{dc2}(t)} & \text{if} \quad i_{dc2}(t) > 0 \\ \overline{v_{dc1}(t) \cdot i_{dc1}(t)} & \text{if} \quad i_{dc2}(t) \le 0 \end{cases} \tag{5.17}$$

where the bar over the symbol represents the mean value over one fundamental period. In the case when both inverters are sourcing the power to the drive, that is, when both dc-link currents are always positive, (5.17) gives the sum of their powers. Previous analysis shows that i_{dc1} is always positive, meaning that corresponding dc source is always sourcing power to the drive. Hence, condition in (5.17) considers i_{cdc2} only. Fig. 5.12 shows that the four-level configuration with coupled PWM methods leads to additional energy losses. This can be seen as a trade-off between hardware complexity and efficiency, for the given requirements of drive harmonic performance. Superior harmonic performance of coupled modulation strategies for $r = 2$ demonstrated in Chapter 3 potentially leads to the lower losses and reduction (or complete elimination) of filter components in ac transmission lines between inverters and machine. However, the provided results show that harmonic performance cannot be the only merit of modulation strategy quality. General, but often overlooked conclusion is that all application demands (power density, hardware complexity and price, efficiency, expected operating conditions, etc.) have to be analysed together, affecting both hardware and software design.

5.3. STABILITY ANALYSIS OF THE 3L-OEW-2L DRIVE DC-LINK VOLTAGES

5.3.1. PRELIMINARY ANALYSIS

The second topology under analysis in this thesis is the 3L-OeW-2L drive. Using extended equivalent model in Fig. 5.13, one can derive the dc-link model based on the Kirchhoff's current law:

$$\begin{aligned} i_{cdc11}(t) &= i_{dc1}(t) - i_{dclink1}(t) \\ i_{cdc12}(t) &= i_{dc1}(t) - i_{dclink1}(t) - i_{mp}(t) \\ i_{cdc2}(t) &= i_{dc2}(t) - i_{dclink2}(t) \end{aligned} \tag{5.18}$$

where i_{mp} stands for the current sourced from the mid-point of the NPC inverter dc side (Fig. 5.13). This current, as well as $i_{dclink1}$, $i_{dclink2}$, can have both positive and negative mean value during one fundamental period, which affects capacitor voltage balancing on VSI_1 side.

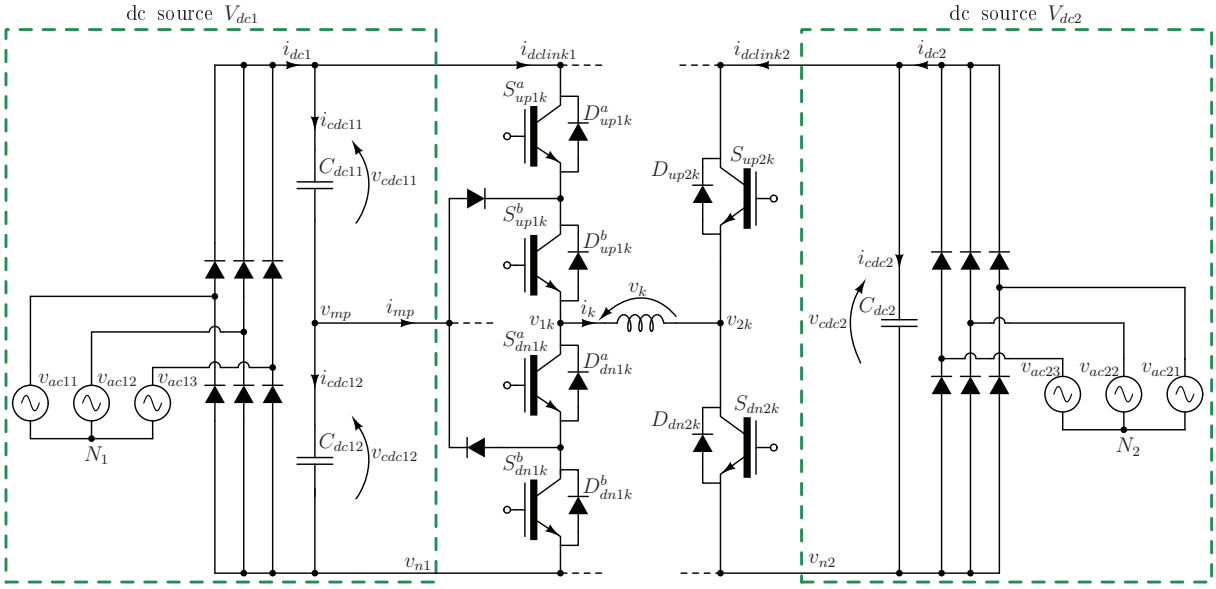


Fig. 5.13. Extended equivalent model for 3L-OeW-2L topology.

Analysis of Fig. 5.13 and (5.18) reveals the conditions under which all dc-link capacitor voltages are balanced. Currents i_{dc1} and i_{dc2} are always positive or zero, which means that sufficient condition for power sourcing from the dc to ac side of application is that $i_{dclink1}$ and $i_{dclink2}$ have positive mean values. This also ensures stable dc-link capacitor voltage on VSI_2 side, determined by the rest of the dc source circuitry. The situation is more complex on the VSI_1 side. This inverter is aimed to operate with three equidistant voltage levels (V_{dc1}, $v_{mp} = V_{dc1}/2$ and $v_{n1} = 0$), while switching is only allowed between adjacent levels, i.e. there should be no switching from V_{dc1} to 0 and vice versa. The desired dc-link voltage levels on VSI_1 side mean that the expected capacitor voltages are $v_{cdc11} = v_{cdc12} = V_{dc1}/2$. In this case, it is not sufficient to have positive $i_{dclink1}$ and $i_{dclink2}$, in order to ensure stable dc-link voltages. In addition, the i_{mp} mean value has to be zero over one fundamental period in order for v_{cdc11} and v_{cdc12} to be equal. This can also be concluded from the expressions for dc-link capacitors voltages, based on Fig. 5.13:

$$\begin{aligned} v_{cdc11}(t_2) &= \frac{1}{C_{dc11}}\int_{t1}^{t2}\left(i_{dc1}(t)-i_{dclink1}(t)\right)\cdot \mathrm{d}t + v_{cdc11}(t_1) \\ v_{cdc12}(t_2) &= \frac{1}{C_{dc21}}\int_{t1}^{t2}\left(i_{dc1}(t)-i_{dclink1}(t)-i_{mp}(t)\right)\cdot \mathrm{d}t + v_{cdc11}(t_1) \\ v_{cdc2}(t_2) &= \frac{1}{C_{dc2}}\int_{t1}^{t2}\left(i_{dc2}(t)-i_{dclink2}(t)\right)\cdot \mathrm{d}t + v_{cdc2}(t_1) \end{aligned} \tag{5.19}$$

In order to understand the 3L-OeW-2L drive dc-link capacitor voltage balancing it is sufficient to analyse $i_{dclink1}$, i_{mp} and $i_{dclink2}$. Relations between switching states and phase currents, with dc-link currents, obtained by analysis of inverter operation in Chapter 4 and using labels from Fig. 5.13, are:

$$\begin{aligned} i_{dclink1}(t) &= \sum_{k=1}^{5}\left(S_{1k}^{a}(t)\cdot S_{2k}^{b}(t)\cdot i_k(t)\right) \\ i_{mp}(t) &= \sum_{k=1}^{5}\left(\overline{S}_{1k}^{a}(t)\cdot S_{2k}^{b}(t)\cdot i_k(t)\right) \\ i_{dclink2}(t) &= \sum_{k=1}^{5}\left(S_{2k}(t)\cdot i_k(t)\right) \end{aligned} \tag{5.20}$$

where each switching state stands for one complete IGBT+D structure, while the bar over the symbol represents logical negation operation. Obtained expressions are more complex than those in (5.2) regarding VSI_1 dc-link currents, involving both switching states of NPC converter. The expression for VSI_2 dc-link current is the same as in the case of 2L-OeW-2L topology. However, careful analysis of switching patterns shows that S_{1k}^{a} and S_{1k}^{b} are never in PWM mode at the same time, at least for the analysed modulation strategies. The only situation when this is not the case is for six-level operation with $1 < r < 2$, which is eliminated from further analysis due to worse harmonic performance and the impact of very dominant dead-time spikes.

Although solving (5.20) can be simplified by splitting the analysis into several cases, which correspond to different reference zones, analytical calculations in the case of 3L-OeW-2L drive are more demanding and complex, when compared to the 2L-OeW-2L case, not only because of the more complex starting expressions, but also due to the fact that one of the conditions that should be met in order to have balanced dc-link capacitor voltages is more strict.

In the 2L-OeW-2L drive case it is sufficient to prove that all dc-link currents have positive mean values in order to demonstrate dc-link voltages' stability. In 3L-OeW-2L case, analysis of i_{mp} is of special interest, which requires consideration of the dead-time effects, since any asymmetry in switching pattern can lead to its non-zero mean value. In essence, this requirement is the reason why many single-sided multilevel topologies require special algorithms for dc-link

capacitors' voltage balancing. The dead-time influence on dc-link currents is already incorporated in (5.20), due to definitions of switching states. However, this fact does not make further analysis any easier, since the modulation algorithms presented in previous two chapters, have dead-time insertion as the last step in the switching pattern generation.

This means that expressions for duty ratios based on phase voltage reference manipulation have to be updated with an additional term that represents dead-time effects. This has no influence on $i_{dclink1}$ and $i_{dclink2}$, since positive mean values are of interest, which is the condition that has to be ensured by the modulation strategy itself, regardless of small side effects, such as those caused by dead-time. From this point of view, the analysis in the previous section is valid, although dead-time influence is not included in the linear drive model. This can be confirmed by the fact that the model provided accurate predictions of drive behaviour during experiments.

On the other hand, i_{mp} mean value is very sensitive to dead-time, but only when an asymmetrical switching pattern on VSI_1 low- and high-sides is commanded by the modulation strategy. Inclusion of dead-time in the models increases the overall complexity of the analysis, since some of the integration limits are now dependent not only on M and ϕ, but also on dead-time effects. Hence, in this section, only starting sets of equations are provided for each of the three configurations (r = 1, 2 and 4), modulated with coupled and decoupled schemes. Drive models, based on sinusoidal approximation and circuit linearization, are analysed only numerically.

5.3.2. LINEARIZED DRIVE MODEL AND SINUSOIDAL APPROXIMATION

The 3L-OeW-2L drive is analysed here using the same approach and model derivation arguments as in the previous section. Linearized drive model based on sinusoidal phase current approximation is shown in Fig. 5.14. An equivalent circuit, based on ideal transformers and (5.20) is shown in Fig. 5.15. Based on Figs. 5.14 and 5.15, expressions for dc-link current contributions from one drive phase are:

$$\begin{aligned} i_{dclink1k}(t) &= d_{1k}^{a}(t)\cdot i_k(t) \\ i_{mpk}(t) &= d_{mpk}(t)\cdot i_k(t) \\ i_{dclink2k}(t) &= -d_{2k}(t)\cdot i_k(t) \end{aligned} \tag{5.21}$$

where $d_{mpk}(t)$ stands for NPC mid-point duty ratio, which is calculated as:

$$d_{mpk}(t) = \begin{cases} 1-d_{1k}^{a}(t) & \text{if} \quad 1-d_{1k}^{a}(t) < d_{1k}^{b}(t) \\ d_{1k}^{b}(t) & \text{if} \quad 1-d_{1k}^{a}(t) \geq d_{1k}^{b}(t) \end{cases} \tag{5.22}$$

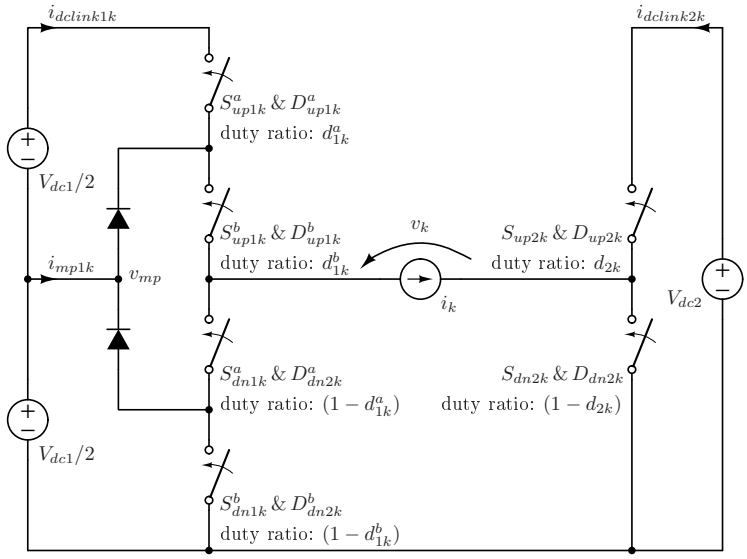


Fig. 5.14. Equivalent model of ideal 3L-OeW-2L topology under the sinusoidal approximation. For simplicity, only k^{th} drive phase is shown.

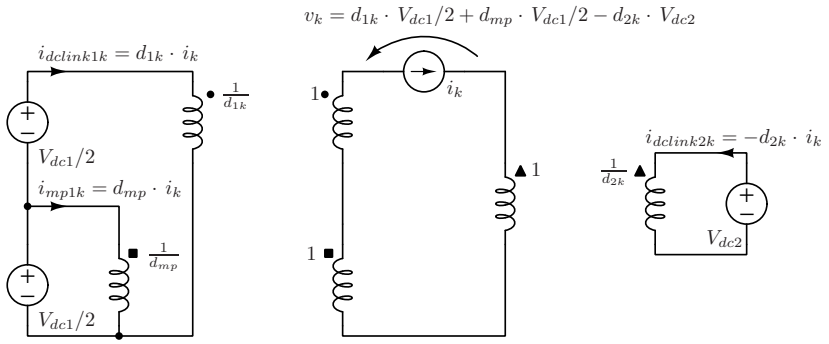


Fig. 5.15. Linearized equivalent model of ideal 3L-OeW-2L topology under the sinusoidal approximation.

In (5.21) and (5.22) d_{1k}^a and d_{1k}^b duty ratios correspond to S_{1k}^a and S_{1k}^b switching states, respectively. These two expressions form the complete drive model, which can be applied to any configuration (i.e. *r* value) and any modulation strategy. The only difference comes from the fact that duty ratios are calculated in a different manner. Phase current is in all these cases calculated using (5.5), while (5.6) provides the overall phase voltage reference, regardless of drive configuration and modulation strategy.

5.3.3. ANALYSIS FOR DC-LINK VOLTAGE RATIO 1:1

In this case ($r = 1$), duty ratios are calculated using phase voltage reference and expressions (4.4). As already mentioned, the expressions are aimed for numerical analysis of dc-link currents. Considering this, instead of using a time domain condition based on reference intersections with normalised equivalent voltage levels, it seems sufficient to express duty ratios in different reference zones, which in the numerical model comes down to simple *if-then-else* conditional statements. These are summarised in Tables 5.3 and 5.4, for coupled and decoupled modulation, respectively. Normalised voltage levels are $l_1 = 0$, $l_2 = 1/4$, $l_3 = 1/2$, $l_4 = 3/4$ and $l_5 = 1$ (Figs. 4.3b, 4.6a and 4.7a). Using expressions (5.21) and (5.22) and Tables 5.3 and 5.4, one is able to calculate dc-link current values for every time instant in one fundamental period. Obtained waveforms are shown in Figs. 5.16 and 5.17. In the case of coupled modulation (Fig. 5.16), low- and high-side PWMs of VSI_1 are not symmetrical, while VSI_2 operates in PWM mode in only one reference zone. Both $i_{dclink1}$ and $i_{dclink2}$ clearly have more positive than negative instantaneous values during one fundamental period. This means that the overall dc-link voltages are not going to be increased, even if current unidirectional dc sources are used, like those in Fig. 5.13. Surprisingly, asymmetry on the VSI_1 side does not affect i_{mp}, which is symmetrical and has zero mean value during one fundamental period, regardless of *M* and ϕ. Careful analysis of d_{1k}^a and d_{1k}^b shows that d_{mpk} has purely sinusoidal waveform although d_{1k}^a and d_{1k}^b do not. However, this finding is not in agreement with observations made during experimental verification, to be presented further on, where separate control of v_{mp} and V_{dc1} is required to provide stable voltage levels on VSI_1 side. In this case, i_{mp} has a strictly negative mean value.

Table 5.3. Duty ratio calculations for 3L-OeW-2L five-level configuration and coupled PWM methods.

Condition	d_{1k}^a	d_{1k}^b	d_{2k}
$l_1 \le v_k^*(t) \le l_2$	0	$4\cdot(v_k^*(t) - l_1)$	1
$l_2 < v_k^*(t) \le l_3$	0	$4\cdot(l_3 - v_k^*(t))$	$4\cdot(l_3 - v_k^*(t))$
$l_3 < v_k^*(t) \le l_4$	0	$4\cdot(v_k^*(t) - l_3)$	0
$l_4 < v_k^*(t) \le l_5$	$4\cdot(v_k^*(t) - l_4)$	1	0

Table 5.4. Duty ratios for 3L-OeW-2L five-level configuration and decoupled PWM methods.

Condition	d^a_{1k}	d^b_{1k}	d_{2k}
$0 \le v^*_k(t) \le 1/2$	$2\cdot(v^*_{1k}(t) - 1/2)$	1	$v^*_{2k}(t)$
$1/2 < v^*_k(t) \le 1$	0	$2\cdot v^*_{1k}(t)$	$v^*_{2k}(t)$

Comparison of simulation results with and without dead-time effects shows that dead-time is responsible for what is observed in practice. Hence, the linearized model, based on sinusoidal approximation, is updated with an additional term for each duty ratio, which represents the difference between commanded duty ratio (Tables 5.3 and 5.4) and actually produced one, after dead-time implementation. Since the dead time interval in experimental rig is $t_{d\text{-}t} = 6$ μs, while the switching period is $T_S = 500$ μs, duty ratios d^a_{1k} and d^b_{1k} have to be updated with $-6/500\cdot\text{sign}(i_k)$ while d_{2k} has to be corrected with $+6/500\cdot\text{sign}(i_k)$ in order to include dead-time effects in the model (sign(x) function returns –1 for $x < 1$ and 1 for $x \ge 0$). This modification has no influence on $i_{dclink1k}$ and $i_{dclink2k}$ as well as on $i_{dclink1}$ and $i_{dclink2}$ mean values. However, it has a strong influence on i_{mp} mean value, when coupled control of two inverters is utilised.

In the case of decoupled modulation schemes, obtained waveforms for $i_{dclink11}$ and $i_{dclink21}$ are always positive for a longer period of time during one fundamental period, which indicates corresponding dc-link currents have positive mean values, regardless of M and ϕ values (Fig. 5.17). Waveforms obtained for i_{mp11} are always symmetrical around zero, since VSI_1 performs symmetrical three-level operation at all times, as a part of the decoupled modulation scheme proposed in Chapter 4.

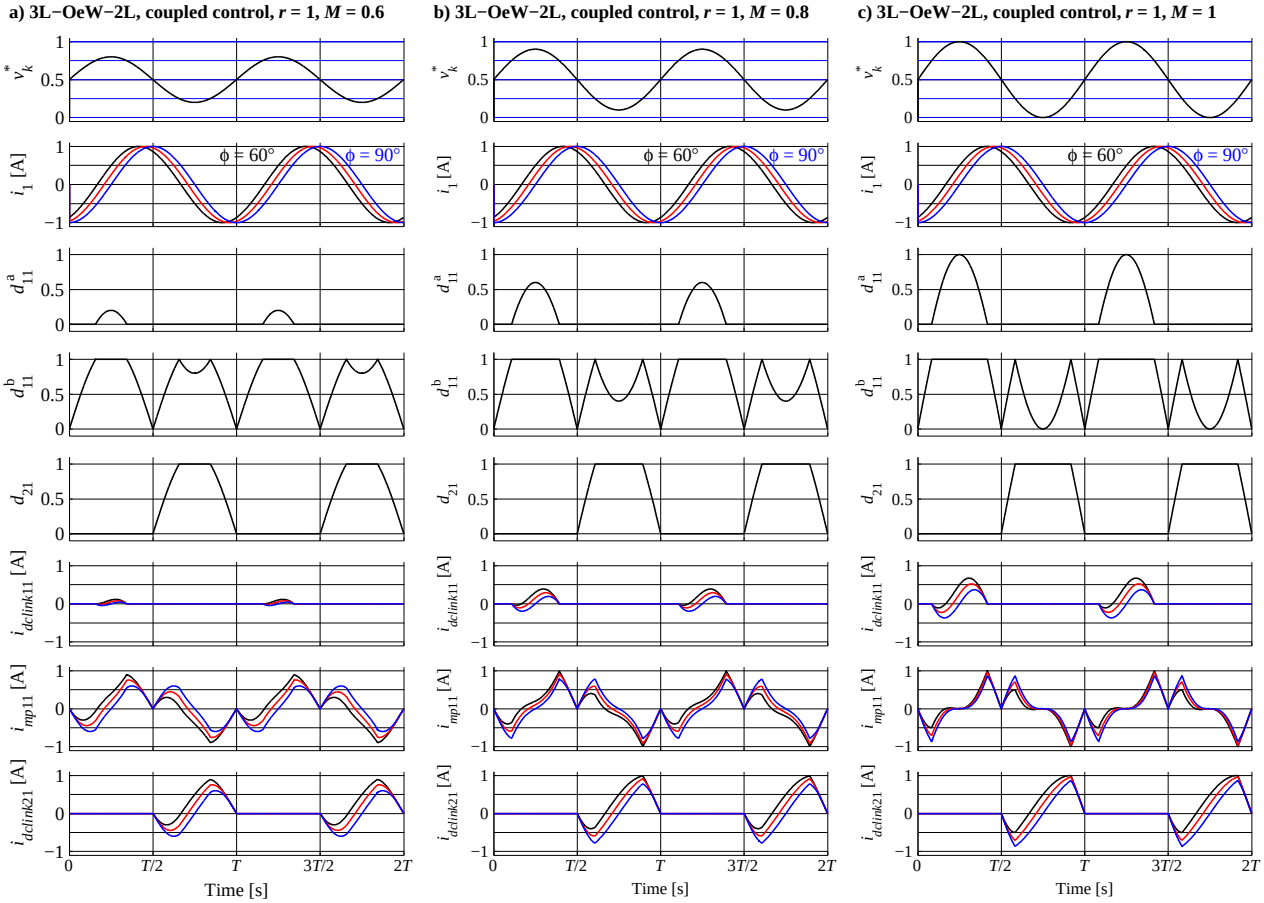


Fig. 5.16. Waveforms obtained using the model in Fig. 5.14 and coupled modulation for $r = 1$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

Results in Fig. 5.18 show dc-link currents' mean values with respect to phase angle, calculated using duty ratios after dead-time effects are included. As expected, if coupled control is used, there is a non-zero i_{mp} mean value, even for the purely inductive load (ϕ = 90 degrees), while dead-time effects are cancelled out due to symmetrical switching in the case of decoupled control.

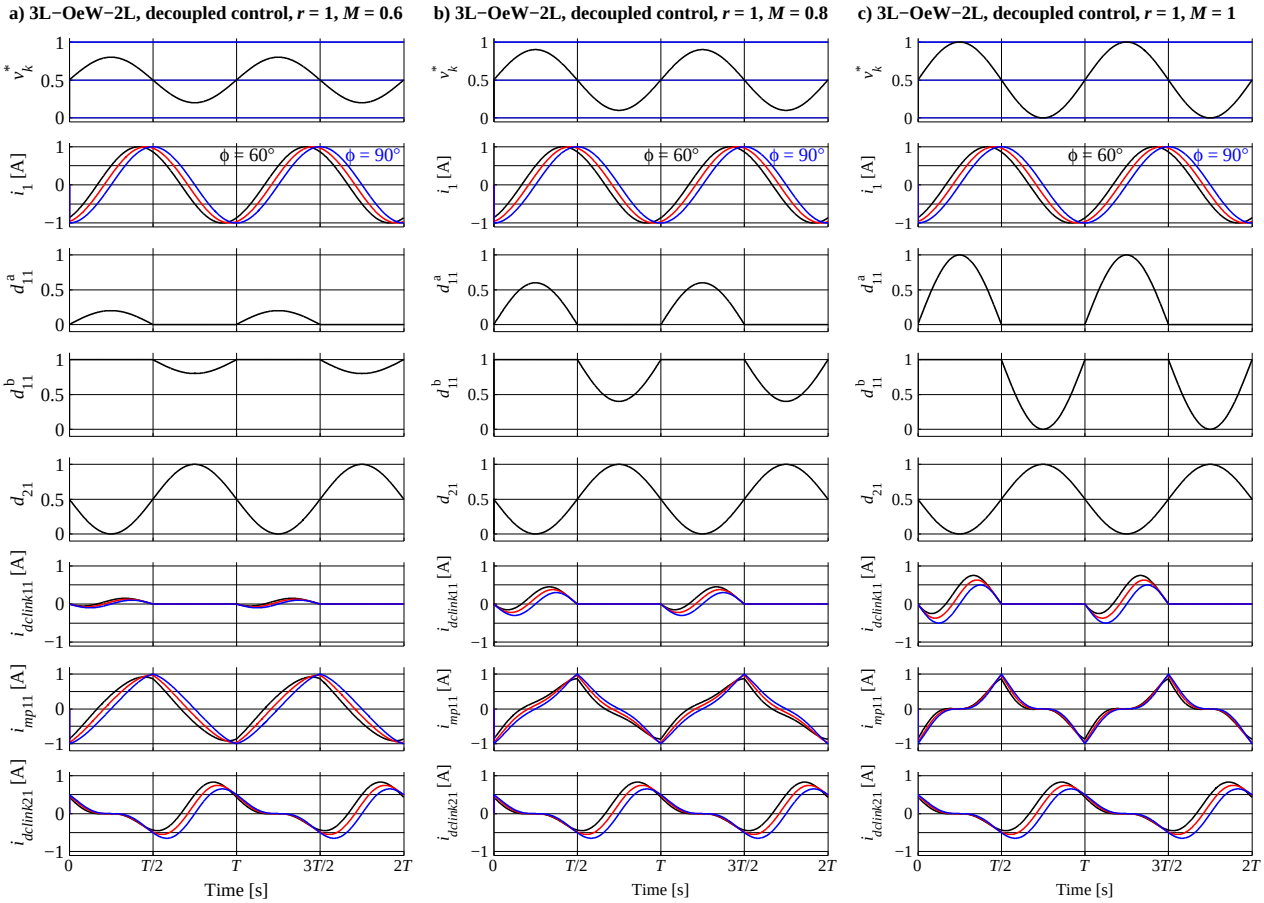


Fig. 5.17. Waveforms obtained using the model in Fig. 5.14 and decoupled modulation for r = 1, ϕ = 60°, 75° and 90° (black, red and blue lines, respectively) and M = 0.6 (a), M = 0.8 (b) and M = 1 (c).

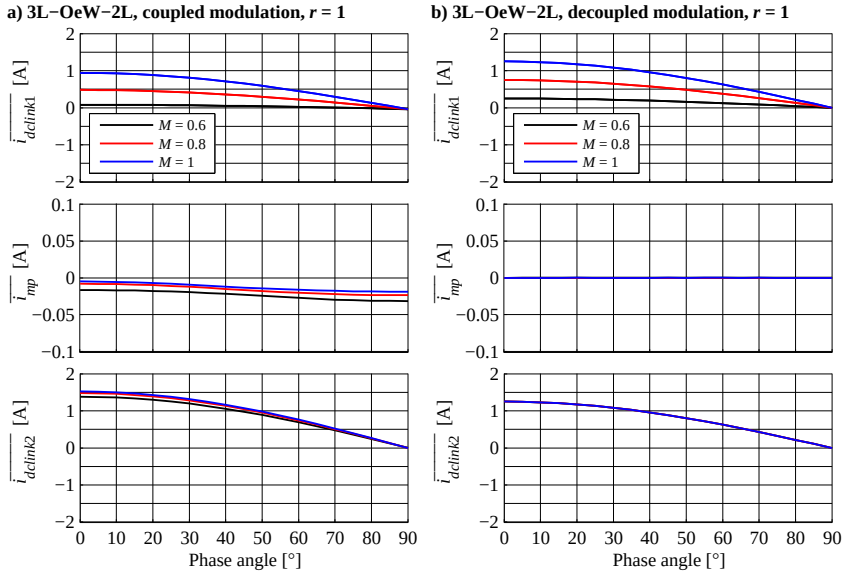


Fig. 5.18. Phase angle influence on the dc-link current mean values in the case of 3L-OeW-2L five-level configuration with coupled (a) and decoupled (b) modulation, with included dead-time effects.

5.3.4. ANALYSIS FOR DC-LINK VOLTAGE RATIO 2:1

In this case (r = 2), which is referred to as a four-level configuration in Chapter 4, duty ratios are calculated using simpler expressions. All three complementary pairs of switches (S^a_{1k}, S^b_{1k} and S_{2k}) are equally and symmetrically used during one fundamental period (in multilevel operation). Normalised voltage levels are $l_1 = 0$, $l_2 = 1/3$, $l_3 = 2/3$ and $l_4 = 1$ (Figs. 4.3b, 4.6c and 4.7c). This leads to completely stable dc-link voltages, which is observed during experimental verification of the proposed modulation strategies in Chapter 4. Here, analysis of dc-link currents is used to confirm these findings and to investigate if any phase angle and modulation index value can lead to dc-link capacitor voltage balancing problems. Duty ratios expressions, based on (4.5) under the assumption of infinite switching frequency are summarised in Table 5.5. Results are shown in Figs. 5.19 and 5.20. Waveforms shown in Fig. 5.19 lead to a conclusion that $i_{dclink1k}$ and $i_{dclink2k}$ have positive mean values. Contrary to the previously analysed configuration with coupled modulation, study of d^a_{1k} and d^b_{1k} waveforms in Fig. 5.19 shows that d_{mpk} has a symmetrical waveform in this case. Duty ratios are updated with $-6/500 \cdot \text{sign}(i_k)$, but contributions of $(1 - d^a_{1k})$ and d^b_{1k} to d_{mpk} are equal, which eliminates dead-time influence on the i_{mp} mean value.

Table 5.5. Duty ratio calculations for the 3L-OeW-2L four-level configuration and coupled PWM methods.

Condition	d^a_{1k}	d^b_{1k}	d_{2k}
$l_1 \le v^*_k(t) \le l_2$	0	$3\cdot(v^*_k(t) - l_1)$	1
$l_2 < v^*_k(t) \le l_3$	0	1	$3\cdot(l_2 - (v^*_k(t))$
$l_3 < v^*_k(t) \le l_4$	$3\cdot(v^*_k(t) - l_3)$	1	0

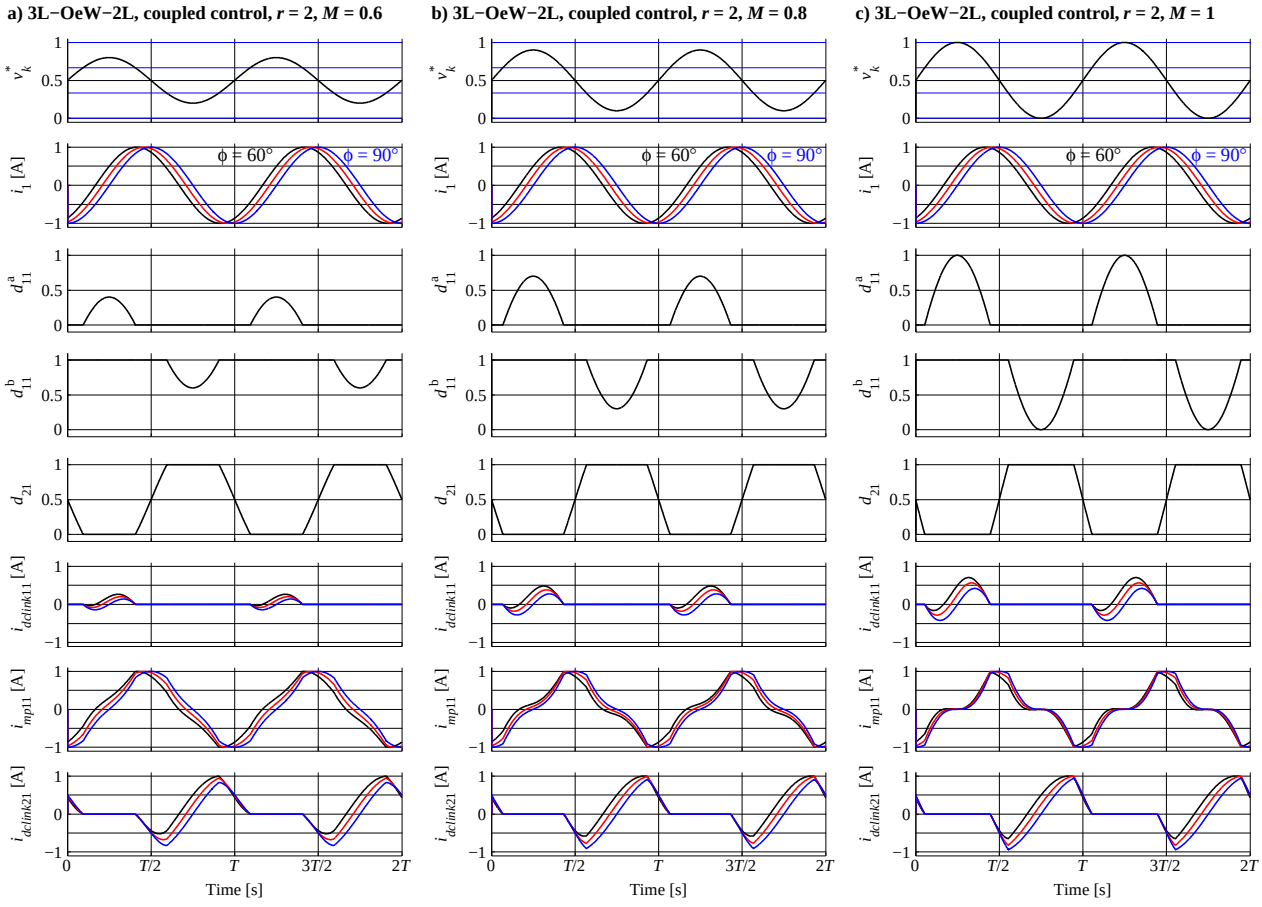


Fig. 5.19. Waveforms obtained using the model in Fig. 5.14 and coupled modulation for r = 2, ϕ = 60°, 75° and 90° (black, red and blue lines, respectively) and M = 0.6 (a), M = 0.8 (b) and M = 1 (c).

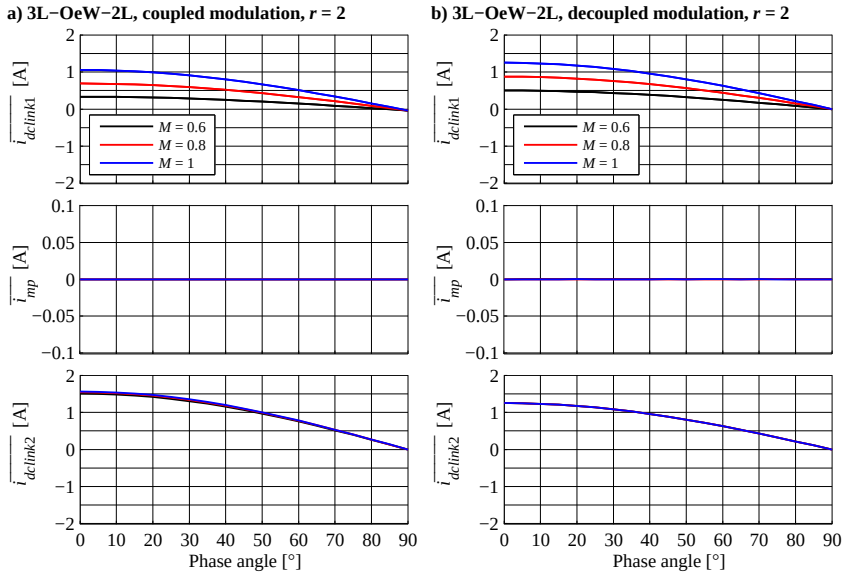


Fig. 5.20. Phase angle influence on the dc-link current mean values for a 3L-OeW-2L four-level configuration (r = 2) with coupled (a) and decoupled (b) modulation.

Duty ratio expressions for decoupled modulation are the same as in Table 5.2. As already stated in Chapter 4, decoupled modulation is in essence the same for any dc-link voltage ratio, which only has influence on the border between two-level and multilevel PWM operation. Hence, obtained waveforms in this case are almost identical with those in Fig. 5.17. The only difference is in somewhat lower M_1. Since $M_2 = 1$, $i_{dclink2k}$ is identical in all cases.

Phase angle influence on dc-link currents, for several values of modulation index, and for both coupled and decoupled methods, is depicted in Fig. 5.20. Current i_{mp} has a mean value equal to zero with both modulation methods, while all other dc-link currents have always positive mean values. This means that the 3L-OeW-2L drive with r = 2 is suitable for both coupled and decoupled VSI_1 and VSI_2 control.

5.3.5. ANALYSIS FOR DC-LINK VOLTAGE RATIO 4:1

With r = 4, the 3L-OeW-2L drive is able to produce six equidistant voltage levels. Their normalised values are $l_1 = 0$, $l_2 = 1/5$, $l_3 = 2/5$, $l_4 = 3/5$, $l_5 = 4/5$ and $l_6 = 1$ (Figs. 4.3b, 4.6d and 4.7d). As shown in Chapter 4, this drive configuration employs VSI_2 in every reference zone. VSI_1 performs low-side PWM switching in reference zone 2 and high-side PWM in reference zone 4. This kind of operation is required, since transitions between $l_2 - l_3$ and $l_4 - l_5$ can be performed only with simultaneous switching on both OeW sides. Similarly to the case of 2L-OeW-2L four-level configuration, this kind of modulation causes not only dead-time spikes, but also capacitor balancing problem on lower dc-link voltage side. Duty ratios for coupled modulation methods are listed in Table 5.6. Using (5.21) and (5.22) contributions of each drive phase to the overall dc-link currents are obtained. Obtained waveforms for the first drive phase are shown in Fig. 5.21, while Fig. 5.22 shows dc-link current mean values for coupled and decoupled modulation.

Table 5.6. Duty ratio calculations for 3L-OeW-2L four-level configuration and coupled PWM methods.

Condition	d^a_{1k}	d^b_{1k}	d_{2k}
$l_1 \le v^*_k(t) \le l_2$	0	0	$5\cdot(1 - v^*_k(t))$
$l_2 < v^*_k(t) \le l_3$	0	$5\cdot(v^*_k(t) - l_2)$	$5\cdot(v^*_k(t) - l_2)$
$l_3 < v^*_k(t) \le l_4$	0	1	$5\cdot(l_4 - v^*_k(t))$
$l_4 < v^*_k(t) \le l_5$	$5\cdot(v^*_k(t) - l_4)$	1	$5\cdot(v^*_k(t) - l_4)$
$l_5 < v^*_k(t) \le l_6$	1	1	$5\cdot(l_6 - v^*_k(t))$

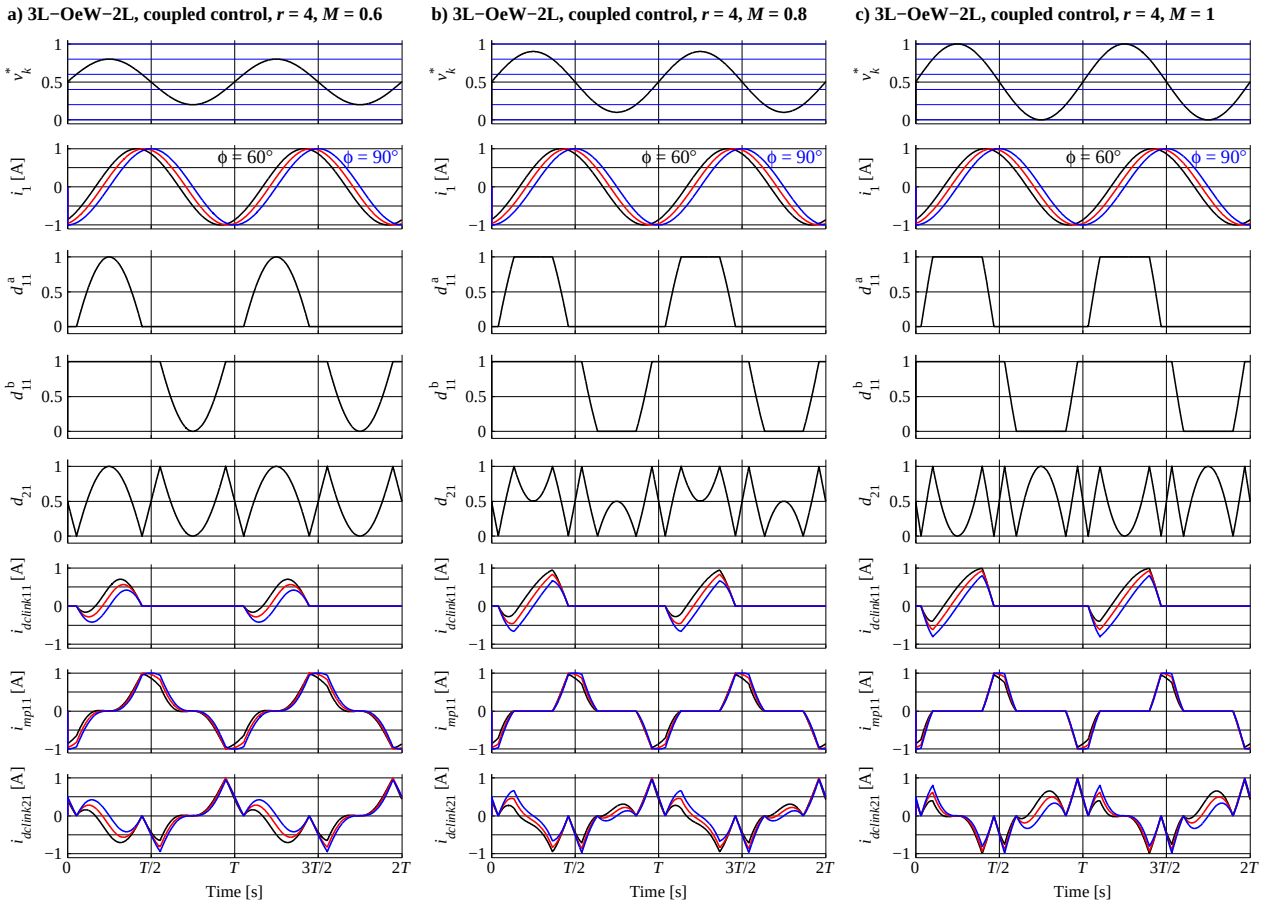


Fig. 5.21. Waveforms obtained using the model in Fig. 5.14 and coupled modulation for $r = 4$, $\phi = 60°$, 75° and 90° (black, red and blue lines, respectively) and $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

Due to symmetrical operation of the low- and high-sides of VSI_1, i_{mpk} negative and positive parts are symmetrical, regardless of M and ϕ. Operation of VSI_1 high-side also ensures that $i_{dclink1k}$ always has a positive mean value. Situation on the VSI_2 side is more complex, since this inverter operates in all reference zones in PWM mode. For some M values, this leads to an overcharging, which can be seen from the $i_{dclink21}$ waveform in Fig. 5.21, for $M = 0.6$ and 0.8. In this case, the lower M value for which $i_{dclink2}$ becomes negative is not equal to the border between single-sided and multilevel operation (i.e. $M = 0.2$). Detailed numerical analysis shows that this phenomenon takes place for $0.495 < M < 0.901$, regardless of the phase angle.

The same analysis is performed for decoupled modulation methods, modified for this configuration. Again, duty ratios for this case can be obtained using Table 5.4. Hence, obtained waveforms are almost identical to those in Fig. 5.17. Phase angle influence on dc-link currents for both coupled and decoupled control is shown in Fig. 5.22. Results demonstrate that coupled modulation leads to the overcharging problem, while phase angle influence on the $i_{dclink2}$ amplitude is similar to that shown in Fig. 5.9.

Although the modulation index range in which the 3L-OeW-2L drive with $r = 4$ suffers from overcharging problem is somewhat smaller, when compared to the 2L-OeW-2L with $r = 2$, it is clear that this represents a huge drawback. When compared to other 3L-OeW-2L configurations ($r = 1$ and $r = 2$) it is clear that the overall drive performance is not greatly improved by utilising one additional voltage level, while the overcharging problem leads to additional energy losses and/or increases hardware complexity. In other words, this configuration (3L-OeW-2L with $r = 4$) may have great practical significance for applications in which the machine is aimed to operate with constant speed most of the time.

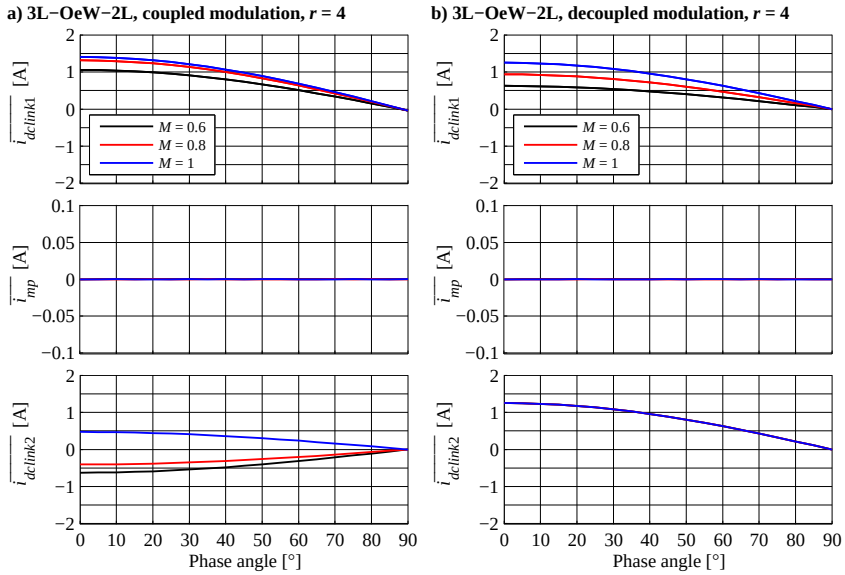


Fig. 5.22. Phase angle influence on the dc-link current mean values for a 3L-OeW-2L six-level configuration (r = 4) with coupled (a) and decoupled (b) modulation.

5.3.6. SIMULATION AND EXPERIMENTAL RESULTS

The findings reported in this section are obtained via simulation of the extended drive model, which includes dc sources based on three-phase diode rectifies with suppressed output voltage ripple, as shown in Fig. 5.13. Results are presented in Figs. 5.23 and 5.24, for PD PWM and URS1 PWM, respectively. Ideal dc sources are used during acceleration until shortly after steady state is reached, at t = 0.5 s, when they are replaced with diode rectifiers and dc-link capacitors, modelled according to Appendix 1. In the case of the five-level configuration (r = 1), modulated with PD PWM, this change of dc source type immediately leads to VSI_1 mid-point voltage level increment, which ruins the modulation performance. At the same time, it is clear that voltage across the low-side dc-link capacitor (C_{dc12}) is increased. Although the VSI_1 overall dc-link voltage remains the same, the overcharging mechanism leads to several important issues. It affects not only the low-side capacitor bank design (it has to be able to withstand V_{dc1} instead of $V_{dc1}/2$), but also semiconductor choice, since maximal blocking voltage can be twice higher than usual. This reinforces the impression from Chapter 4: the 3L-OeW-2L with r = 1 does not seem to be beneficial for high-power drives, where both blocking voltage and current conduction capabilities of all semiconductor devices are maximally exploited. Further detailed studies of simulation results based on the drive models with and without dead-time confirm that dead-time is the main reason for non-zero i_{mp} mean value.

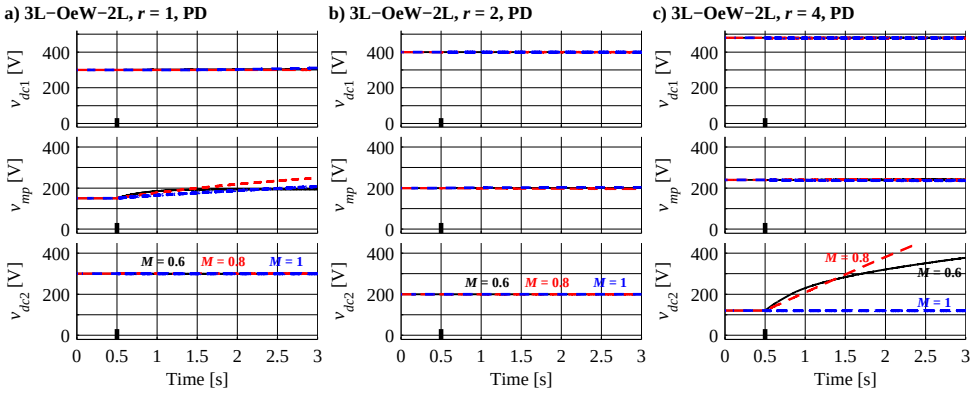


Fig. 5.23. Simulation results: 3L-OeW-2L drive dc-link voltages for PD PWM r = 1 (a), r = 2 (b) and r = 4 (c).

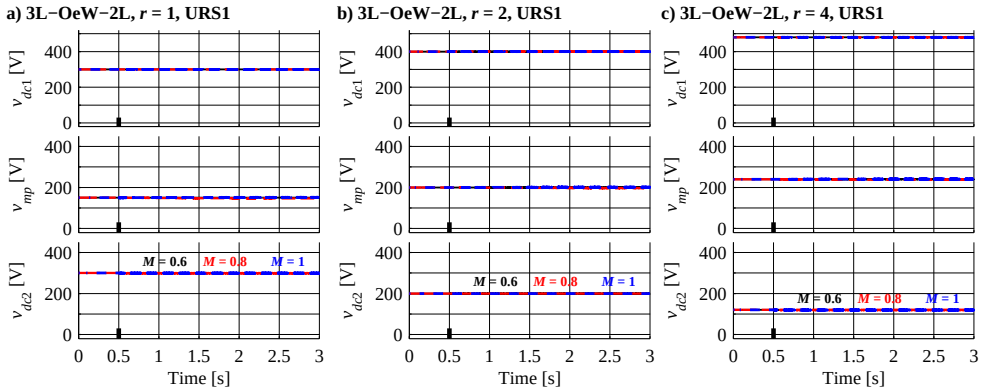


Fig. 5.24. Simulation results: 3L-OeW-2L drive dc-link voltages for URS1 PWM $r = 1$ (a), $r = 2$ (b) and $r = 4$ (c).

The four-level configuration ($r = 2$) does not suffer from any dc-link capacitor voltage balancing problems. As expected, application of PD PWM to the six-level configuration results in an increase of V_{cdc2}, since $i_{dclink2}$ is negative, while i_{dc2} can only be positive. Fig. 5.24 shows that decoupled PWM methods keep dc-link voltages balanced in all configurations.

The influence of unbalanced voltage levels on produced phase voltages and currents is shown in Figs. 5.25 and 5.26. Comparison of these two cases leads to a conclusion that the five-level configuration ($r = 1$) with coupled modulation methods leads to drastic harmonic pollution, which is a direct consequence of v_{mp} increase, since this voltage level is used in every switching period, for final phase voltage formation. Due to a non-zero i_{mp} mean value, even in the case of $M = 1$, the drive suffers from high current harmonic distortion.

Six-level configuration ($r = 4$) waveforms in Fig. 5.26 are highly polluted when $M = 0.6$ and 0.8 with low-order harmonic content, which also comes from the fact that the modulation strategy is designed for a dc-link voltage ratio of 4:1, while dc-link voltages are not in that ratio. Similarly to the case of the 2L-OeW-2L drive with $r = 2$, the overcharging problem does not exist for nominal modulation index value. Overcharging rates depicted in Fig. 5.23c are not in agreement with model based findings from the previous subsection. Overcharging rate for $M = 0.8$ is higher than for $M = 0.6$, as a consequence of additional current components. Phase currents amplitudes are increased in Fig. 5.26, which is the consequence of using modulation strategy developed for dc-link voltage ratio 4:1 ($V_{dc1} = 480$ V and $V_{dc2} = 120$ V), while V_{dc2} eventually becomes greater than $v_{mp} = V_{dc1}/2$. These findings are confirmed experimentally, by performing the same kind of acceleration tests under *V/f* control, under no load, as in the case of 2L-OeW-2L drive. Results are shown in Fig. 5.27.

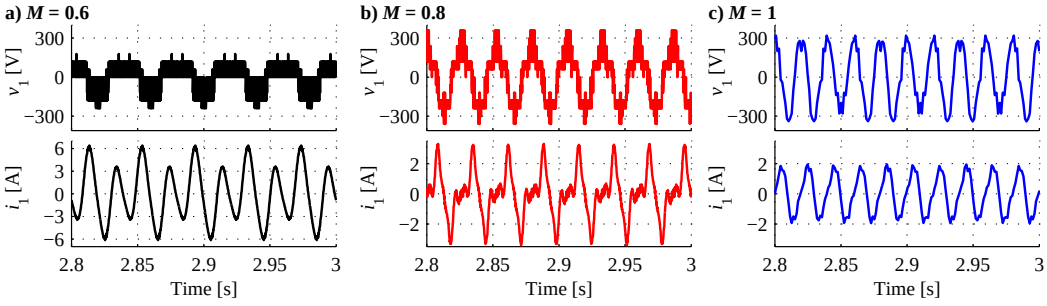


Fig. 5.25. Simulation results: 3L-OeW-2L drive with PD PWM, $r = 1$ steady state v_1 and i_1 for $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

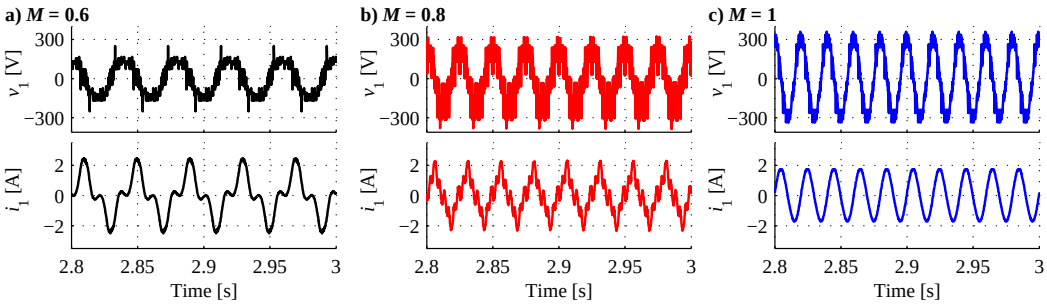


Fig. 5.26. Simulation results: 3L-OeW-2L drive with PD PWM, $r = 4$ steady state v_1 and i_1 for $M = 0.6$ (a), $M = 0.8$ (b) and $M = 1$ (c).

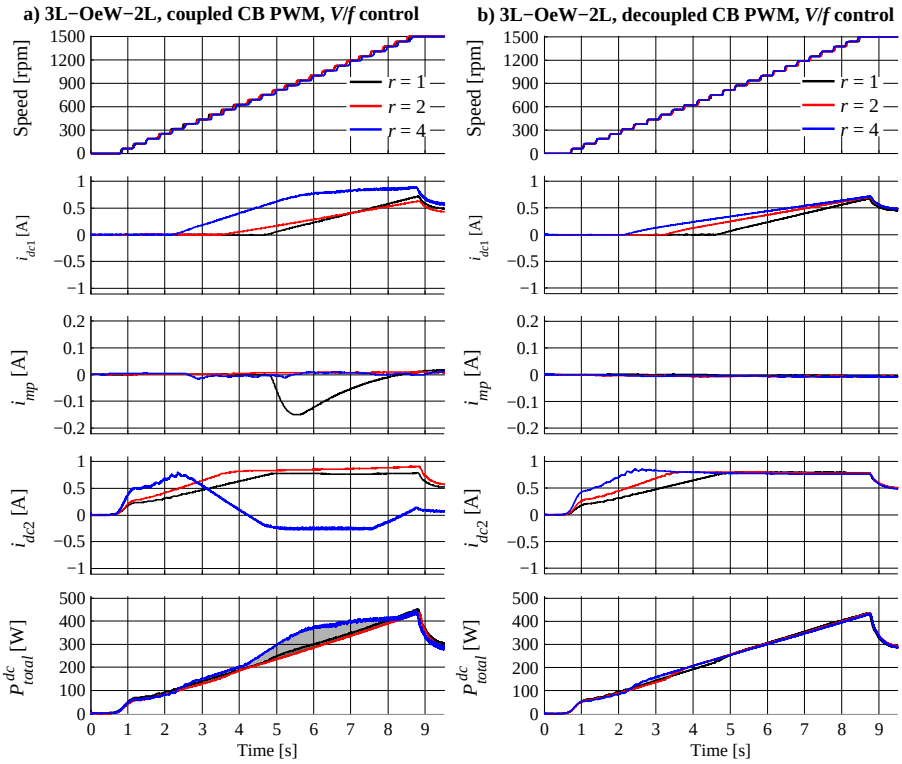


Fig. 5.27. Experimental results: 3L-OeW-2L dc-link currents and total drive power during *V/f* acceleration, for PD PWM (a) and URS1 PWM (b) with $r = 1$, $r = 2$ and $r = 4$.

Regarding coupled control, it is clear that $r = 2$ results in optimal energy consumption, while in the two other cases ($r = 1$ and $r = 4$) additional energy losses can be observed. For the case of $r = 1$, two controllable dc sources are used on VSI_1 side, connected in series, between the lower dc-link rail and v_{mp} (low-side $V_{dc1}/2$) and between v_{mp} and the upper dc-link rail (high-side $V_{dc1}/2$). Three-level single-sided modulation is used for $0 < M < 0.5$. The drive enters five-level operation mode at one half of the full speed range, which immediately causes negative mid-point current. In order to keep $v_{mp} = V_{dc1}/2$, somewhat more energy is needed. Energy losses in this case come from asymmetrical use of low- and high-side dc sources, meaning that they do not have the same output currents, which leads to minimal increment in the overall power consumption (expected, due to very small value of i_{mp}).

In the case of $r = 4$, VSI_1 naturally keeps its voltage levels balanced, due to symmetrical low- and high-side PWM operation. However, coupled modulation leads to overcharging on VSI_2 side. The modulation results in negative $i_{dclink2k}$ mean value over one fundamental period, for any phase angle lower than 90°. Experimental results for decoupled PWM methods (Fig. 5.27b) show that drive operates with naturally balanced dc-link voltages for all three values of r.

5.4. SUMMARY

This chapter deals with dc-link capacitor voltage balancing in open-end winding drives. In particular, the ability to naturally balance dc-link voltages under the modulation strategies presented in the previous two chapters is analysed. It has been shown that in some cases coupled PWM methods suffer from different sorts of dc-link capacitors' voltage balancing issues.

For the purpose of this analysis, both drives are modelled using a sinusoidal approximation of phase currents. Models are further simplified assuming almost infinite switching frequency, i.e. linear change of switch duty ratios. This enables derivation of analytical expressions for dc-link current mean values in the case of 2L-OeW-2L drive, which is then analysed for each configuration and corresponding modulation strategies. It is shown that the capacitor voltage overcharging phenomenon occurs at the VSI_2 side when dc-link voltages in the ratio of 2:1 are used, but only if coupled modulation methods are applied. As a consequence, the harmonic performance is far from expected. At the same time, this may lead to capacitor bank overvoltage and/or VSI_2 semiconductors damage, due to their limited voltage blocking ability. The same drive does not suffer from any dc-link voltages stability issues if decoupled modulation methods are used. This conclusion applies for both analysed configurations, i.e. for dc-link voltages in ratio 1:1 and 2:1.

The same kind of model is derived for the case of 3L-OeW-2L drive. Due to its increased complexity, this drive is analysed only numerically, in order to find the reasons for the dc-link capacitor voltage instability encountered when certain modulation strategies are utilised. This topology tends to operate with unstable dc-link capacitor voltages, if coupled control of five- and six-level configurations with equidistant voltage levels is used. In the first case, the problem exists on the VSI_1 side, where NPC inverter mid-point voltage tends to decrease, due to commanded switching actions by the modulation strategy. It is shown that this case is specific, since dc-link capacitor voltage unbalance actually comes as a consequence of asymmetrical low- and high-side PWM operation of the NPC inverter. Only in this case, dead-time effects on switching pattern lead to non-zero mid-point current mean value, which causes low-side dc-link capacitor discharging. In the second case ($r = 4$) VSI_2 dc-link voltage capacitor can be overcharged for the same reasons as in the case of the 2L-OeW-2L with $r = 2$.

These findings are compared against detailed simulation and experimental results, which confirm the validity of the proposed modelling approach, for both analysed drives. It is shown that overcharging always leads to additional energy losses or the necessity of having controllable current bidirectional dc-link voltage source at low dc-link voltage side. This additional hardware complexity and great reduction of efficiency can only be avoided by using simple, decoupled control, which leads to worse harmonic performance and potentially higher losses. Only in the cases when the drive operates at its nominal speed, or very close to it, the overcharging problem is eliminated naturally. This opens a possibility to utilise coupled PWM methods in high-power applications where drive is aimed to operate at constant speed most of the time, since superior harmonic performance, leading to minimal torque ripple, is in this case guaranteed, as well as dc-link voltages stability. For variable speed drives, it seems more appropriate to use other dc-link voltage ratios and modulation methods with suboptimal harmonic performance.

Chapter 6

OPEN-END WINDING DRIVES WITH A SINGLE DC VOLTAGE SOURCE AND ISOLATED INVERTERS

6.1. INTRODUCTION

As explained in Chapter 1, open-end winding drives offer several advantages, when compared to single-sided supplies in terms of control and fault tolerance. At the same time, the OeW concept leads to a reduced component count at the dc to ac conversion stage. However, organisation of the dc power supply for OeW drives leads to potential drawbacks, which often limit the applicability of this concept. The proposed topologies require dc-link isolation, in order to eliminate the zero-sequence current flow path. On the other hand, isolation allows the dc-link voltage ratio to be used as an additional degree of freedom in order to increase the total number of voltage levels [Corzine et al. (2004), Darijevic et al. (2015a)]. Since two isolated dc sources are required, the total number of power devices is lower, but still similar as in the case of equivalent single-sided solutions, meaning that savings in hardware complexity and cost are not high. In some cases [Bodo (2013), Nian et al. (2016)], non-isolated dc-links are used, while zero-sequence current circulation is supressed using the modulation strategy. The usage of a single dc source that supplies both inverters usually leads to a reduced number of voltage levels. In other words, phase voltage and current waveform quality are traded for circuit complexity.

From the point of view of hardware organisation, drives can be classified in two major groups. In the first one, the inverter(s) and machine are close to each other. This, integrated drive structure, leads to much shorter ac transmission lines between inverter housing and machine terminals. Thus, expected copper cost for single-sided and open-end winding drives is similar, while the latter solution relies on simpler inverter structures, reducing the component count and increasing the reliability and fault tolerance. This kind of drive configuration has gained a lot of interest in modern industrial and especially automotive applications, leading to compact solutions in which machine, ac-dc and dc-ac converters are packed together. In other cases, power electronic converters cannot be installed close to the machine, due to some physical limitations of the system (often related to the mechanical part of the application). Since dc rails between ac-dc and dc-ac stages of the drive have to be kept as short as possible (due to parasitic effects and the high cost of the dc bus-bars), the only option for these, so-called distributed drive structures, is to make ac cables long enough to reach from the inverter(s) to the machine. For these applications, the open-end winding drive concept is not a good option, because of the additional cable cost. In the drives where ac lines are several tens of meters, the overall cost of cables overwhelms the cost of additional components required for a single-sided solution with the same number of levels and power rating. At the same time, the OeW configurations with dual dc source supplies require two mutually isolated supplies and therefore additional magnetic components, which are heavy and expensive, due to the current and voltage ratings associated with high-power applications. Although realisation of dc sources in EVs can be based on two isolated battery packs, existence of two dc sources still has some drawbacks, related to the battery charging process.

An alternative open-end winding topology, which combines features of isolated topologies and those with single dc-source is introduced in [Corzine et al. (2004), Corzine et al. (2006)] for a three-phase drive. On one OeW side, a three-level inverter with a low switching frequency is used for supplying the bulk of the machines power needs. The

other side of the windings is connected to the so-called conditioning inverter, capable of high frequency switching. This inverter is isolated but it does not have an independent voltage supply for dc-link formation. Instead, the modulation strategy is designed to maintain a constant dc-link capacitor voltage. This concept has been applied to different drive configurations [Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)] in conjunction with SV PWM.

In this chapter, a novel five-phase single dc source supplied OeW topology with isolated inverters is presented. In Section 6.2 two OeW drive configurations are analysed for the case when both VSIs are supplied using independent and isolated dc sources, but using a modified CB PWM method, referred to as modified PD PWM. In particular, this modification is possible only if the inverters in OeW configuration do not operate in PWM mode at the same time. This implies that only 2L-OeW-2L with $r = 1$ and 3L-OeW-2L with $r = 2$ are suitable for the proposed control concept. Contrary to the conventional PD PWM, the proposed modulation performs PWM switching of one inverter only, while the other operates in staircase mode. Simulation results show that, for both topologies, this modification leads to operation equivalent to PD PWM for the same drive configuration, but offers a possibility to eliminate the active dc source at the PWM switching inverter side.

This feature is analysed in Section 6.3. The inverter that operates in staircase mode is referred to as the bulk inverter, since it supplies the drive with the majority of the required active power. The inverter that operates in PWM mode is named the conditioning inverter, since its main role is to suppress the low order harmonics produced by the bulk inverter. This requires some modifications of the modulation strategy, when compared to previously presented modulation methods, which relies on PWM operation of both inverters in order to produce the desired phase voltage fundamental and to suppress unwanted harmonic content. Analysis shows that introduction of the closed-loop control of the conditioning inverter dc-link voltage offers a possibility to maintain the drive performance. Furthermore, it is demonstrated that this can be done even without an increase of the remaining active dc source voltage. This feature is known as dc voltage supply boosting in OeW drives [Ewanchuk et al. (2013)]. The proposed control is here referred to as bulk and conditioning (B&C) CB PWM, indicating that VSI_1 and VSI_2 perform the functions similar to those presented in [Corzine et al. (2004), Corzine et al. (2006)]. Simulation results demonstrate that elimination of one dc source does not lead to any significant drawbacks in the 2L-OeW-2L drive case, while 3L-OeW-2L drive is able to deliver expected harmonic performance with a single dc source. Hence, this configuration gained more attention and preliminary results are presented in [Darijevic et al. (2015c)].

6.2. MODIFIED PD PWM

6.2.1. PRELIMINARY ANALYSIS

It is shown in Chapters 3 and 4 that the 2L-OeW-2L and 3L-OeW-2L topologies have only one configuration in which two inverters never operate at the same time in PWM mode. This is the case if 2L-OeW-2L drive is supplied from equal dc-link voltages ($r = 1$), which leads to three-level configuration, and for 3L-OeW-2L drive with $r = 2$ (four-level configuration). These configurations lead to the lowest number of voltage levels (in multilevel operation), when compared to any other dc-link voltage ratio, applied to the same drive. However coupled modulation does not cause any problems related to dead-time spikes (Chapters 3 and 4) or dc-link capacitor voltage stability (Chapter 5). Another common feature of both drive configurations is that the equivalent voltage levels are equidistant. This means that PWM

switching is always performed with the same voltage steps, regardless of which VSI operates in PWM mode. If the overall dc-link voltage is 600 V, in the case of the 2L-OeW-2L drive with r = 1, VSI_1 and VSI_2 operate with PWM steps of 300 V (equal to their dc-link voltages). For the same overall dc-link voltage, the 3L-OeW-2L drive with r = 2, operates with PWM steps of 200 V. This feature can be used to reorganise the operation of the inverters, as shown next.

6.2.2. REORGANISATION OF INVERTER OPERATIONS IN THE CASE OF THE 2L-OEW-2L DRIVE

Equidistant voltage levels and absence of simultaneous PWM switching of the inverters offers a possibility to modify the modulation strategy in such a way that one inverter operates only in ten-step mode, while the second inverter operates in PWM mode at all times. In this research, VSI_1 is aimed to operate in staircase mode and its switching states are obtained by comparison of the phase voltage reference v_k^* with reference zone borders instead of carriers. This can be written as:

$$S_{1k} = \begin{cases} \text{if } v_k^* \geq l_2 & \text{then 1} \\ \text{if } v_k^* < l_2 & \text{then 0} \end{cases} \tag{6.1}$$

In order to provide the same performance as PD PWM, a set of five voltage references for VSI_2 is acquired as a difference between the produced waveforms by VSI_1 and original phase voltage references:

$$v_{2k}^*(t) = v_{1k}^*(t) + 1 - 2 \cdot v_k^*(t) \tag{6.2}$$

where v_{1k}^* stands for the normalised waveform produced by VSI_1 (in this case, $v_{1k}^* = S_{1k}$). Multiplication with 2 comes from the ratio between reference zones size and the overall reference range, similarly to multiplication factors in duty ratio calculations in Chapter 5 for coupled methods. An additional level shift that is equal to 1 is required in order to obtain the reference in the range from 0 to 1. The final VSI_2 reference is compared with a single carrier signal in the range from 0 to 1 (f_S = 2 kHz):

$$S_{2k} = \begin{cases} \text{if } v_{2k}^* \geq C & \text{then 1} \\ \text{if } v_{2k}^* < C & \text{then 0} \end{cases} \tag{6.3}$$

This way, the difference between the purely sinusoidal phase voltage and the staircase waveform produced by VSI_1 is suppressed by PWM operation of VSI_2. Expressions for duty ratios are summarised in Table 6.1, while Fig. 6.1 shows reference formation for three modulation index values. This kind of modification can be performed for APOD PWM as well, but with some additional calculations. In that case (6.3) has to be split in two parts that correspond to the reference zones 1 and 2, due to different orientation of two carriers in Fig. 3.6a. Since this increases the complexity of the algorithm, while APOD PWM results in worse harmonic performance, only modified PD PWM is considered further.

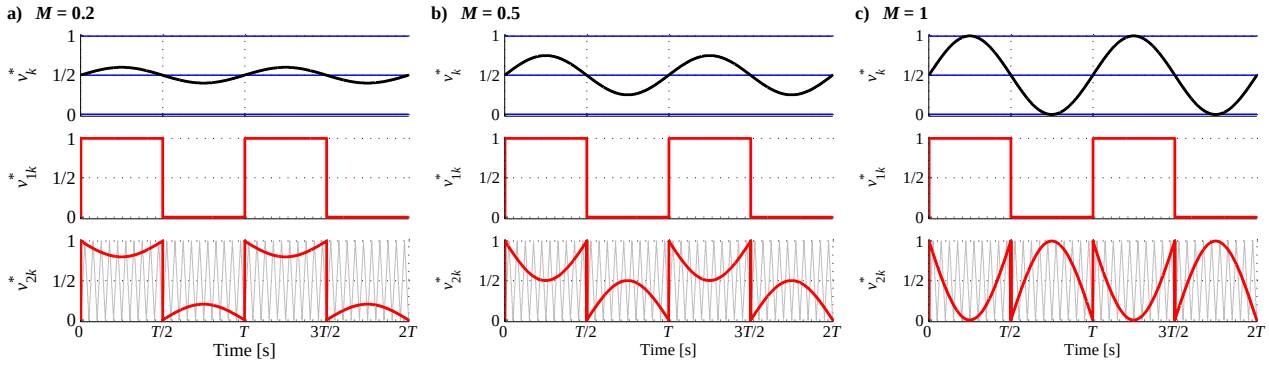


Fig. 6.1. Formation of the inverters' references: modified PD PWM for 2L-OeW-2L topology with r = 1. Top to bottom: v_k^* comparison with equivalent voltage levels, v_{1k}^* and comparison of v_{2k}^* with carrier C for M = 0.2 (a), M = 0.5 (b) M = 1 (c). Carrier frequency is reduced 2/M times, for better visualisation.

Table 6.1. Duty ratios for 2L-OeW-2L with $r = 1$ and modified PD PWM.

Condition	$d_{1k}(t)$	$d_{2k}(t)$
$l_1 \le v_k^*(t) \le l_2$	0	$v_{2k}^*(t)$
$l_2 < v_k^*(t) \le l_3$	1	

The topology under analysis is the same as in Fig. 3.1 ($V_{dc1} = V_{dc2} = 300$ V), which means that the corresponding linearized drive model is identical to the one shown in Fig. 5.3. Here and in the rest of Chapter 6, harmonic components are considered to be the same in every drive phase: $\underline{X}_{nj}$ stands for n^{th} harmonic produced by j^{th} inverter, while $\underline{X}_n$ stands for phase voltage n^{th} harmonic. Analysis of VSI_1 and VSI_2 reference formation with respect to M yields a conclusion that VSI_1 always operates with the same conduction angle $\alpha = 180°$, which results in the same $i_{dclink1}$ mean value for any M, as shown in Fig. 6.2. The produced staircase voltage waveform has a fundamental component $\underline{X}_{11}$, whose rms voltage is:

$$X_{11} = \frac{2 \cdot V_{dc1}}{\pi \cdot \sqrt{2}} \approx 135 \text{ V} \tag{6.4}$$

When the commanded phase voltage fundamental component $\underline{X}_1$ has a lower rms value than $\underline{X}_{11}$, the VSI_2 produces fundamental component $\underline{X}_{12}$ in order to adjust the overall phase voltage fundamental. Numerical analysis shows that this kind of operation takes place for $M < 0.63$. For this reason, $M = 0.6$ leads to a negative $i_{dclink2}$ mean value in Fig. 6.2, i.e. VSI_2 dc-link source is sinking instead of sourcing energy. Based on the analysis in Chapter 5, it can be concluded that $M < 0.63$ causes C_{dc2} overcharging, if dc voltage source with unidirectional output current flow is used for V_{dc2} formation. For higher values of M, VSI_1 operation results in $X_{11} < X_1$. As a result, $\underline{X}_{11}$ and $\underline{X}_{12}$ are now in phase, which leads to positive $i_{dclink2}$ mean value over one fundamental period (Fig. 6.2, $M = 0.8$ and $M = 1$). The border M value, for which $i_{dclink2}$ mean value changes its sign, is referred to as M_b in the rest of the chapter.

Waveforms and rms spectra obtained in simulation for conventional and modified PD PWM are shown in Fig. 6.3 for $M = 1$. Fig. 6.3a shows that conventional PD PWM results in symmetrical operation of the inverters, resulting in identical spectral components in Fig. 6.3c. Since the inverters are ideal, all unwanted harmonics present in v_{1k} and v_{2k} cancel out each other and a purely sinusoidal phase voltage is produced, while both inverters contribute equally to the phase voltage fundamental $X_{11} + X_{12} = X_1$, $X_{11} = X_{12} = 106$ V rms. The same phase voltage can be produced by the modified PD PWM modulation, but in a different manner (Fig. 6.3b) where VSI_1 produces a high fundamental component, $X_{11} = 134$ V rms, but also much higher low-order harmonic content, when compared to the conventional PD PWM case. The unwanted harmonics are filtered out by VSI_2 operation, which also supplies the remaining part of the fundamental component, $X_{12} = 78$ V rms, which is lower than in the case of conventional PD PWM.

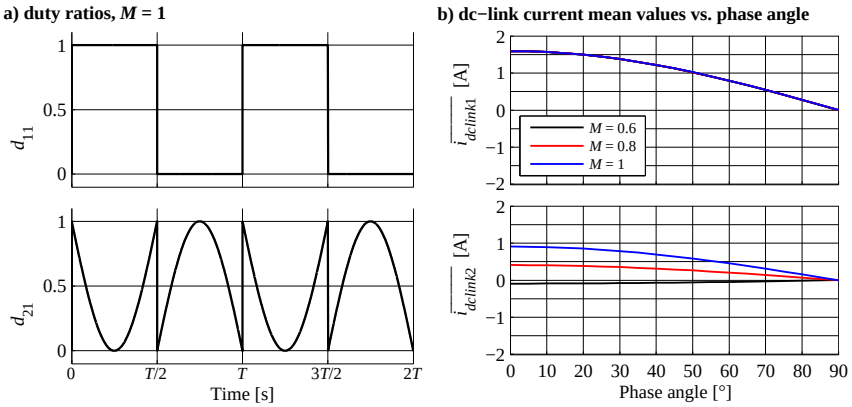


Fig. 6.2. Duty ratios in the first drive phase (a) and phase angle influence on the dc-link current mean values (b) for modified PD PWM in the case of the 2L-OeW-2L drive with $r = 1$, $I_m = 1$ A in (5.5).

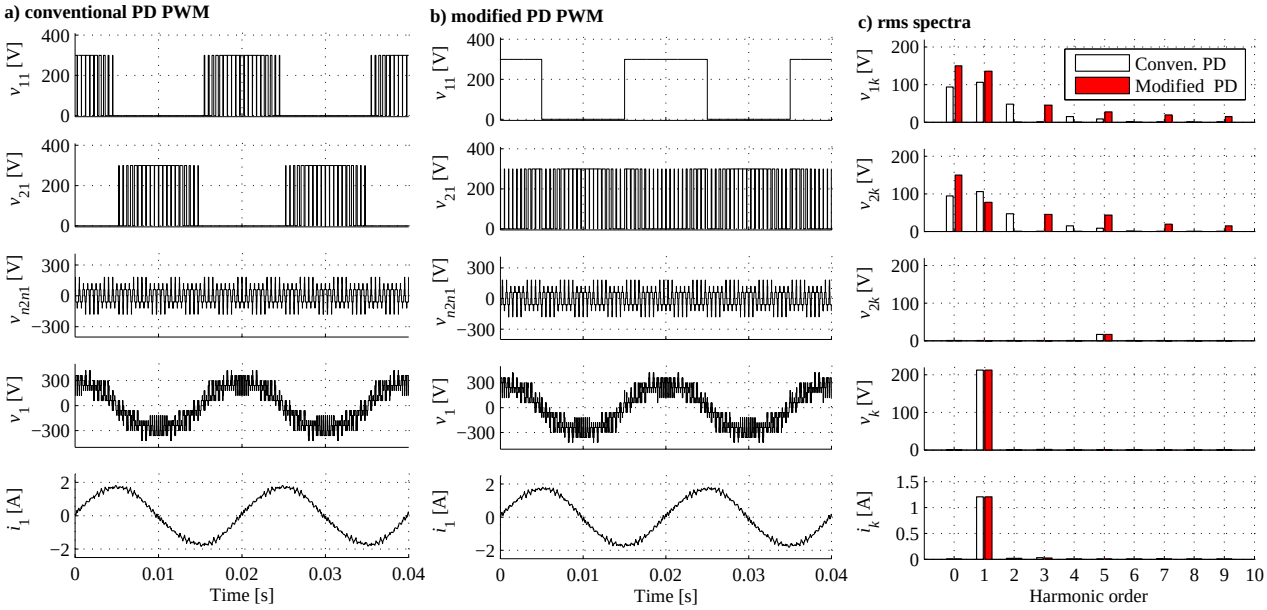


Fig. 6.3. Simulation results: 2L-OeW-2L drive, r = 1 and M = 1, conventional PD PWM (a), modified PD PWM (b) and resulting rms spectra comparison (c).

In [Bodo (2013)], the lower dc-link capacitor overcharging is reported for the range from 0.525 < M < 0.66, which is in agreement with the presented findings (Fig. 6.2b). Note that min-max injection is not applied in the simplified drive model analysed here. The overcharging range lower border in [Bodo (2013)] comes from the fact that only one inverter is used for $M < M_{max}/2$. As a solution, [Bodo (2013)] proposes the adjustment of dc-link voltages in order to eliminate the overcharging problem. This modification leads to overlapping the range of M in which overcharging occurs with $M < M_{max}/2$ where overcharging cannot exist due to single-sided operation. However, this kind of modification is not in agreement with desired operation equivalent to a three-level single-sided supply and it still relies on two isolated dc sources.

6.2.3. REORGANISATION OF INVERTER OPERATIONS IN THE CASE OF THE 3L-OEW-2L DRIVE

The same modification of the PD PWM scheme can be applied to the 3L-OeW-2L drive with r = 2. Again, VSI_1 is controlled using staircase modulation while VSI_2 is aimed for PWM operation. Note that these functionalities can be swapped without any consequences in the case of the 2L-OeW-2L drive due to the symmetrical structure and equal dc-link voltages of two inverters. However, this is not the case for the 3L-OeW-2L drive. Only staircase modulation of VSI_1 (three-level) and PWM operation of VSI_2 (two-level) results in the same v_k, v_{n2n1} and i_k waveforms as in the case of conventional PD PWM, presented in Section 4.3. Similarly to the previously analysed case, VSI_1 switching states are obtained by comparison with normalized equivalent voltage levels:

$$S_{1k}^{a} = \begin{cases} \text{if } v_{1k}^{*} \geq l_3 & \text{then 1} \\ \text{if } v_{1k}^{*} < l_3 & \text{then 0} \end{cases}$$
$$S_{1k}^{b} = \begin{cases} \text{if } v_{1k}^{*} \geq l_2 & \text{then 1} \\ \text{if } v_{1k}^{*} < l_2 & \text{then 0} \end{cases} \tag{6.5}$$

Staircase waveform produced with (6.5) utilises all three dc voltage levels on VSI_1 side. Voltage reference v_{1k}^{*} is:

$$v_{1k}^{*} = \frac{S_{1k}^{a} + S_{2k}^{a}}{2} \tag{6.6}$$

VSI_2 voltage references are again obtained as the difference between v_k^{*} and v_{1k}^{*}:

$$v_{2k}^{*}(t) = 2 \cdot v_{1k}^{*}(t) + 1 - 3 \cdot v_{k}^{*}(t) \tag{6.7}$$

Voltage references, formed using (6.5) - (6.7), are shown in Fig. 6.4. As in the case of conventional PD PWM, for $M < 0.35$, the phase voltage reference is always between l_2 and l_3, which results in two-level operation, performed with VSI_2 in PWM mode only, while VSI_1 holds all its leg outputs at v_{mp}. For higher modulation index values, both inverters are in use. Duty ratio expressions are summarised in Table 6.2. VSI_1 operates in staircase mode, producing a leg voltage with a fundamental rms component equal to [Corzine et al. (2006)]:

$$X_{11} = \frac{2 \cdot V_{dc1}}{\pi \cdot \sqrt{2}} \cdot \cos(\alpha) \tag{6.8}$$

In this case, conduction angle α corresponds with $v_k^*(t)$ intersections with $l_2 = 1/3$ and $l_3 = 2/3$.

Table 6.2. Duty ratios for the 3L-OeW-2L with $r = 2$ and modified PD PWM.

Condition	d_{1k}^{a}	d_{1k}^{b}	d_{2k}
$l_1 \le v_k^*(t) \le l_2$	0	0	$v_{2k}^*(t)$
$l_2 < v_k^*(t) \le l_3$	0	1	
$l_3 < v_k^*(t) \le l_4$	1	1	

Using (3.8) with $R_{offset} = 0.5$, (6.8) and the condition $v_k^*(t) = l_3$, VSI_1 leg voltage fundamental component rms is:

$$X_{11} = \frac{\sqrt{2} \cdot V_{dc1}}{\pi} \cdot \cos\left(\arcsin\left(\frac{1}{3 \cdot M}\right)\right) = \frac{\sqrt{2} \cdot V_{dc1}}{3 \cdot M \cdot \pi} \cdot \sqrt{9 \cdot M^2 - 1} \tag{6.9}$$

For $M = 1$, (6.9) yields $X_{11} \approx 170$ V rms, while the fundamental component required by the machine is $X_1 \approx 212$ V rms. Like the previously analysed configuration, the 3L-OeW-2L is also not capable of satisfying the phase voltage fundamental component using VSI_1 only. Based on Table 6.2, the drive model in Fig. 5.15 and sinusoidal phase currents approximation with $I_m = 1$ A in (5.5), duty ratio waveforms and mean dc-link current values in Fig. 6.5 are calculated. Due to symmetrical VSI_1 operation, the i_{mp} mean value is always zero, which guarantees that the NPC inverter operates with balanced dc-link capacitor voltages. Phase angle influence on the overall $i_{dclink1}$ mean values is similar to the case of conventional PD PWM (Fig. 5.18a). Contrary to the 2L-OeW-2L drive case, M also has influence on the $i_{dclink1}$ mean value, but much lower than in Fig. 5.18a. The VSI_2 dc-link current mean value depends highly on M. In the cases when VSI_1 produces higher X_{1k} than commanded X_1, the $i_{dclink2}$ mean value is negative, and the low- side dc-link voltage is sinking power instead of sourcing. This takes place for $M_{max}/3 < M < 0.764$. In the rest of the multilevel operation range, VSI_2 is contributing to the v_k fundamental, which results in positive $i_{dclink2}$ mean value. Simulation results are shown in Fig. 6.6.

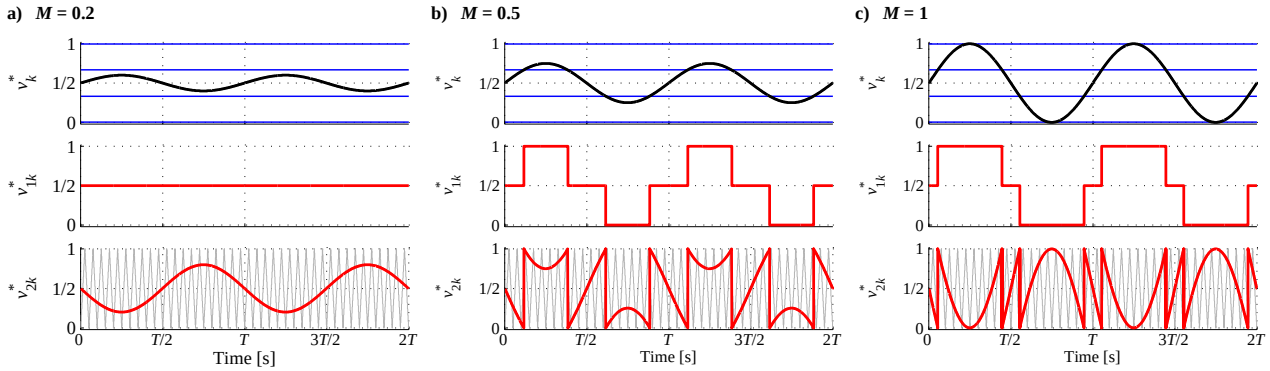


Fig. 6.4. Formation of the inverters' references: modified PD PWM for 3L-OeW-2L topology with $r = 2$. Top to bottom: v_k^* comparison with equivalent voltage levels, v_{1k}^* and comparison of v_{2k}^* with carrier C for $M = 0.2$ (a), $M = 0.5$ (b) $M = 1$ (c). Carrier frequency is reduced $2/M$ times, for better visualisation.

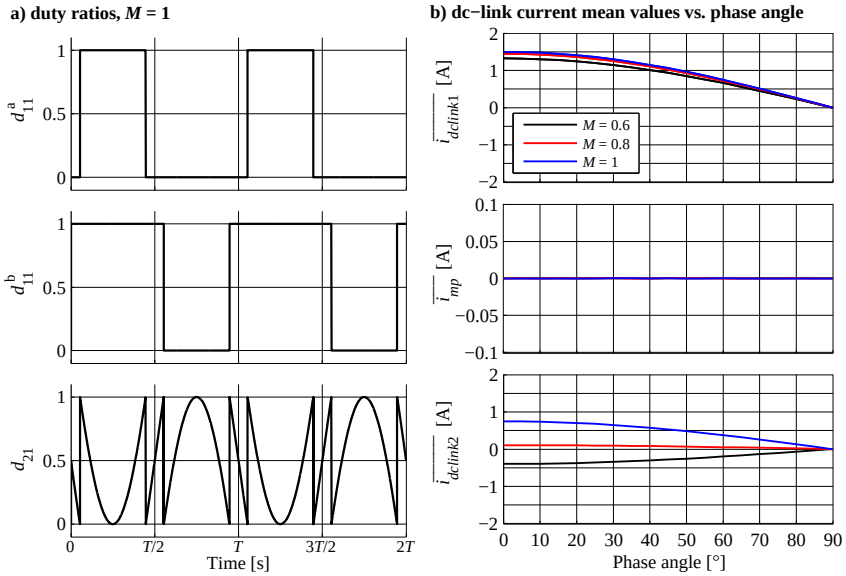


Fig. 6.5. Duty ratios in the first drive phase (a) and phase angle influence on the dc-link current mean values (b) for modified PD PWM in the case of 3L-OeW-2L drive with $r = 2$.

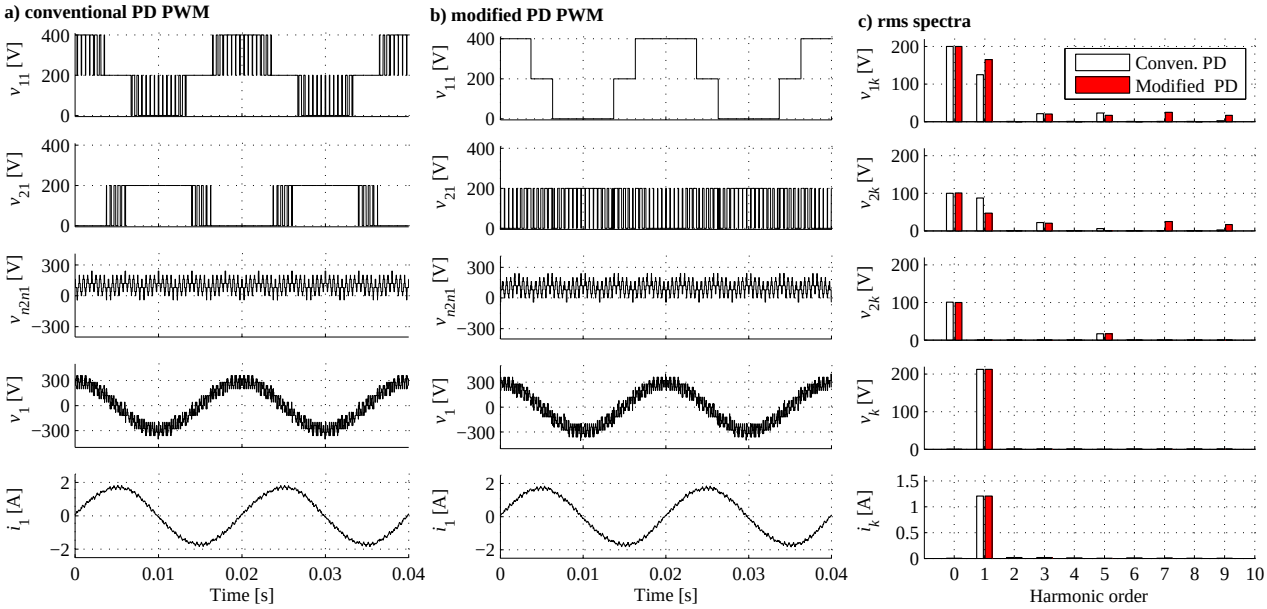


Fig. 6.6. Simulation results: 3L-OeW-2L drive, $r = 2$ and $M = 1$, conventional PD PWM (a), modified PD PWM (b) and resulting rms spectra comparison (c).

Conventional PD PWM results in lower harmonic distortion of the leg voltages of the two inverters when compared to the modified PD PWM. Phase voltage fundamental component is formed in a different manner compared to the 2L-OeW-2L drive with $r = 1$. The fundamental components supplied by the inverters depend on M, since VSI_1 only operates in reference zones 1 and 3, while VSI_2 operates in PWM mode in the reference zone 2 only. Modified PD PWM modulation increases VSI_1 contribution to the phase voltage fundamental, i.e. required X_{12} is lower than in the case of the 2L-OeW-2L drive. Another advantage of the 3L-OeW-2L drive are lower low-order harmonics produced by VSI_1.

6.3. ELIMINATION OF ONE DC SOURCE

As shown in [Corzine et al. (2004), Kim et al. (2004), Corzine et al. (2006), Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)] some OeW winding topologies require only one active dc-link voltage source, which supplies the inverter that operates in staircase mode. This, so-called bulk [Corzine et al. (2004), Corzine et al. (2006)] or main [Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)] inverter is capable of producing the complete phase voltage fundamental, thanks to an appropriate dc-link voltage on that drive side. The second inverter is operating as an active filter only, in order to suppress undesired harmonic content. This inverter is referred to as a floating bridge [Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)] or conditioning inverter [Corzine et al. (2004), Corzine et al. (2006)]. Special attention is paid to the VSI_2 dc-link capacitor voltage balancing algorithm, based on closed-loop control, incorporated within the modulation strategy. This kind of drive configuration, based on a single dc source and isolated inverters, requires more complex control algorithms and higher dc-link voltage on VSI_1 side, when compared to the dual supply case. Nevertheless, the motivation for omitting one dc source from the circuitry is still very high, since it leads to lower hardware complexity and cost.

As shown in the two previous subsections, analysed topologies with modified PD PWM form the phase voltage fundamental component using both inverters, although their operation is similar to those presented in [Corzine et al. (2004), Kim et al. (2004), Corzine et al. (2006), Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)]. A minor difference in operation comes from the fact that conduction angle α is not actively controlled. The major difference is in utilised dc-link voltages. In all previous research efforts except in [Ewanchuk et al. (2013)], the complete phase voltage fundamental component is supplied from the inverter that operates in staircase mode. The control proposed in [Ewanchuk et al. (2013)] leads to dc-link voltage boosting, which means that the achievable phase voltage fundamental is higher than maximally producible by VSI_1 alone. This approach offers a possibility to balance the charge stored in the conditioning VSI dc-link capacitor, which leads to the desired dc-link voltage ratio and to utilise the overall dc-link voltage equal to $V_{dc1} + V_{dc2}$, for phase voltage fundamental production, instead of utilisation of V_{dc1} only, as in [Corzine et al. (2004), Kim et al. (2004), Corzine et al. (2006), Ewanchuk and Salmon (2010), Ewanchuk et al. (2013), Haque et al. (2013), Chowdhury et al. (2015)]. At the same time, a harmonic performance equivalent to the multilevel single-sided inverter case is achieved. In this section, a novel control algorithm is proposed, based on the analysis of dc-link currents and dc-link voltage stability presented in Chapter 5.

In both analysed cases in Section 6.2, the VSI_1 dc voltage source delivers most of the active power to the drive. Hence, the dc source at VSI_2 drive side can be potentially omitted. This leads to equivalent models of the two topologies as in Fig. 6.7. The first consequence of VSI_2 dc source elimination is the need for initial charging of C_{dc2}. The simplified equivalent circuit for pre-charging is depicted in Fig. 6.8. The first drive phase is used to transfer sufficient charge from the VSI_1 dc source to C_{dc2}, in order to increase v_{cdc2} from zero to the desired V_{cdc2}. Control of this process is performed using S_{up21} and S_{dn21} in PWM mode, while every other leg output of the two VSIs is kept at constant voltage potential. Voltage across C_{dc2} is monitored and controlled with a PI controller, which adjusts duty ratio d_{21}, and ensures that v_{cdc2} slowly reaches the commanded voltage level (V^*_{cdc2}). Due to the desired dc-link voltage ratios, this method is more accurate for the 3L-OeW-2L drive, while in the case of 2L-OeW-2L drive a steady-state error exists, due to dead-time effects and voltage drops on machine windings and semiconductors. Hence, this pre-charging method is more accurate for the case when $V_{dc1} = 400$ V is used for achieving $v_{cdc2} = 200$ V (3L-OeW-2L), than in the case when $V_{dc1} = V^*_{cdc2} = 300$ V (2L-OeW-2L drive).

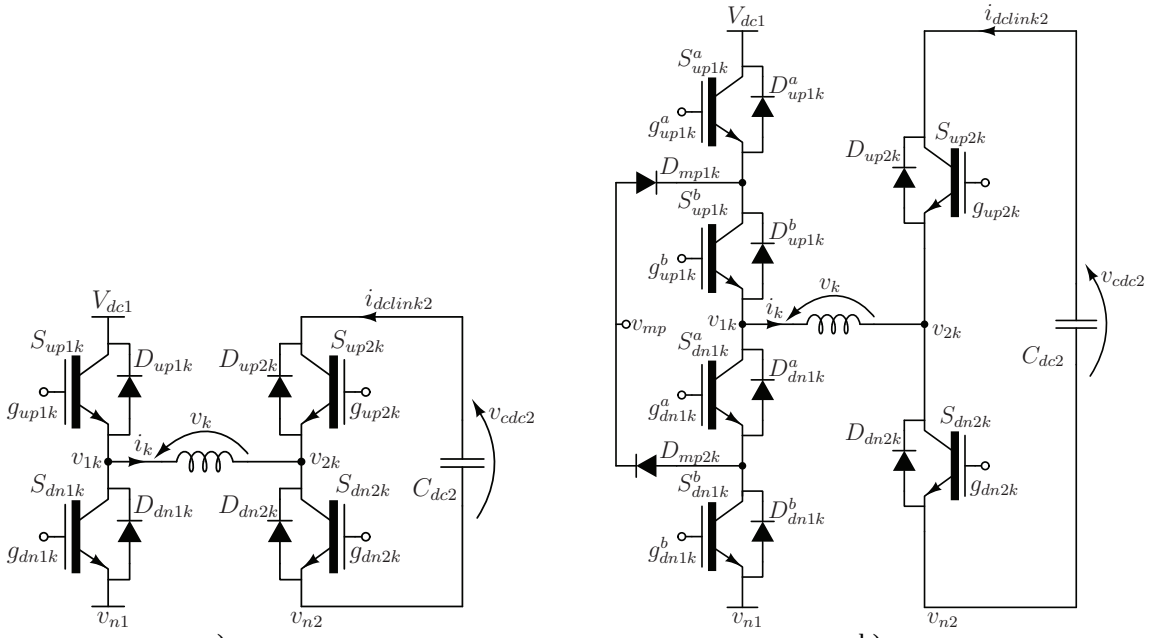


Fig. 6.7. Equivalent models of: 2L-OeW-2L (a) and 3L-OeW-2L (b) with single dc source. For simplicity, VSI_2 dc-link capacitor is labelled with C_{dc2} instead of previously used C_{dc21} in the case of 3L-OeW-2L drive.

However, simulation results show that this error is naturally eliminated during regular drive operation, thanks to the closed-loop v_{cdc2} balancing algorithm, which is explained next.

The analysis presented in Chapter 5, yields that the C_{dc2} voltage can be constant only if the $i_{dclink2}$ mean value is equal to zero. However, it is shown in Figs. 6.2 and 6.5 that modified PD PWM leads to both negative and positive $i_{dclink2}$ mean values, depending on the modulation index. Only $\phi = 90°$ results in an $i_{dclink2}$ zero mean value for any value of M. Although this case has no practical importance, due to machines characteristics, it actually provides a clue to how C_{dc2} voltage can be balanced. As shown in [Ewanchuk et al. (2013)], control of the phase angle between references of the two inverters provides a sufficient degree of freedom for dc-link capacitor balancing on the floating inverter side. If VSI_1 modulation has a role of producing the phase voltage fundamental, the phase angle between VSI_1 leg voltage and phase current depends on the machine and its load only. This opens the possibility to adjust the phase angle between VSI_2 reference and phase current in such a way that the $i_{dclink2}$ mean value is zero during one fundamental period. However, this approach requires complex calculation and estimation of phase angle based on phase current measurements, which is difficult to perform, especially during speed transients or load variations.

In [Darijevic et al. (2015c)] a different dc-link capacitor voltage balancing algorithm is proposed, based on the analysis of dc-link currents and drive models presented in Chapter 5, where it is shown that the C_{dc2} charge depends on the conduction times (i.e. duty ratios) of semiconductors in upper IGBT+D pairs in VSI_2. Since the drive is symmetrical, it follows that each stator phase has to be treated in the same way, which is naturally achieved using CB PWM. The simplest method for capacitor voltage balancing is based on a PI controller, which compares measured v_{cdc2} with the reference V^*_{cdc2}, similarly to the pre-charging control. Control block diagram is given in Fig. 6.9. Error signal (e) is processed with proportional and integral gain ($K_P = 0.004\ \mathrm{V}^{-1}$, $K_I = 0.08\ \mathrm{V}^{-1}\cdot\mathrm{s}^{-1}$). The anti-windup constant is $K_{aw} = 50$ V, while output saturation block (SAT) has limits of ±0.12 and ±0.07, in the case of 2L-OeW-2L and 3L-OeW-2L drives, respectively. The error signal is conditioned with $M > M_{start}$, since the balancing algorithm should be applied only for dual inverter operation. For the 2L-OeW-2L drive, $M_{start} = 0$, while Fig. 6.4 yields $M_{start} = 0.35$ for the 3L-OeW-2L drive if min-max injection is applied.

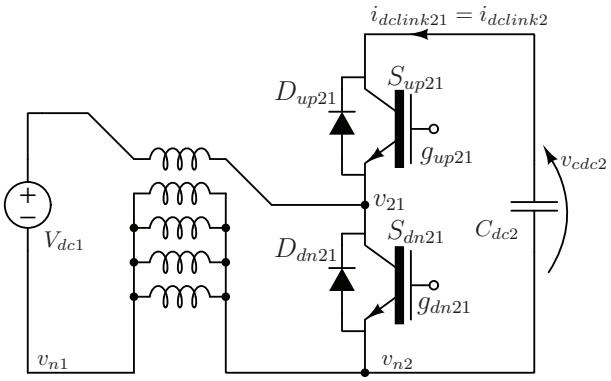


Fig. 6.8. Equivalent circuit for C_{dc2} pre-charging mode.

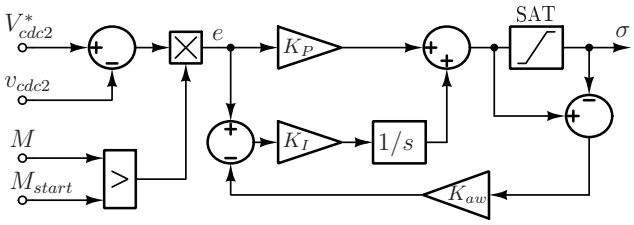


Fig. 6.9. PI controller for capacitor voltage balancing.

The final output of PI controller (σ) represents the small offset that should be added to the v^*_{2k}, in order to adjust the switching times. Parameter σ has no unit and it is directly applied to the normalised voltage references. Such an updated reference for VSI_2 is compared with carrier signal C:

$$S^*_{2k} = \begin{cases} \text{if } \left(v^*_{2k} + \sigma \cdot \text{sign}(i_k)\right) > C & \text{then 1} \\ \text{if } \left(v^*_{2k} + \sigma \cdot \text{sign}(i_k)\right) < C & \text{then 0} \end{cases} \tag{6.10}$$

The phase current sign is taken into account since σ would otherwise change its sign approximately every half of the fundamental period. However, since the phase current sign is not the same in every drive phase, it would be necessary to tune each phase voltage reference independently, with different σ. In essence, capacitor voltage depends on the duration of conduction intervals of S_{up2k} and D_{up2k}. If the phase current is positive, when diode D_{up2k} is on, some amount of charge will be added to the C_{dc21}. Negative phase current and conduction of S_{up2k} will lead to the capacitor discharge, which reduces v_{cdc21}. This leads to a conclusion that the amount of charge that is transferred to C_{dc2} when $i_k > 0$ and D_{up2k} is on, and taken from the C_{dc21} when $i_k < 0$ and S_{up2k} is on, should be equalised. Conduction intervals of S_{up2k} are of interest for this analysis only when $i_k < 0$. Similarly, D_{up2k} conducts only when $S_{2k} = 1$ and $i_k > 0$.

In order to clarify the proposed method, let us analyse two examples. In the case when $v_{cdc2} < V^*_{cdc2}$ and $i_k > 0$, σ takes positive value, while sign(i_k) equals 1. This increases the instantaneous value of v^*_{2k}, meaning that comparison with C results in somewhat longer duration of state $S_{2k} = 1$. Since the current is positive, additional charge is added to the capacitor via D_{up2k}, leading to the v_{cdc2} increment and reduction of the PI error signal. At the same time, some other phase current is negative. In that phase, positive σ will be multiplied with −1 and added to the corresponding VSI_2 reference. Comparison of such an updated reference with C will result in shorter duration of S_{2k}. In other words, less charge will be removed from the capacitor (by switching actions in that phase) than in the case of the original v^*_{2k}. The overall effect is therefore increment of the C_{dc2} voltage. The same mechanism leads to v_{cdc2} reduction for $v_{cdc2} > V^*_{cdc2}$. This algorithm is incorporated within the modified PD PWM, which leads to a complete bulk and conditioning (B&C) carrier based PWM technique. Application of this method is firstly tested in idealised drive models presented in Chapter 5. Results are shown in Figs. 6.10 and 6.11.

In order to simulate the influence of closed-loop control, an estimation of σ is applied to v^*_{2k}, multiplied with the phase current sign:

$$d_{2k} = v^*_{2k} + \sigma \cdot \text{sign}(i_k) = v^*_{2k} + r \cdot \frac{X_{11} \cdot \sqrt{2}}{V_{dc}} \cdot \frac{(90^o - \phi)}{90^o} \cdot (M_b - M) \cdot \text{sign}(i_k) \tag{6.11}$$

where $M_b = 0.63$ for 2L-OeW-2L drive and $M_b = 0.764$ for 3L-OeW-2L drive, while X_{11} is calculated using (6.4) and (6.9), respectively. As a result, absolute $i_{dclink2}$ mean value is minimised throughout ϕ range. Duty ratio d_{21} in Fig. 6.10a is highly distorted, when compared to Fig. 6.2a.

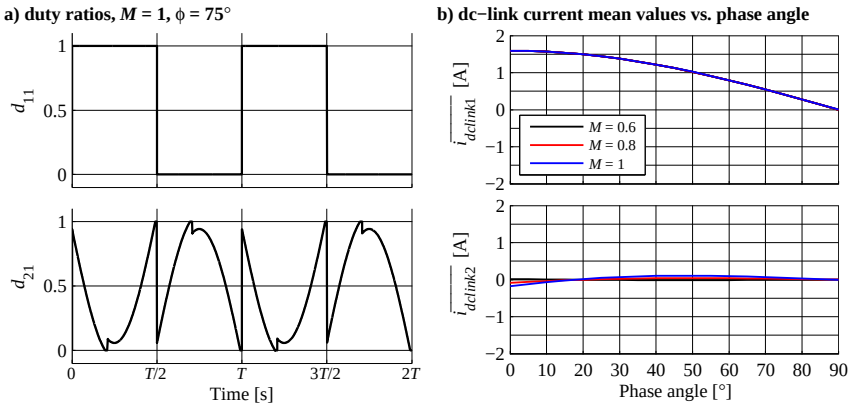


Fig. 6.10. Duty ratios in the first drive phase for $M = 1$ and $\phi = 75°$ (a) and phase angle influence on the dc-link current mean values (b) for B&C in the case of 2L-OeW-2L drive with $r = 1$, $I_m = 1$ A in (5.5).

For the 2L-OeW-2L drive, B&C leads to the higher harmonic distortion for low modulation indices, since VSI_2 duty ratios are always close to the minimal and maximal values. This means that the VSI_2 switching pattern for low M values is similar to staircase operation (Fig. 6.1a). Note that single-sided PWM operation up to $M = M_{max}/2$ as in [Bodo (2013)] is now not feasible, since VSI_2 does not have an active power source. When v_{cdc2} balancing algorithm is applied for low modulation indices, required σ is highly negative and distortion of the VSI_2 reference is very high, in order to keep v_{cdc2} constant. Similarly, in the range around $M = 1$, VSI_2 contribution to the phase voltage fundamental is high. In order to prevent C_{dc2} from discharging, high and positive σ value is produced by the PI controller. In both cases, capacitor voltage balancing is traded for elimination of low-order harmonics introduced by the staircase modulation of VSI_1. Consequently, the harmonic performance is far from ideal.

Similar effects of the voltage balancing algorithm can be observed when B&C is applied to the 3L-OeW-2L drive, as shown in Fig. 6.11. However, staircase modulation is now performed with the higher dc-link voltage, meaning that the VSI_1 contribution to the phase voltage fundamental component is higher. This means that the required fundamental voltage boost from VSI_2 side is lower, compared to the 2L-OeW-2L drive. At the same time, the staircase waveform is less distorted, which reduces the requirements for low-order harmonic conditioning, making v_{cdc2} balancing easier.

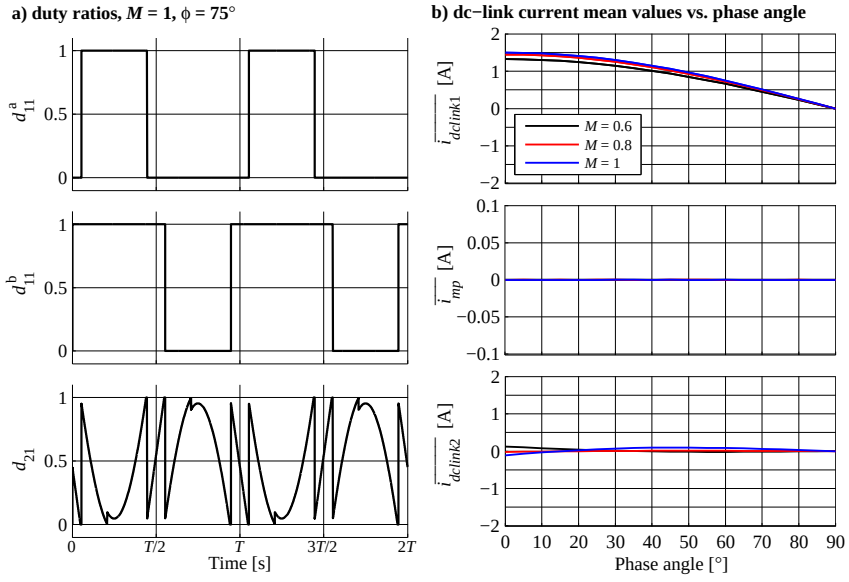


Fig. 6.11. Duty ratios in the first drive phase for $M = 1$ and $\phi = 75°$ (a) and phase angle influence on the dc-link currents mean values (b) for B&C in the case of 3L-OeW-2L drive with $r = 2$.

Unfortunately some restrictions apply. Namely, B&C cannot be applied for the 3L-OeW-2L drive with a single dc source when $M \leq M_{max}/3$. The reason is that the proposed modulation results in formation of a star connection on VSI_1 side, since (6.5) will give $S_{1k}^{a} = 0$ and $S_{1k}^{b} = 1$, which results in a constant leg voltage equal to v_{mp} throughout the fundamental period (Fig. 6.4a), for all five-phases. At the same time, the inverter that does not have an active voltage source (VSI_2, Fig. 6.7b) should be in PWM mode, according to Fig. 6.4a. Hence, for $M \leq 0.35$ VSI_1 is used in PWM mode, with a low switching frequency of 1 kHz. In this operation mode, VSI_2 is used for the star connection formation, which means that the machine is supplied from a three-level single-sided supply with an effective dc-link voltage of $V_{dc1} = 400$ V. If C_{dc2} can be treated as lossless (which seems to be a reasonable simplification for very short time intervals), the proposed modification results in v_{cdc2} voltage being constant for $M \leq 0.35$. When $M > 0.35$ both inverters are used, according to the modified PD PWM, with v_{cdc2} voltage balancing algorithm. As explained in Chapter 8, modification of this approach, based on active control of bulk inverter conduction angle for low modulation index values is one of the topics for future work. Here, the main aim of this research topic is to investigate if, and under what conditions, the OeW drive with a single active dc source is capable of delivering the same harmonic performance as its counterpart with two active dc sources and the same dc-link voltage ratio.

One may wonder if a similar modification can be applied to the 2L-OeW-2L drive under B&C control, in order to avoid the mentioned deterioration in harmonic performance for low M. When compared to the 3L-OeW-2L drive, where this modification is necessary, it seems that single-sided PWM operation of VSI_1 in the case of the 2L-OeW-2L drive is impractical, due to the higher V_{dc1}, i.e. blocking voltage requirements for IGBT+D modules on VSI_1 side. At the same time, single-sided operation with the 2L-OeW-2L drive should be applied up to $M = 0.525$, due to dc-link voltage ratio of 1:1. After all, this leads to two-level modulation, while for the 3L-OeW-2L drive three-level modulation is utilised in the same operation mode. In other words, the 3L-OeW-2L drive requires single-sided operation in a lower M range, which has smaller drawbacks in drive design and harmonic performance.

The THD(M) dependencies for both topologies are obtained using simulations. The results are shown in Fig. 6.12, for the operation with no load, and Fig. 6.13 for load torque equal to $TL = 2$ Nm. As expected, if modified PD PWM is used, both drives have similar harmonic performance to that obtained with PD PWM (Figs. 3.20c and 4.14c). However, THD(M) dependences for B&C control yield a conclusion that the 2L-OeW-2L drive suffers from degraded harmonic performance, while the 3L-OeW-2L drive produces less distorted waveforms even under load conditions. This difference is a direct consequence of utilised dc-link voltage ratios, as well as the superior three-level staircase modulation, when compared to the two-level counterpart.

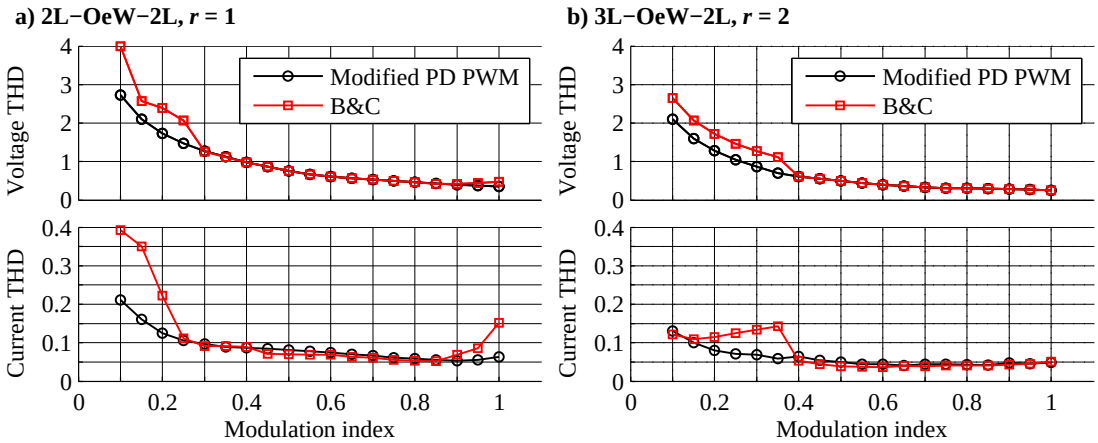


Fig. 6.12. Simulation results: v_1 and i_1 THD against M for 2L-OeW-2L (a) and 3L-OeW-2L(b), $TL = 0$.

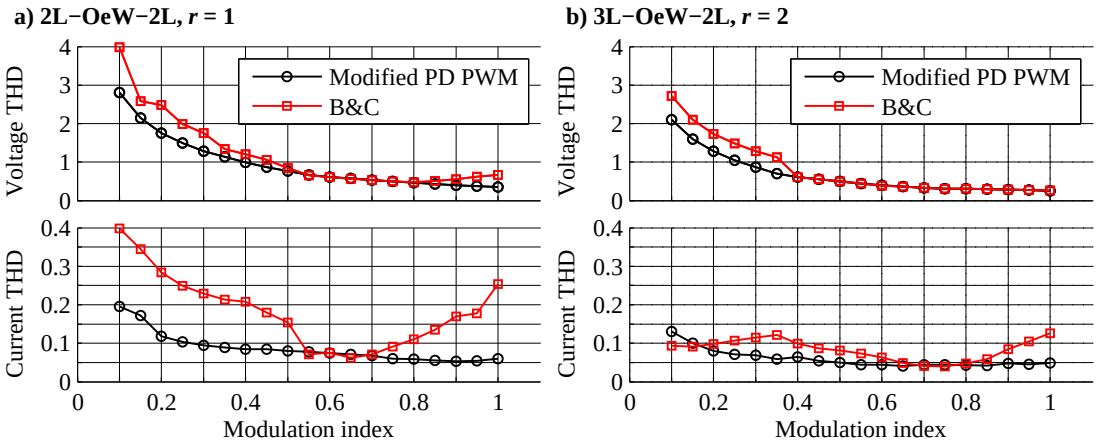


Fig. 6.13. Simulation results: v_1 and i_1 THD against M for 2L-OeW-2L (a) and 3L-OeW-2L(b), TL = 2 Nm.

VSI_1 contribution to the fundamental voltage is always higher in the case of the 3L-OeW-2L drive, since in that case V_{dc1} is about 33% higher than the same dc-link voltage in the case of 2L-OeW-2L drive. At the same time, the requirement of the conditioning inverter with regard to suppression of low-order harmonics is lower, due to the finer voltage shape produced by VSI_1. This outcome can also be seen from the proposed closed-loop v_{cdc2} balancing parameters. Namely, the 2L-OeW-2L drive requires about 42% higher saturation limits of SAT block in Fig. 6.9, in order to maintain the v_{cdc2} at the desired level, during transients and under load conditions. This means that a 42% higher σ value can be expected, which lowers the ability to supress unwanted low-order harmonics under load conditions (Fig. 6.13). Clearly, the 3L-OeW-2L drive is the better candidate for this kind of B&C control.

The dynamic performance of the two drives under *V/f* control is depicted in Fig. 6.14. Traces for different M and TL values are shown in order to demonstrate the differences in steady state σ, which are predicted by previous analysis of linearized models (where load is modelled as influence of phase angle on dc-link currents) for different load conditions. Acceleration of the 2L-OeW-2L drive results in an unstable v_{cdc2} in the region of low modulation indices, due to the inherent inability to reduce the phase voltage fundamental produced by VSI_1. This causes saturation of the PI controller output, leading to higher harmonic distortion and v_{cdc2} voltage drop, since VSI_2 is not able to balance its dc-link voltage and control phase voltage fundamental in this region. In the same M range, the 3L-OeW-2L drive operates in single-sided mode, where the VSI_1 switching frequency is 1 kHz, which eliminates the v_{cdc2} balancing problem up to M = 0.35 (when min-max injection is applied).

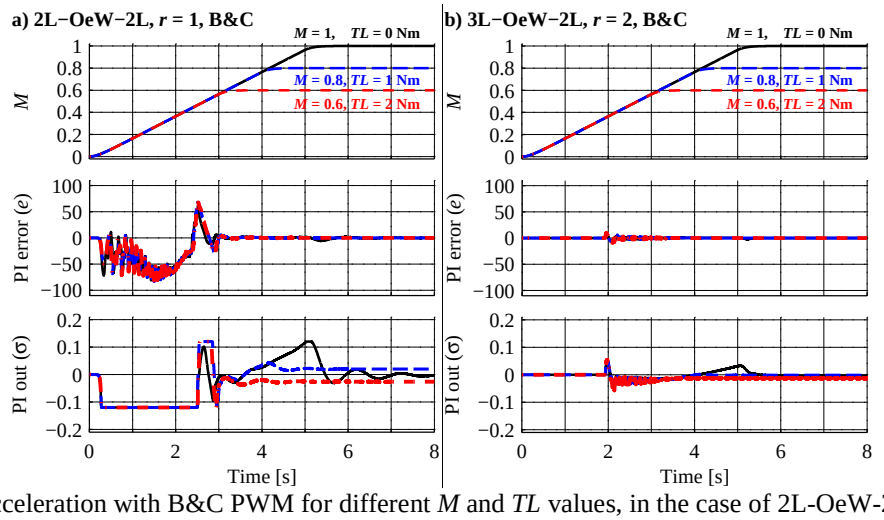


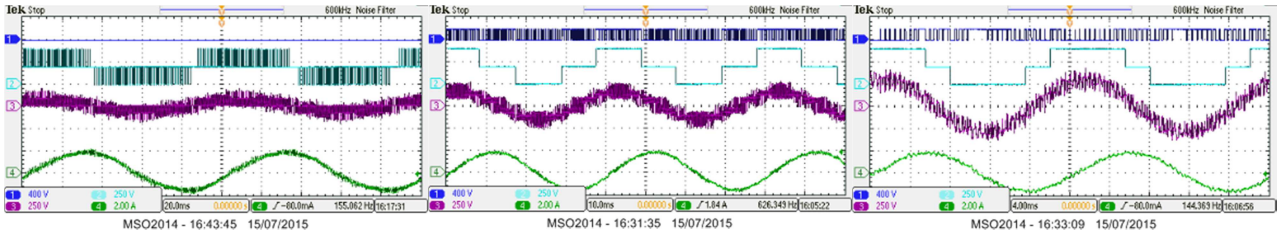
Fig. 6.14. Drive acceleration with B&C PWM for different M and TL values, in the case of 2L-OeW-2L drive with r = 1 (a) and 3L-OeW-2L drive with r = 2 (b).

The final σ is different for different loads, which clearly means that harmonic performance is ruined even in steady state, under loaded conditions in Fig. 6.14a. Furthermore, in the no load case, the 2L-OeW-2L drive is hardly able to balance v_{cdc2} if nominal speed is commanded ($M = 1$), according to damped oscillations in σ trace in this case. This issue can be suppressed with a higher C_{dc2} value, but this again leads to the higher hardware cost and reduced power density. Fig. 6.14b shows that the 3L-OeW-2L drive offers more stable operation in all analysed cases, and lower σ value in steady state conditions, which results in better control of low-order current harmonics. This finding is in agreement with THD performance in Figs. 6.12 and 6.13. For these reasons, only the 3L-OeW-2L topology is considered for experimental verification in the following section.

6.4. EXPERIMENTAL RESULTS

Recorded waveforms for bulk and conditioning operation for the 3L-OeW-2L drive with $r = 2$ are shown in Fig. 6.15. Four oscilloscope channels CH1 to CH4 show v_{21}, v_{11}, v_1 and i_1, respectively. During single-sided operation ($M = 0.2$), the drive operates in three-level mode, while B&C operation (Figs. 6.15b and 6.15c) produces the phase voltage and phase current waveforms equivalent to those obtained with four-level operation (Fig. 4.15b and 4.15c). Some pulse dropping in VSI_2 operation can be observed for $M = 1$, which is a consequence of the applied v_{cdc2} balancing algorithm, i.e. non-zero σ value (Fig. 6.11). According to the constant maximal VSI_2 leg voltage value for $M = 0.5$ and $M = 1$, it can be concluded that v_{cdc2} is stable.

Obtained spectra and THD(M) dependencies are shown in Figs. 6.16 and 6.17, respectively. Comparison with PD PWM shows that somewhat higher low-order harmonic content is produced. Three-level operation with $f_S = 1$ kHz and a dc-link voltage of 400 V leads to lower 3rd but higher 9th phase voltage harmonic, when compared to two-level operation in Fig. 4.17, where only VSI_2 operates in PWM mode ($f_S = 2$ kHz, $V_{dc2} = 200$ V). When the v_{cdc2} balancing algorithm is active ($M > 0.35$), harmonic distortion is slightly increased, due to the trade-off between voltage balancing and suppression of low-order harmonics by VSI_2 modulation. As expected, differences between PD PWM and B&C harmonic performance are the smallest in the region $0.6 < M < 0.8$, where VSI_1 produces almost the complete phase voltage fundamental. Simplified model analysis from Section 6.2 yields $X_1 = X_{11}$ for $M = 0.764$. However, in both detailed numerical simulation analysis (Figs. 6.12 and 6.13) and experimental verification (Fig. 6.17), min-max injection is applied, which leads to an increased dc-link utilisation. As a result $X_1 = X_{11}$ is obtained for $M \approx 0.7$. Around this value VSI_2 naturally keeps low-order harmonic content low as well as maintaining the desired v_{cdc2}. For the case when the machine operates with no load, experimentally verified here, this means that σ value is close to zero, since induction machine has a phase angle of almost 90°. For modulation index values around $M = 1$, slightly higher phase current THD values are obtained, due to somewhat increased low order harmonics in the second plane.



a) b) c)

Fig. 6.15. Experimental results: B&C operation waveforms, TL = 0, $M = 0.2$ (a), $M = 0.5$ (b), $M = 1$ (c). Traces from top to bottom: CH1 shows v_{21} (400 V/div), CH2 v_{11} (250 V/div), CH3 v_1 (250 V/div) and CH4 i_1 (2 A/div).

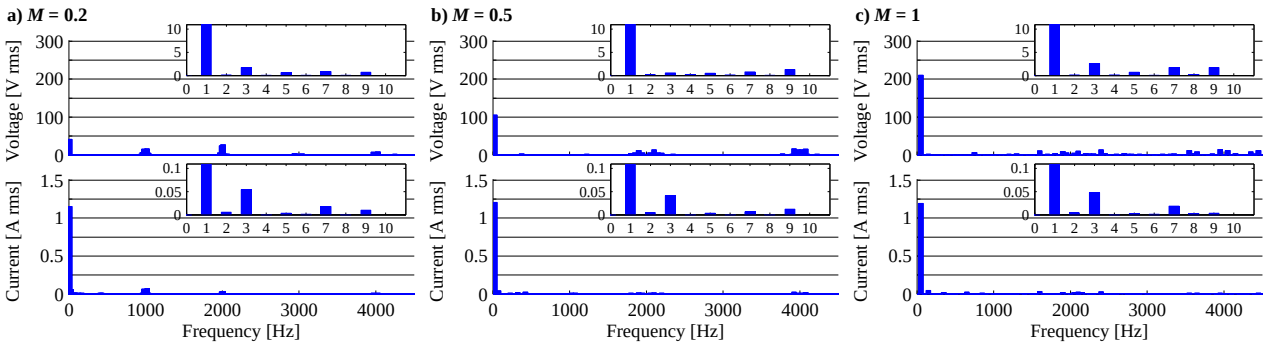


Fig. 6.16. Experimental results: B&C operation v_1 and i_1 spectra, with M = 0.2 (a), M = 0.5 (b), M = 1 (c).

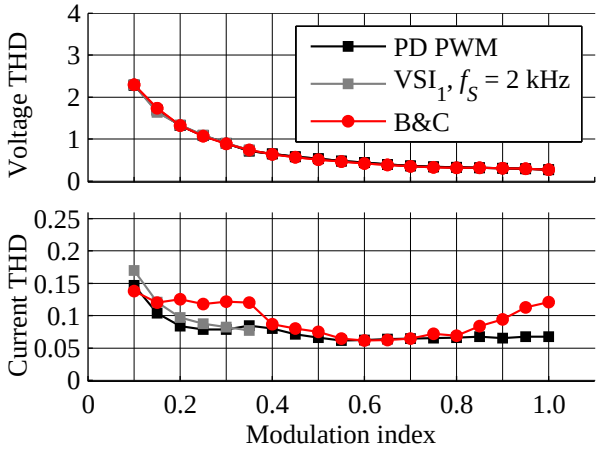


Fig. 6.17. Experimental results: Comparison of phase voltage and phase current THD(M) for PD PWM, single-sided three-level operation with VSI_1 (f_S = 2 kHz) and B&C operation of 3L-OeW-2L drive.

Fig. 6.17 also shows the harmonic performance of the three-level single-sided PD PWM operation, that utilises VSI_1 at f_S = 2 kHz. This is tested only for M < 0.35, in order to examine the switching frequency reduction, with regard to the proposed modulation method in this range. Clearly, the impact of the lower switching frequency is minor and tolerable. Due to lower dead-time effects, PWM switching at 1 kHz seems to be more appropriate for very low M, around 0.1. B&C performance under loaded conditions is experimentally verified in Chapter 7, where the OeW drive dynamic performance under closed-loop control is analysed.

6.5. SUMMARY

In this chapter, a possibility to reduce the OeW drive hardware complexity is investigated. It is shown that two previously analysed drive configurations in Chapters 3 and 4 are suitable for CB PWM scheme reorganisation, which would lead to different roles for the two inverters, with regard to phase voltage fundamental control and low-order harmonic content reduction. The basic principle of the proposed modifications is to perform PWM switching with one VSI only, while the remaining inverter contributes to the final phase voltage by holding a constant voltage level (staircase modulation). It is explained that only the 2L-OeW-2L drive with r = 1 and the 3L-OeW-2L drive with r = 2 are suitable for this kind of control, since coupled modulation in these cases does not rely on PWM operation of the both VSIs at the same time. Next, the possibility to omit the dc source at the PWM (conditioning) inverter side is investigated. Although analysis shows that both inverters are contributing to the phase voltage fundamental, i.e. torque producing

component, it is shown that so-called dc-link voltage boosting is taking place in both topologies, which enables full speed range of operation with only one dc source, that has the same dc-link voltage as in the dual supply configuration case. This dc source supplies the bulk inverter, which operates in staircase mode, making further hardware cost reduction possible, by using low-frequency switching devices for bulk inverter realisation. The second, conditioning inverter operates in PWM mode. For this OeW drive realisation, balancing of the conditioning inverters' dc-link capacitor voltage is essential, in order to keep the desired dc-link voltage ratio. This offers a possibility to obtain harmonic performance equivalent to that obtained with a corresponding dual supplied OeW drive. However, elimination of one dc source limits the drive ability to operate under loaded conditions, especially in the case of the 2L-OeW-2L drive. On the other hand, the proposed reconfiguration in the 3L-OeW-2L drive case results in much higher bulk inverter contribution to phase voltage fundamental component, as well as lower harmonic pollution of the three-level staircase modulation, when compared to the two-level counterpart. As a result, a single dc source supply of 3L-OeW-2L drive is more suitable for bulk and conditioning operation, which is experimentally verified.

Chapter 7

DYNAMIC PERFORMANCE OF OPEN-END WINDING DRIVES UNDER THE CLOSED-LOOP CONTROL

7.1. INTRODUCTION

It has been demonstrated that open-end winding drives can be a suitable solution for high-power applications, with regard to harmonic performance. Furthermore, this concept offers several benefits, as discussed in Chapter 1. Probably the greatest motivation for the OeW drive is the utilisation of simpler inverter structures, where the structure corresponds to off-the-shelf two- and three-level power modules. Although the OeW drive utilises two isolated dc sources, their voltage ratings are lower, when compared to a single dc source for a single-sided multilevel inverter (with the same overall V_{dc}). From a hardware complexity point of view, it is shown that even greater savings can be achieved, using certain dc-link voltage ratios, which leads to higher number of voltage levels, since equivalent single-sided solutions require more power modules, dc-link capacitors, etc. Drawbacks, introduced in these cases by simultaneous switching of two inverters, can be mitigated using a modified modulation strategy, as shown in Chapters 3 and 4. Solutions for issues related to dc-link capacitors voltage stability can be found in the modulation strategy design as well, since results in Chapter 5 indicate that superior harmonic performance of coupled PWM schemes can be traded for dc-link voltage stability by using decoupled methods (only in certain modulation index ranges). At the same time, it seems that all analysed configurations, in combination with coupled modulation strategies, can be interesting for some high-power applications, in which the complete speed range is not expected to be required most of the time.

The need to implement a novel drive configuration and apply a certain modulation strategy is not only related to harmonic performance. Nowadays, a number of industrial drives are under closed-loop control, which maximises their dynamic response and offers a higher controllability of relevant (output) drive parameters, when compared to an open-loop control approach. Unfortunately, the majority of novel drive configurations and modulation strategies presented in the literature are not tested in terms of closed-loop control dynamic performance. This can be justified with the fact that the inverter structure and corresponding modulation strategy should have no effect on the drive speed, position and torque control. However, vector control results in much faster dynamic response and maximal torque during speed changes is expected during speed transients. As a consequence, a sinusoidal shape of phase voltage reference cannot be claimed any more at all times, since acceleration from 0 to a nominal speed of, for example 1500 rpm, i.e. phase voltage fundamental frequency change from 0 to 50 Hz, is expected to take place in a very short time interval. At the same time, the phase angle between produced stator voltage and current varies over a very wide range, even if no external load is applied. For these reasons, dynamic performance of several previously analysed OeW drive configurations is examined for the case of closed-loop speed control. Due to its simplicity and ease of implementation, indirect rotor flux field oriented control (FOC) is chosen for this testing.

Additionally, the most dominant low-order current harmonics in the *x-y* plane are suppressed using PI current controllers. Initial results for the 2L-OeW-2L drive with $r = 2$ and PD PWM under closed-loop control are published in [Darijevic and Jones (2014), Darijevic et al. (2016)]. In this chapter, FOC performance for both 2L-OeW-2L and 3L-

OeW-2L drives with coupled and decoupled PWM schemes is analysed. The 3L-OeW-2L drive under B&C control is also tested in the same manner.

7.2. CLOSED-LOOP CONTROL

7.2.1. INDIRECT ROTOR FLUX FIELD ORIENTED CONTROL

The FOC algorithm is shown in Fig. 7.1. Inputs of the control are speed reference ω^* and i_d^* which corresponds to rotor flux. According to the open-loop steady state phase current amplitude in no load conditions, it is found that i_d^* = 2.7 A should be applied. Feedback signals, i.e. rotor mechanical speed ω, rotor position θ and phase currents i_k are obtained using dSPACE boards, as explained in Appendix 2. In order to obtain stator current vector components in a rotational reference frame, decoupling and rotational transformations are applied. The latter uses measured θ and estimated slip angle $\theta_{slip} = i_q^*/(T_r \cdot i_d^*)$ for rotor flux vector position estimation, $\theta_e = \theta + \theta_{slip}$. The rotor time constant is equal to $T_r = 1/(R_r \cdot (L_{\gamma r} + L_m))$, while machine parameters can be found in Table A1.1. The structure of the PI controller used in the speed control loop is the same as in Fig. 6.9, but without conditioning of error signal with modulation index value. Its parameters are: K_P = 0.205 A s/rad, K_I = 0.5 A/rad. The anti-windup constant is K_{aw} = 6 rad·A^{-1}·s^{-1}, while the SAT block has limits of ±5 A.

The influence of the multiphase drive topology on FOC implementation comes down to the usage of different transformation matrices, when compared to the three-phase drive case. The decoupling transformation is performed using the following expression ($\gamma = 2 \cdot \pi/5$):

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_x \\ i_y \\ i^+ \end{bmatrix} = \sqrt{\frac{2}{5}} \cdot \begin{bmatrix} 1 & \cos(\gamma) & \cos(2\gamma) & \cos(3\gamma) & \cos(4\gamma) \\ 0 & \sin(\gamma) & \sin(2\gamma) & \sin(3\gamma) & \sin(4\gamma) \\ 1 & \cos(2\gamma) & \cos(4\gamma) & \cos(6\gamma) & \cos(8\gamma) \\ 0 & \sin(2\gamma) & \sin(4\gamma) & \sin(6\gamma) & \sin(8\gamma) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \times \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} \tag{7.1}$$

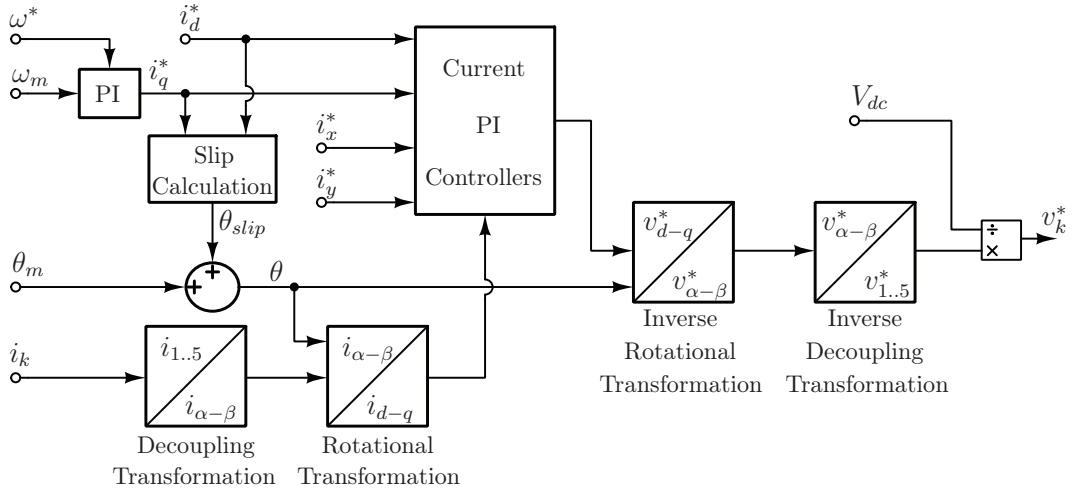


Fig. 7.1. Rotor flux field oriented control algorithm.

The rotational transformation is similar to one used in three-phase drives, since rotation is applied with respect to the current components in the first plane only:

$$\begin{bmatrix} i_d \\ i_q \\ i_x \\ i_y \\ i^+ \end{bmatrix} = \sqrt{\frac{2}{5}} \cdot \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) & 0 & 0 & 0 \\ -\sin(\theta_e) & \cos(\theta_e) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_\alpha \\ i_\beta \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} \tag{7.2}$$

The final phase voltage references are obtained using inverse transformations and normalisation with measured value of $V_{dc} = V_{dc1} + V_{dc2}$.

7.2.2. CLOSED-LOOP CURRENT CONTROL AND SUPPRESSION OF LOW-ORDER PHASE CURRENT HARMONICS

Multiphase drive structure leads to additional requirements of controlling stator current components in *x*-*y* plane. Since these are not torque producing components, their references are set to be zero. Closed-loop current control in Fig. 7.1 is shown in more detail in Fig. 7.2. The structure of PI controllers is the same as in Fig. 6.9. Two of them are used in the first plane, for i_d and i_q current components, which is denoted as i_d (i_q) in Fig. 7.2. Standard decoupling is included between these two currents. Initially, the same approach is applied to the i_x (i_y), which requires only two PI controllers in the second plane. However, due to higher ripple content, which mainly depends on the dead-time influence on low-order current harmonics, this approach is not found to be satisfactory. Therefore, a different approach is considered, which relies on separate control of the two most dominant current harmonics in the *x*-*y* plane. As shown in Fig. 7.2, this requires additional rotational transformations, which in essence result in formation of two fictitious planes. The planes rotate synchronously with the 3rd and 7th current harmonic vectors, which enables separate control of their *x* and *y* components, denoted as i_{x3} (i_{y3}) and i_{x7} (i_{y7}), respectively. This effectively reduces the ac components in the error signal of the PI controllers, while its dc component corresponds to harmonic *x* and *y* projections in two planes, since references i_x^* and i_y^* are always equal to zero. Although this requires four PI controllers, in order to control i_{x3}, i_{y3}, i_{x7} and i_{y7} separately, the algorithm is still very simple and easy to extend to an arbitrary number of harmonics that should be suppressed. Empirical results show however that control of the 9th harmonic in the first plane and other higher harmonics does not lead to significant improvement in harmonic performance. Hence, only the 3rd and 7th current harmonics are processed in this manner. The parameters of the current controllers are given in Table 7.1.

Table 7.1. Parameters of PI controllers in Fig. 7.2.

PI controller applied to	K_P	K_I	K_{aw}	*SAT* limits
i_d (i_q)	40 V/A	6000 V·A^{-1}s^{-1}	5000 A/V	±500 V
i_{x3} (i_{y3})	25 V/A	1000 V A^{-1}s^{-1}	5000 A/V	±50 V
i_{x7} (i_{y7})	10 V/A	200 V A^{-1}s^{-1}	5000 A/V	±50 V

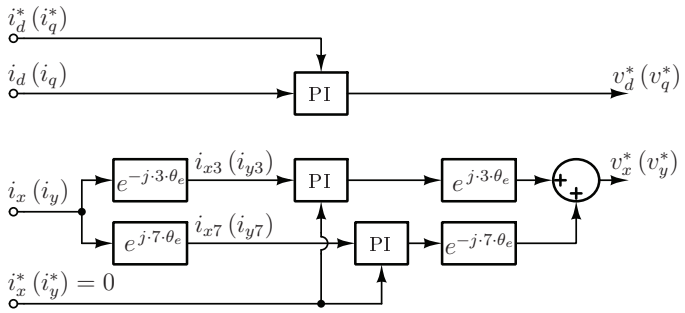


Fig. 7.2. Closed-loop current control algorithm.

7.3. EXPERIMENTAL RESULTS

7.3.1. DYNAMIC PERFORMANCE OF THE 2L-OEW-2L DRIVE

Firstly, the dynamic performance of the 2L-OeW-2L topology is tested under indirect rotor flux oriented control. Although Chapters 3 and 5 show that equal dc-link voltage ratios result in easier drive control, without issues such as dead-time spikes and dc-link capacitor overcharging, for this testing $r = 2$ is chosen, which leads to a four-level configuration, but also requires a more complex modulation strategy (PD PWM with SAR/SRA implementation) and the use of a controllable current bidirectional dc source for V_{dc2} formation. As in the case of previously reported experimental verifications, the overall dc-link voltage is set to be $V_{dc} = 600$ V, which leads to $V_{dc1} = 400$ V and $V_{dc2} = 200$ V. Experimental results for the case when two inverters are modulated using PD PWM are shown in Fig. 7.3. Speed transients, shown in Figs. 7.3a and 7.3b demonstrate that the proposed modulation algorithm is suitable for high-performance FOC control. Even fast changes between single-sided and multilevel operation, which require instantaneous change of R_{offset} from 1/6 to 1/2 when $M = 0.35$, do not cause any negative impact on the dynamic performance. For example, in Fig. 7.3b, the drive initially operates with steady state speed $n = 1350$ rpm, where n is equal to $2 \cdot \pi / 60 \cdot \omega$. This n value corresponds to $M = 0.9$, meaning that both inverters operate during one fundamental period. At $t = 3$ s speed reversal is commanded, $n^* = -1350$ rpm. During the transient, the drive dynamically changes its operating mode twice: for 1350 rpm $\geq n >$ 525 rpm drive operates in multilevel mode, for 525 rpm $\geq n \geq -525$ rpm only VSI_2 is modulated, while VSI_1 forms star connection according to SAR algorithm, and finally multilevel operation is performed again for -525 rpm $> n \geq -1350$ rpm. A controllable power supply is used for VSI_1 dc-link supply. This kind of dc source is able to compensate small changes in dc-link voltage, while implementation of digitally controlled braking (Appendix 2) additionally ensures that dc-link voltage ratio is kept constant at all times. This applies for drive deceleration as well, since only a small increase of V_{dc1} can be detected. V_{dc2} is formed using a linear four quadrant power source, due to the overcharging problem, which also ensures stable VSI_2 dc-link voltage during the deceleration transient. Fig. 7.3c shows the drive response to the step loading and unloading test. For this purpose, a dc machine is mechanically coupled with the five-phase machine under test. Electrical terminals of the dc machine are connected to a resistor bank via a mechanical switch. This enables step loading of the induction motor, with torque proportional to the rotor speed. Sudden change of load causes a reduction of drive speed which is quickly regulated thanks to the closed-loop speed control. The load causes an increase of i_q component to about 3 A. In the same manner, the control quickly eliminates the error in speed introduced by removal of the load.

The dynamic response of the drive is tested under decoupled modulation. Results for the case of URS1 PWM scheme are shown in Fig. 7.4. Acceleration from 0 to 1500 rpm shows that in the range $0 \leq n \leq 525$ rpm $v_{11}^* = 0$, meaning that the VSI_1 forms a star connection at its side of the windings. At the same time, VSI_2 operates in PWM mode. For $n >$ 525 rpm v_{21}^* has constant amplitude. Comparison of both speed tests, i.e. for speed step and reversal command in Fig. 7.4 with corresponding ones in Fig. 7.3, shows that transient between single-sided and multilevel operation modes results in somewhat smoother phase voltage reference shape in the case of decoupled modulation. This is a consequence of differences between PD and URS1 PWM. In the first case, when M is close to, but still higher then 0.35, VSI_1 holds a constant voltage level in reference zones 1 and 2. For the same M, URS1 operates both VSIs in PWM mode, which provides higher controllability over the phase voltage instantaneous values. In both cases, CMV dc component is changed during transient, from -100 V to 100 V. This is shown in Fig. 7.5 (CH1 trace shows M, CH2: v_1^*, CH3: v_{n2n1}, CH4: i_1). The CMV transient takes about ten switching periods, which also has an influence on modulation strategy performance around $M = 0.35$.

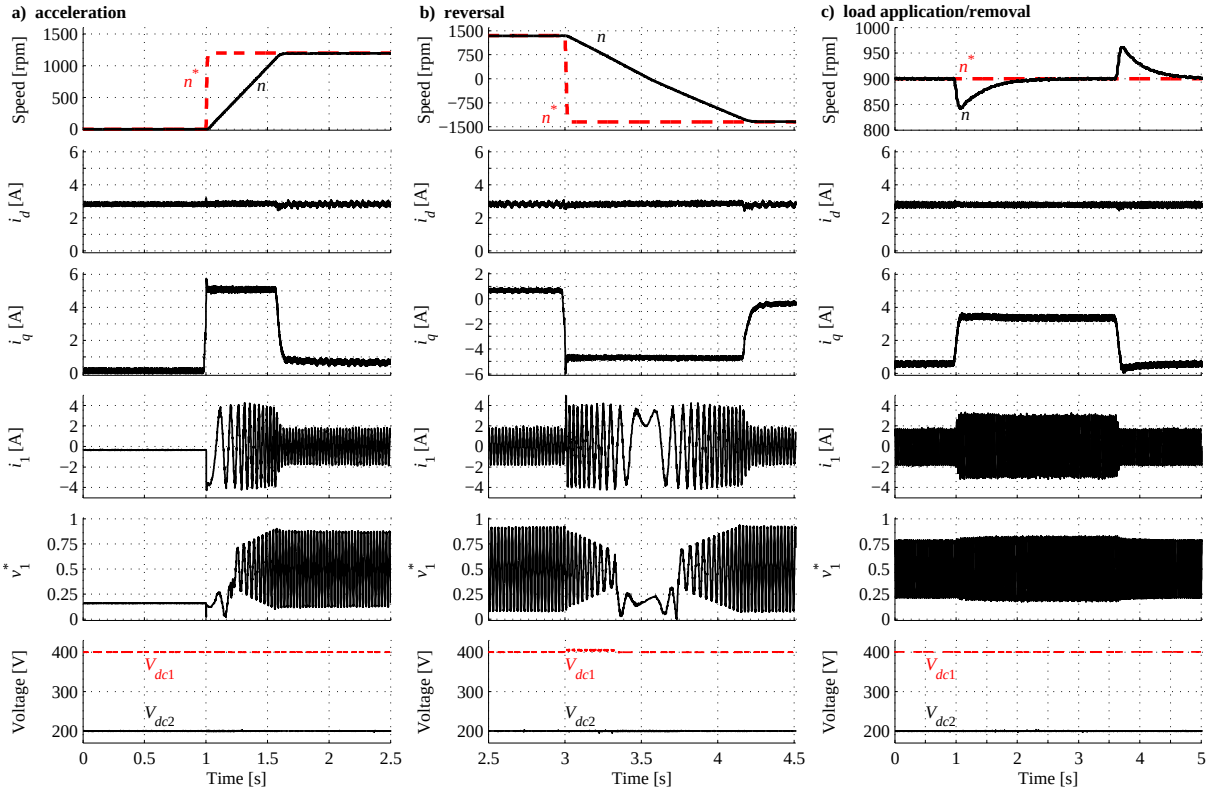


Fig. 7.3. FOC response of 2L-OeW-2L drive (r = 2) and PD PWM with SAR and SRA: acceleration from 0 to 1200 rpm (a), reversal from 1350 rpm to −1350 rpm (b) and load application/removal at n = 900 rpm (c). Top to bottom: drive speed, i_d, i_q, i_1, v_1^*, and dc-link voltages.

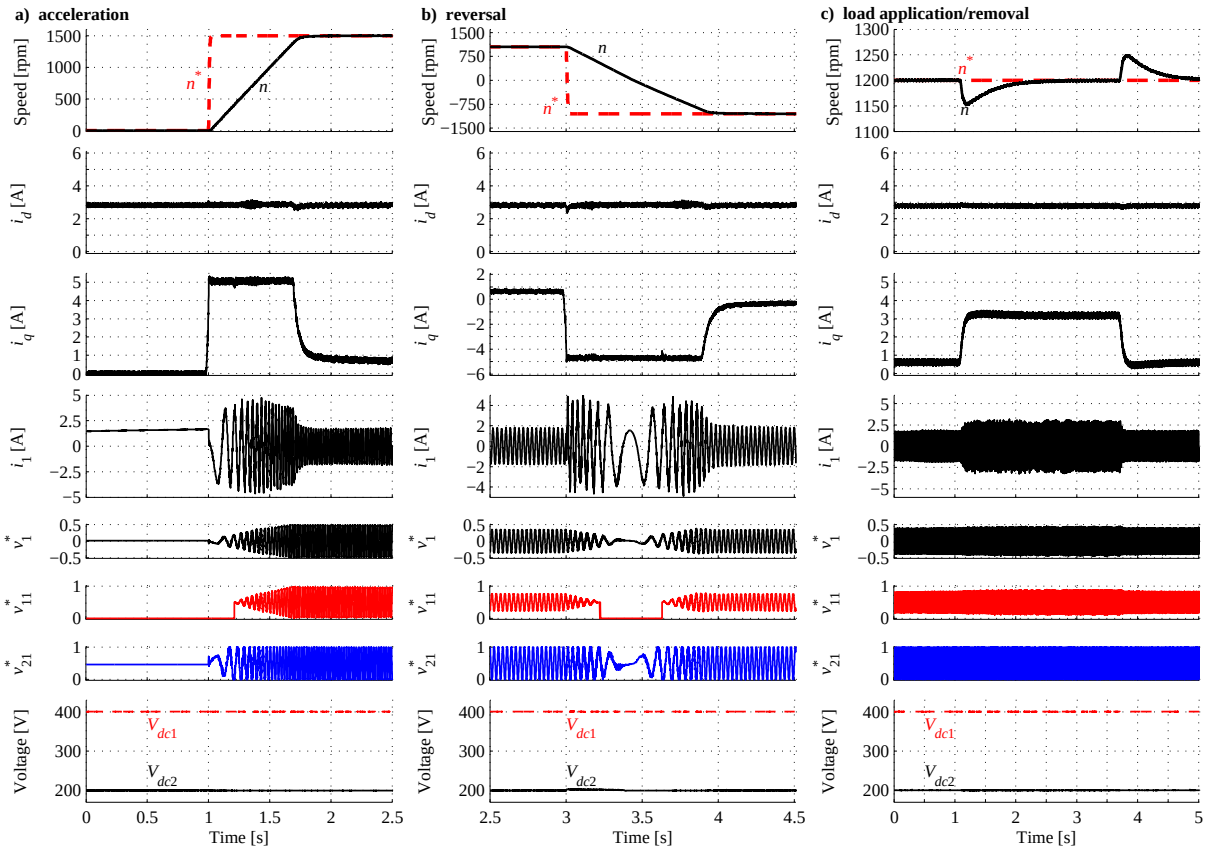


Fig. 7.4. FOC response of 2L-OeW-2L drive (r = 2) and URS1: acceleration from 0 to 1500 rpm (a), reversal from 1050 rpm to −1050 rpm (b) and load application/removal at n = 1200 rpm (c). Top to bottom: drive speed, i_d, i_q, i_1 v_1^*, v_{11}^* and v_{21}^* and dc-link voltages.

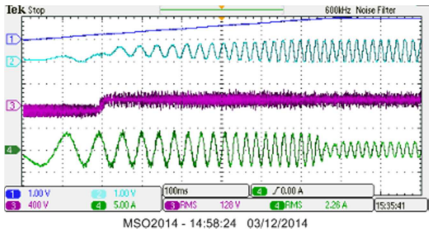


Fig. 7.5. Common mode voltage transient during acceleration under FOC control (example is for PD PWM). Traces: CH1 M (normalised to 1 p.u. = 1 V, 1 V/div), CH2 v_1^* (1 p.u. = 1 V, 1 V/div), CH3 v_{n2n1} (400 V/div), CH4 i_1 (5 A/div).

7.3.2. DYNAMIC PERFORMANCE OF THE 3L-OEW-2L DRIVE

The same dc-link voltage ratio is chosen for 3L-OeW-2L drive dynamic performance testing. This enables comparison with the previously considered 2L-OeW-2L drive. Although the four-level configuration is again utilised, the 3L-OeW-2L drive does not suffer from dead-time spikes or dc-link capacitor voltage stability issues. Hence, a simpler realisation of dc sources is used in this case, based on three-phase diode rectifiers, as in Fig. 5.13 (parameters can be found in Appendix 2). Results in Figs. 7.6 and 7.7, obtained with PD and URS1 PWM, respectively, show that the small dc-link voltage fluctuations do not have a significant impact on the dynamic performance of the drive. Digitally implemented PWM braking allows only small increase of V_{dc2} during deceleration, while V_{dc1} is kept stable at all times. This can be expected since VSI_1 operation during deceleration quickly leads to low duty ratios, i.e. the amount of charge that can be returned on that drive side is constantly dropping according to the analysis in Chapter 5. This makes dc-link control easier on that drive side, using a braking resistor. It can be concluded that the 3L-OeW-2L with $r = 2$ is able to deliver the expected FOC performance, with both coupled and decoupled modulation strategies. This also confirms that all dc-link voltages are stable (Chapter 5) for a wide range of ϕ, combined with fast M variations, which is a requirement of high-performance control.

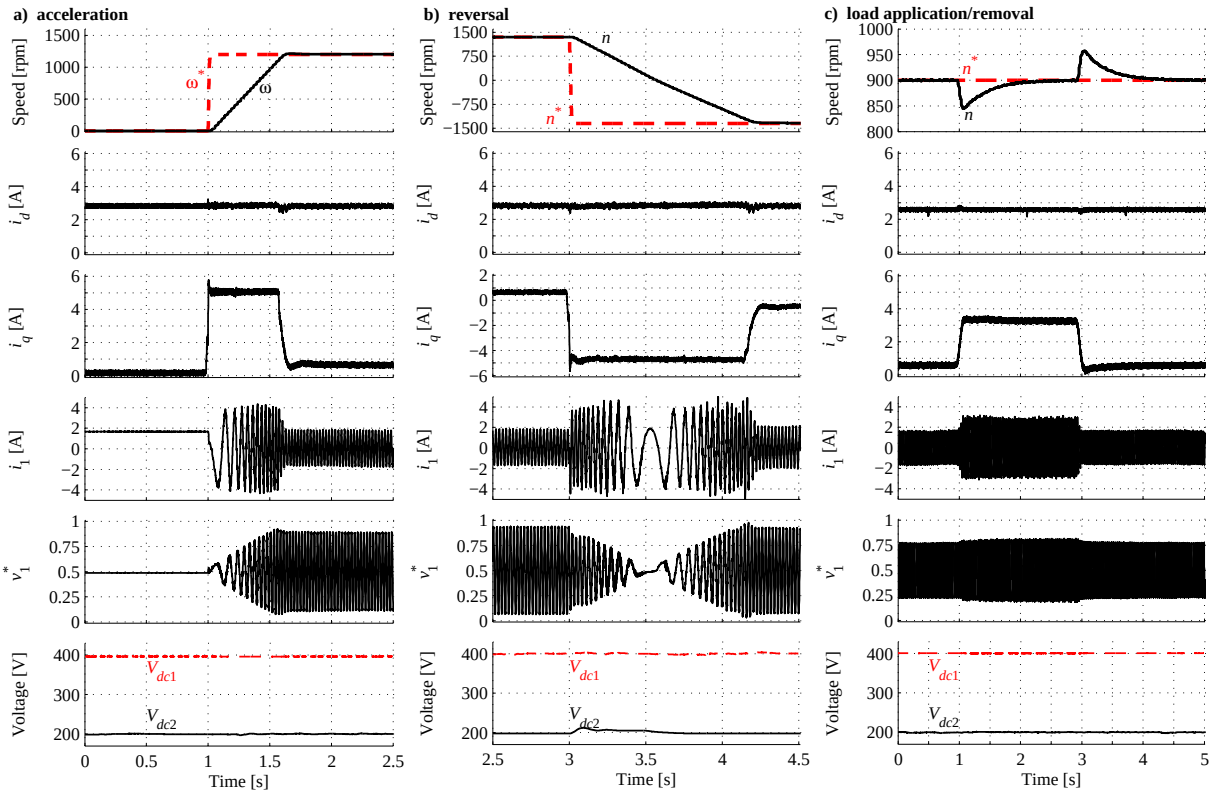


Fig. 7.6. FOC response of 3L-OeW-2L drive ($r = 2$) and PD PWM: acceleration from 0 to 1200 rpm (a), reversal from 1350 rpm to −1350 rpm (b) and load application/removal at $n = 900$ rpm (c).

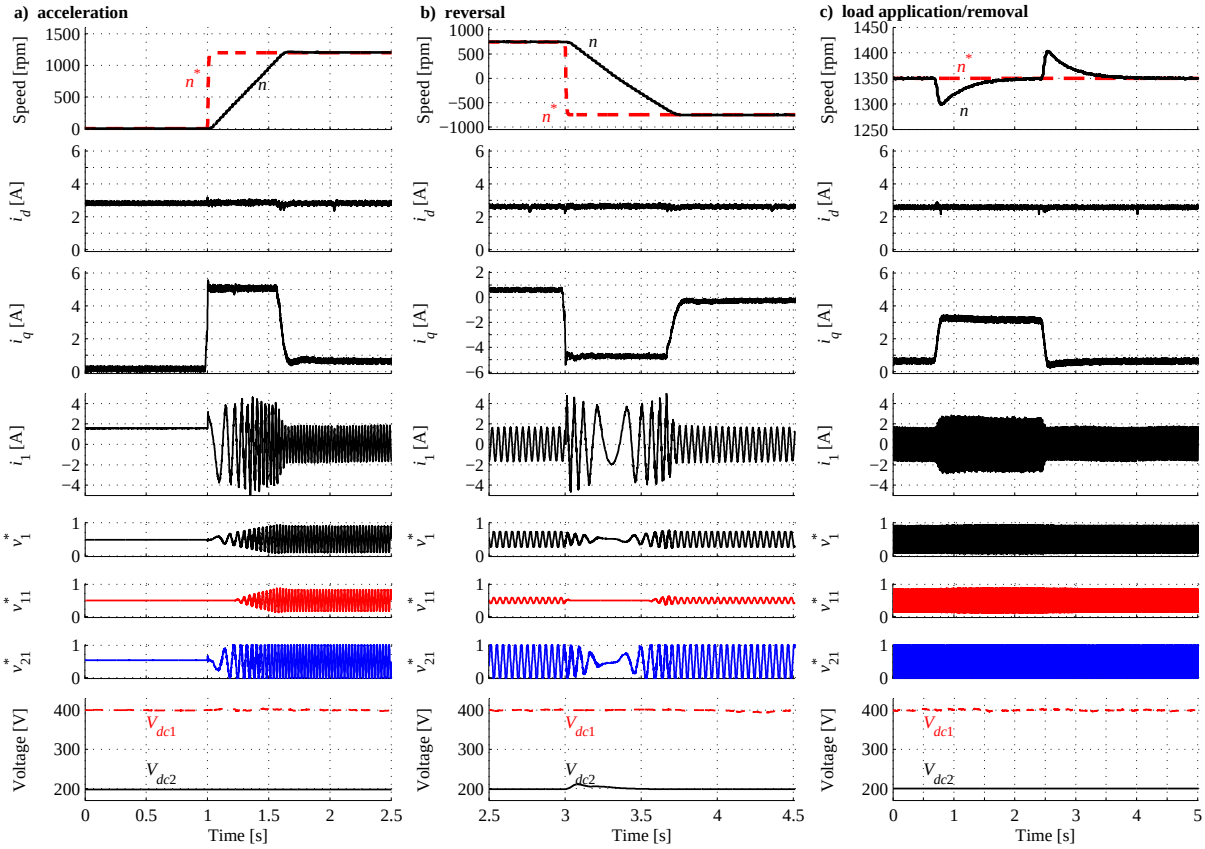


Fig. 7.7. FOC response of 3L-OeW-2L drive (r = 2) and URS1: acceleration from 0 to 1200 rpm (a), reversal from 750 rpm to −750 rpm (b) and load application/removal at n = 1350 rpm (c). Top to bottom: drive speed, i_d, i_q, i_1 v_1^*, v_{11}^* and v_{21}^* and dc-link voltages.

7.3.3. DYNAMIC PERFORMANCE OF THE 3L-OEW-2L DRIVE WITH BULK AND CONDITIONING CONTROL

The 3L-OeW-2L topology with a single dc source, dc-link voltage ratio of 2:1, and operating under B&C control, should lead to a harmonic performance similar to that obtained using PD PWM for the same drive configuration when two dc sources are used (Chapter 6). Absence of the dc source at the VSI_2 side introduces an additional requirement, in terms of maintaining v_{cdc2} = 200 V at all times, regardless of the commanded speed and applied load. This leads to a trade-off between three conflicting requirements: harmonic performance, v_{cdc2} stability and drive dynamic performance. The experimental results are shown in Fig. 7.8. It can be seen that the drive is able to deliver the expected dynamic performance for both speed transient and load disturbance rejection tests. On the other hand, v_{cdc2} voltage is less stable when compared to V_{dc2} voltage in Figs. 7.6 and 7.7. In order to investigate v_{cdc2} balancing performance during FOC transients, the braking chopper is used only as a protection, i.e. not for keeping r constant. In other words, v_{cdc2} voltage stability is here completely determined with B&C algorithm (Chapter 6). During transients, for $M \leq 0.35$, only VSI_1 operates in PWM mode (f_S = 1 kHz). Transition between single-sided and multilevel operation is similar to the one obtained with the 2L-OeW-2L drive with r = 2 and PD PWM. This leads to a somewhat increased ripple content of i_d and i_q during transients, caused by non-constant r value. Tests also show that the speed-torque characteristic of the drive is influenced by the absence of the lower dc-link voltage dc source. This can be seen when n^* = 1500 rpm (M = 1) and a high load torque is applied. This leads to a high value of σ, produced by the voltage balancing algorithm. Current distortion in this situation is visible in Fig. 7.9, although v_{21} demonstrates that VSI_2 dc-link voltage (v_{cdc2}) is stable.

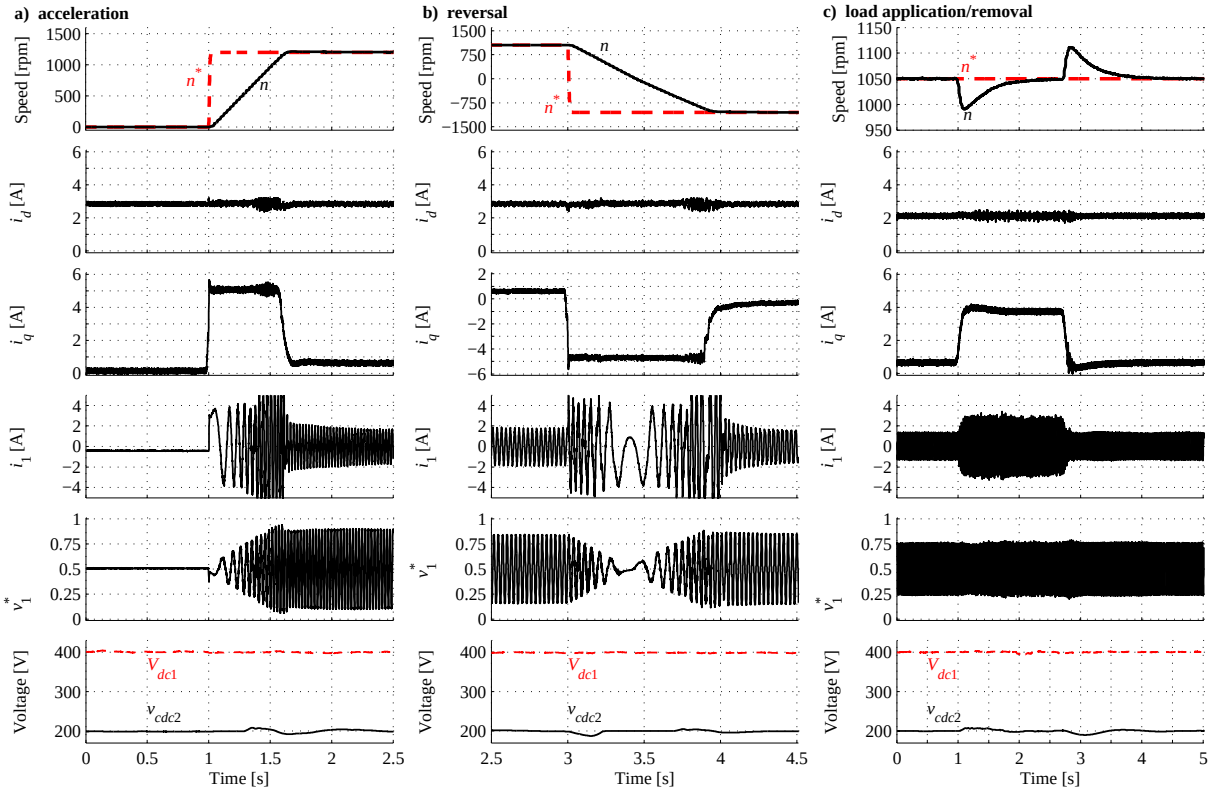


Fig. 7.8. FOC response of 3L-OeW-2L drive (r = 2) and B&C: acceleration from 0 to 1200 rpm (a), reversal from 1050 rpm to −1050 rpm (b) and load application/removal at n = 1050 rpm (c). Top to bottom: drive speed, i_d, i_q, i_1, v_1^*, and dc-link voltages.

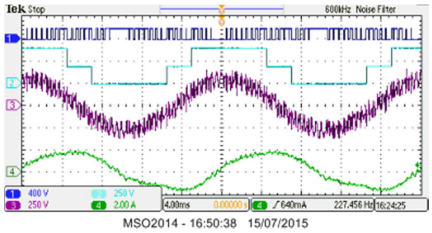


Fig. 7.9. Experimentally obtained steady state waveforms for the first drive phase for 3L-OeW-2L drive with B&C control and M = 1, when heavy load is applied. Traces from top to bottom: CH1 v_{21} (400 V/div), CH2 v_{11} (250 V/div), CH3 v_1 (250 V/div), CH4 i_1 (2 A/div).

7.4. CLOSED-LOOP CURRENT CONTROL PERFORMANCE

As explained in subsection 7.2.2, current controllers aimed for suppression of the most dominant low-order harmonics are incorporated in the FOC control scheme. Although their performance is not the primary topic of this research, THD(M) dependencies are obtained for this kind of control as well, for the two most interesting cases.

The first one is the 2L-OeW-2L drive with PD PWM, which requires SAR and SRA implementation, according to the issues related to dead-time spikes. As shown in Chapter 3, SRA leads to somewhat increased low-order current harmonics, since the effective dead-time interval is doubled in reference zone 2. Chapter 3 also shows that this drawback can be eliminated if closed-loop current control is applied. The second investigated case is the 3L-OeW-2L drive with r = 2 and B&C control. In this case, the lower dc-link voltage capacitor balancing algorithm introduces a small reference offset, which enables control of C_{dc2} voltage, but also leads to increased harmonic distortion. This opens the question if the additional distortion can be suppressed using closed-loop current control. Results for both cases are shown in Fig. 7.10.

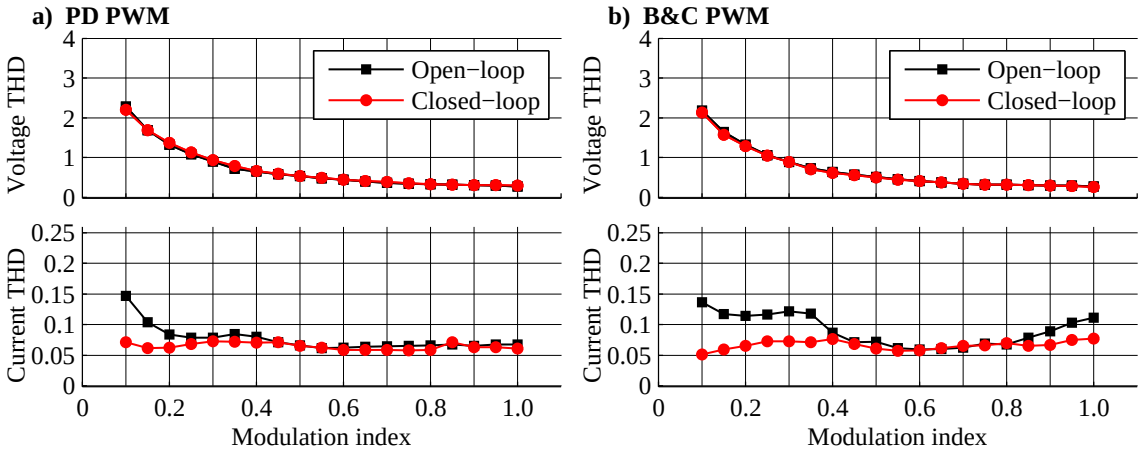


Fig. 7.10. Experimental results: comparison of obtained THD(*M*) dependencies with open- and closed-loop current control, for 2L-OeW-2L with $r = 2$ and PD PWM (a) and 3L-OeW-2L with $r = 2$ and B&C (b).

Open-loop THD(*M*) dependencies, already shown in Chapters 3 (for PD PWM) and 6 (for B&C control), are shown here just for comparison purposes. Closed-loop measurements are obtained in steady state operation under FOC and with closed-loop current controllers. Clearly, reduction of the 3rd and 7th current harmonics leads to great improvement of the phase current THD for low and high modulation index values, i.e. in the regions where the original modulation schemes had the worst harmonic performance. Although implementation of a more sophisticated current controller may lead to further improvement, it seems that the remaining harmonic pollution is mainly caused by switching harmonics, due to very small variations in the phase current THD throughout the *M* range when the proposed current control method is applied.

7.5. SUMMARY

This chapter discusses the experimental results obtained with several previously analysed OeW configurations and corresponding modulation strategies, under closed-loop speed control. In particular, indirect rotor flux oriented control is applied to a 2L-OeW-2L drive and a 3L-OeW-2L drive with $r = 2$, in combination with different modulation strategies. In all analysed cases, dynamic performance is in agreement with expectations. Detailed analysis of results shows that differences in modulation strategy complexity have very small influence on the speed transients in the vicinity of *M* values which are at the border between single-sided and multilevel operation modes. These transitions are performed more smoothly when both inverters are operated with sinusoidal references (URS1), when compared to complex coupled control, although the latter results in better steady state harmonic performance. From that point of view, one of the future work topics may be related to optimal OeW control, which combines different modulation methods, with regard to their impact on drive dynamic response and steady state harmonic performance. This is discussed in more detail in the section about future work, in Chapter 8.

Additionally, closed-loop current control of phase current harmonics in the second plane is applied. Although the proposed method is very simple, harmonic performance is improved, when compared to the results obtained in the case of open-loop *V*/*f* control. This is investigated in detail for two cases, where phase current harmonic content is influenced the most by modulation algorithms: PD PWM for 2L-OeW-2L drive and B&C control of 3L-OeW-2L drive ($r = 2$ in both cases).

When compared to the widely published single-sided drives behaviour under closed-loop control, it is clear that the OeW drive concept offers the same performance, which makes this concept equally relevant for high-performance industrial and automotive high-power applications.

Chapter 8

CONCLUSIONS AND FUTURE WORK

8.1. SUMMARY AND CONCLUSIONS

This thesis addresses modulation strategies for multilevel five-phase open-end winding drives. Two OeW topologies with isolated dc-links are analysed. The first one, is the simplest OeW configuration and employs two two-level inverters (2L-OeW-2L drive) while the second one consist of one three-level and one two-level inverter (3L-OeW-2L drive). Both drives are able to produce different number of voltage levels, which mainly depends on the ratio between the dc-link voltages. Analysis of the equivalent drive models, a method developed during this research, shows that the 2L-OeW-2L topology can be considered as a three-level drive, if equal dc-link voltages of two inverters are used, while any other dc-link voltage ratio leads to utilisation of four voltage levels [Darijevic et al. (2013a), Darijevic et al. (2013b), Darijevic et al. (2016)]. The 3L-OeW-2L topology can be configured as a four-, five- or six-level drive, by using dc-link voltages in the ratio 2:1, 1:1 or in any other, respectively [Darijevic et al. (2015a), Darijevic et al. (2015b), Darijevic et al. (2015c)]. Hence, the dc-link voltage ratio is considered as a degree of freedom, enabled by the OeW drive structure. Thanks to this parameter, both drives are able to utilise a higher number of voltage levels, when compared to a single-sided solutions with the same component count and hardware complexity. Results in this thesis also show that a further reduction of hardware complexity is possible, but only in certain cases, where one dc-link voltage source can be omitted from the circuitry [Darijevic et al. (2015d)]. In this research only CB PWM schemes are considered. Since duality between certain SV and CB PWM schemes is known [Dordevic (2013), Dordevic et al. (2013)], methods that are easier for development and less computationally demanding seem to be a logical choice. Besides, the structure of the CB PWM schemes leads to a conclusion that the presented modulation strategies are easily extendable to an arbitrary number of phases. This makes the contributions of this thesis more general and the developed CB PWM methods suitable for a wider application range.

The thesis begins with a short introduction, where motivation and the main aims of this research are explained. Chapter 2 provides a survey of relevant literature, which is used as a starting point for this research. It also shows that topics covered in this thesis have not been investigated so far and that the herein presented results, as well as the developed analysis methods, are an original contribution to the overall knowledge in this research field.

The harmonic performance of modulation strategies for the 2L-OeW-2L drive is analysed in Chapter 3, for different dc-link voltage ratios. Modulation strategies are divided into two major groups. The first group comprises modulation schemes developed from modulation strategies for single-sided multilevel inverters. Consequently, the OeW drive is considered as a single entity, which maximises the harmonic performance quality of the drive. However, these so-called coupled modulation methods, in some cases require simultaneous PWM operation in inverters' legs connected to the opposite sides of the same stator winding, which causes triggering of unwanted voltage levels during dead-time intervals [Darijevic et al. (2013b)]. As a consequence, the harmonic performance is worse than expected and the modulation strategies require some modifications. Simulation and experimental results in Chapter 3 show that the proposed modifications are able to significantly mitigate this issue. The second group of modulation strategies are those that consider the inverters as separate entities [Jones et al. (2014)]. The overall phase voltage reference is shared between

two two-level carrier based pulse width modulators, in the same ratio as the ratio between corresponding dc-link voltages is. Each inverter is modulated independently, which leads to somewhat worse harmonic performance, when compared to the coupled modulation methods for the 2L-OeW-2L drive.

The same approach to modulation strategy development is applied in Chapter 4 for the 3L-OeW-2L drive case. Due to the higher number of utilised voltage levels, differences between harmonic performances obtained with coupled and decoupled modulation methods are smaller. The same conclusion comes from comparison of dead-time spike influence on coupled modulation strategy harmonic performance in the case of 2L-OeW-2L and 3L-OeW-2L drive: higher number of voltage levels utilised in the latter drive case reduces the impact of this issue on phase voltage and phase current harmonic content.

Results in Chapters 3 and 4 yield several conclusions that are common to both topologies. Firstly, dc-link voltage ratios that result in equidistant voltage levels lead to the best harmonic performance and more uniform THD dependencies on modulation index, when compared to other cases. Secondly, only one dc-link voltage ratio per topology leads to the utilisation of all phase voltage levels without employing simultaneous switching of the inverters. This always results in the lowest number of voltage levels obtainable by the topology. In particular, a dc-link voltage ratio 1:1 in the case of 2L-OeW-2L drive leads to utilisation of only three equivalent voltage levels, while the 3L-OeW-2L topology produces its minimal number of levels (four) if the dc-link voltages are in ratio 2:1. At the same time, only in these two cases, dead-time spikes do not occur.

Influence of the proposed modulation strategies in Chapters 3 and 4 on stability of dc-link voltages is analysed in Chapter 5. A novel approach, based on the linearized drive models under the sinusoidal phase current approximation is introduced, in order to derive the dependencies of dc-link current mean values on relevant drive parameters, such as modulation index and phase angle between stator phase voltages and currents. Indicatively, coupled modulation methods developed for OeW configurations in which dc-link voltage ratio is used in order to maximise the number of voltage levels, suffer from dc-link voltage instability. Together with the analysis of their harmonic performances in Chapters 3 and 4, this finding yields a general conclusion that coupled modulation schemes are optimal when the dc-link voltage ratio is the same as the ratio between individual inverters' number of voltage levels reduced by one. On the other hand, the same cannot be said of decoupled modulation schemes, which naturally balance the dc-link voltages, regardless of dc-link voltage ratio. It follows that the decision whether or not to use a decoupled modulation method comes down to a trade-off between harmonic performance and dc-link voltage stability.

Five-phase OeW drives that employ only one active dc source are investigated in Chapter 6. Both 2L-OeW-2L and 3L-OeW-2L drives are analysed in terms of equivalent drive model in the case when PWM switching is performed by only one inverter, while the second one contributes to the phase voltage formation by holding a constant voltage level for a longer period of time. Analysis based on methods introduced in Chapter 5 shows that this so-called modified CB PWM method leads to the different power sharing between two inverters, although harmonic performance is equivalent to that obtained with a conventional CB PWM scheme. This leads to a conclusion that the active part of the dc source used for dc-link voltage formation of inverter that operates in PWM mode can be omitted from the circuitry. Thus, two OeW topologies with a single dc source and isolated dc-links are analysed next: 2L-OeW-2L and 3L-OeW-2L drive with dc-link voltages in ratios 1:1: and 2:1, respectively. In both cases, the inverter that has an active dc supply connected to its dc-link rails, operates in staircase mode and supplies the bulk energy to the rest of the drive (bulk inverter). The second, so-called conditioning inverter has only a dc-link capacitor at its dc side. This inverter is operated in PWM mode at all times, and its main purpose is to eliminate the low-order harmonics introduced by staircase modulation of the bulk

inverter. However, in order to keep harmonic performance at the same level as in the case of the original drive configuration (with two active dc sources), it is mandatory to keep the conditioning inverter dc-link voltage constant, which results in the same dc-link voltage ratio as in the original drive configuration. Analysis shows that the 3L-OeW-2L drive is more appropriate for this kind of modification, since a dc-link voltage ratio 2:1 is used in this case, which leads to the higher contribution of bulk inverter to the phase voltage fundamental when compared to the 2L-OeW-2L case. At the same time, the 2L-OeW-2L drive suffers from an inability to control the conduction angle of the bulk inverter, due to limitations of staircase modulation of the two-level VSI.

Finally, Chapter 7 examines the dynamic performances of the OeW drives, when closed-loop control is applied. Analysis shows that the developed modulation strategies are capable of achieving the required dynamic response. This experimental verification is of significant importance for the adaptation of the OeW concept in future industrial and automotive applications, where high-performance drive control is of great interest.

8.2. FUTURE WORK

Due to practical restrictions related to the project organisation, available resources and time, this research covered only several, but probably the most important, aspects of modulation strategy developments for open-end winding drives. This work can be easily extended to drives that utilise different number of phases, machine types and winding distributions, as well as to topologies that utilise different inverter structures. Probably the most important outcome of this project is the set of analysis methods which might be used for development of CB PWM methods for any other OeW drive configuration. However, the expected benefits from extending this analysis are minimal. Firstly, extension of CB PWM methods for the same drive structure, but for different number of phases is straightforward and the expected novelty and contribution to this field of research is therefore incremental. Secondly, it can be concluded that the rate of harmonic performance improvement drops with increment of the number of voltage levels. That is, the difference in harmonic performance between four-level and three-level drives is lower than between three-level and two-level drives. From this point of view, this kind of extension of the herein presented research might only have practical importance in the case where further increment of the number of voltage levels is a consequence of the power requirements of certain applications. At the same time, it does not seem beneficial to develop alternative modulation strategies based on SV PWM approach, due to the proven duality between the final switching patterns between CB and SV PWM schemes. Still, there are several important topics related to OeW drives, which have not been covered so far:

- Results presented in this thesis show that different modulation strategies offer different benefits. Probably the most obvious case for this are decoupled methods for the 3L-OeW-2L drive. Results in Chapter 4 indicate that URS1 and URS2 offer different harmonic performances for the same modulation index, but it seems to be hard to determine which case is superior in general. Hence, the first topic for future research is related to combining them into a hybrid CB PWM strategy. Practical experience gained during this research showed that modulation algorithms can be easily combined and that transiting between different modulation strategies does not represent a problem, even during fast transients. The final goal for this research is to find an optimal modulation strategy, which satisfies the following criteria: stable dc-link voltages under any operating condition and minimal harmonic distortion. This research topic can be extended to combination of coupled and decoupled modulation schemes as well.
- The second approach to achieve the two above mentioned goals is to introduce the closed-loop dc-link voltage control for coupled modulation strategies. Although this introduces a need for additional controllers and

measurements, similarly to the B&C control case, it is expected that this approach may provide a better trade-off between harmonic performance and dc-link voltage stability, when compared to the previously proposed method.

- Nowadays industrial trends show that further improvement of performance in general is more and more related to parallel and simultaneous research and development of both hardware and software components for given application requirements. When applied to open-end winding drives, this approach can be also used, in order to maximise drive performance. For example, dc-link voltage ratio can be varied during drive operation, if that leads to better efficiency (i.e. elimination of the overcharging problem) and better harmonic performance. Note that existence of a primary dc source and formation of the second, usually lower dc-link voltage level can be performed by using some sort of buck-derived dc-dc converter. At the same time, this approach opens a possibility to utilise both isolated and non-isolated OeW drive structures. Additionally, bidirectional dc-dc converters should be considered as well, especially for the cases where lower dc-link voltage capacitor suffers from overcharging. Namely, in these cases, solutions based on controllable dc sources are capable of preventing lower dc-link voltage overcharging, but only at expense of additional energy losses, as demonstrated in Chapter 5. Hence, the main motivation for this topic is to investigate a possibility to utilise the lower dc-link voltage side surplus current recuperation, by using bidirectional dc-dc converters, which enables the return path between the two dc-links in OeW drive. By designing both hardware and control software for the herein proposed OeW topologies with actively controlled dc-links, one will be able to truly utilise all the benefits offered by dc-link voltage ratio variability.
- Bulk and conditioning control, proposed in Chapter 6, can be improved by introduction of active conduction angle control of the bulk converter. This would lead to even higher contribution to the fundamental component from that OeW drive side, as well as a different solution for modulation indices lower than 0.35. At the same time, comparison of this B&C control approach with the one presented in Chapter 6, would provide a clue as to whether or not extension to different topologies may lead to some benefits. Namely, it has been concluded that the optimal dc-link voltage ratio is equal to the ratio between individual inverters' number of voltage levels reduced by one. Note that the same dc-link voltage ratio is suitable for CB PWM modification leading to a possibility to eliminate one voltage source from the circuitry. Chapter 6 also shows that higher voltage at the bulk inverter side is more suitable, since expected dc-link voltage boosting is lower, with regard to phase voltage fundamental amplitude. From this point of view, it seems logical to extend B&C control to higher dc-link voltage ratios. For example dc-link voltages in ratio 4:1 might be used if five- and two-level converters are combined. When compared to 3L-OeW-2L drive, this would also lead to much finer staircase modulation and lower requirements for conditioning inverter dc-link capacitor voltage rating.
- So far, results presented in this thesis and topics for future work are related to drive operation in healthy conditions. As already explained, both open-end winding and multiphase drive concepts offer a great potential for development of modulation and control strategies aimed for post-fault operation. Some of the possibilities for five-phase open-end winding drive reconfiguration have been examined during this research [Darijevic and Jones (2014b)]. It is shown that some of the post-fault strategies do not require any additional hardware, if OeW concept is used. Many different aspects, such as open-circuit fault, or IGBT fault while corresponding antiparallel diode remains in circuitry, are yet to be investigated. Probably the most important question is whether combination of multiphase and open-end winding concepts leads to a higher controllability and reduction of usually necessary additional hardware for drive reconfiguration when a fault takes place.

Chapter 9

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Appendix 1

NUMERICAL SIMULATION DETAILS AND PARAMETERS

A1.1. PRELIMINARY REMARKS

This appendix describes principles of numerical simulations applied in this research. Having in mind complexity of the proposed topologies and control algorithms, it is clear that numerical simulations are an important step in the overall research process. For this purpose, two software packages are used: Matlab with its integrated Simulink environment and PLECS software, which is similar to Matlab/Simulink, but specialised for simulations in power electronics.

The initial idea was to rely on Matlab's built-in electronic component models, available in Simulink's SimPowerSystems library. However, due to already mentioned circuitry complexity, in many cases this concept has proven not to be useful for several reasons. Firstly, built-in models include various semiconductor and passive component parameters which are not of interest for this kind of numerical simulation, with regard to the analysed effects and time-scale of simulation. This dramatically increases simulation run-time while the necessity of modelling galvanic isolation between two inverters and corresponding dc sources is the main reason of weak models' numerical stability. At the same time, inclusion of an already existing multiphase induction machine model [Dordevic et al. (2010)], derived on a signal and not on an electrical level becomes very complex in Matlab, requiring additional controllable current and voltage sources. As a result, precision of electrical signal calculations is reduced, while the simulation process becomes more computationally demanding, i.e. slower and impractical. Therefore, development of modulation strategies presented in Chapters 3-6, models presented in Chapter 5 and closed loop-control algorithm in Chapter 7 are based on custom-made models of all relevant power electronic devices for the circuits under analysis, without usage of any Matlab SimPowerSystems proprietary blocks and models. Developed models are briefly explained in the following sections.

The modelling approach presented in this appendix, can be easily modified in order to be used in other programming environments. Matlab/Simulink is chosen here mainly because of easier experimental verification, since LJMU EMD multiphase multilevel experimental rig (Appendix 2) is based on dSpace - Matlab integration. PLECS software is used only for further verification of simulation results, when usage of detailed semiconductor models was necessary.

A1.2. FIVE-PHASE INDUCTION MACHINE MODEL

Detailed description of the induction machine model that is used in this research can be found in [Dordevic et al. (2010)]. Parameters that correspond to measured characteristics of two five-phase induction machines available in LJMU EMD laboratory are given in Table A1.1. This machine model has been used in [Satiawan (2012), Bodo (2013), Dordevic (2013)]. Here, the model is slightly improved using pre-calculated values for all the constants in the machine model. This is enabled by degrading the model from a completely general multiphase to the specific five-phase case, with known parameters. As a result, the overall simulation run-time was reduced by about 12%, when compared to the original induction machine model, surrounded with the same power electronics circuitry. Additionally, by setting the initial electrical machine speed to be equal to $2 \cdot \pi \cdot M \cdot f_n$, transient time can be halved. Although in some cases a simple *R-L*

load model can be used, a complete induction machine model is preferred, since it enables easier comparison of steady-state waveforms obtained in experiment, with those obtained in simulations.

Table A1.1. Five-phase induction machine parameters.

Parameter	Value	Description
R_s	3 Ω	Stator resistance
R_r	3 Ω	Rotor resistance
$L_{\gamma s}$	45 mH	Stator leakage inductance
$L_{\gamma r}$	15 mH	Rotor leakage inductance
L_m	545 mH	Magnetising inductance
f_n	50 Hz	Rated frequency
v_n	300 V	Rated phase voltage peak value
p	2	Number of pole pairs
J	0.1 kg·m^2	Rotor inertia
TL_{rated}	8 Nm	Estimated rated torque

A1.3. TWO- AND THREE-LEVEL INVERTER MODELS

Inverters are modelled using Matlab/Simulink *Function Blocks*, which are referred to here as VSI blocks. Gating signals, dc-link voltage(s) and phase currents are considered as inputs, while semiconductors' conduction states and inverter leg voltages are block outputs. Each VSI block accepts separate gating signals for complementary IGBT+D structures, while dead-time implementation ($t_{d\text{-}t}$ = 6 μs) is performed within modulation blocks, according to Figs. 3.8, 3.9, 3.15, 3.35, 4.11-13 and 4.38. Calculations inside VSI blocks are based on *for loop* in which five leg voltages are calculated using *if-then-else* statements which are based on the gating signals and phase current sign. The final leg voltages are obtained as *if-then-else* statement outputs (logical 1 or 0) multiplied by the dc-link voltage level that corresponds with that switching combination. Leg voltage outputs of two VSI blocks represent v_{1k} and v_{2k}, which are used for v_{n2n1} and v_k calculations. In order to avoid so-called algebraic loops, phase current at VSI blocks inputs is delayed for one simulation time-step. Note that this simple model does not include any semiconductor dynamic characteristics, voltage drops, leakage currents and on-state resistance. During development of VSI blocks, simulation results for known modulation strategies are compared with those obtained in PLECS, using detailed semiconductor models. It is shown that inclusion of these parameters has no effect on the generated waveforms of interest, mainly because of the time scale that is used in the analysis. Namely, simulation time-step of 1 μs is proven to be sufficiently small, while all transient times in contemporary semiconductors are usually shorter. Antiparallel diode reverse recovery time (t_{rr}) is comparable with chosen time step, but switching loss analysis is beyond the scope of this research. At the same time, detailed semiconductor models in SimPowerSystems and PLECS often require presence of snubbers in inverter models, in order to avoid large dv/dt and di/dt, which might cause singularities in the overall state space model of the circuitry. Inclusion of snubbers in the model is not only in disagreement with the laboratory rig (Appendix 2) but also increases simulation run-time and computational requirements.

A1.4. MODELLING OF DC SOURCES

For analysis of modulation strategies' harmonic performance, with regard to different drive configurations presented in Chapter 3 and 4, ideal dc source models are used. This practically means that dc-link voltages at inputs of

VSI blocks are set to be constant at any time, while their values are pre-calculated using the *r* parameter in the simulation initialisation Matlab script.

In other cases (Chapters 5 and 6), complete three-phase diode rectifiers with suppressed output voltage ripple are modelled using capacitance values chosen to be the same as for the dc-link capacitors in the experimental rig, $C_{dc1} = C_{dc2} = 1.5$ mF. Considering the extended equivalent model in Fig. 5.1, it should be noted that v_{n1} and v_{n2} are mutually isolated. Three-phase ac sources are modelled with the following system of equations:

$$v_{ac11}(t) = \frac{V_{dc1}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t), \quad v_{ac12}(t) = \frac{V_{dc1}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t - 2 \cdot \pi/3), \quad v_{ac13}(t) = \frac{V_{dc1}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t \cdot t - 4 \cdot \pi/3) \tag{A.1}$$

$$v_{ac21}(t) = \frac{V_{dc2}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t), \quad v_{ac22}(t) = \frac{V_{dc2}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t - 2 \cdot \pi/3), \quad v_{ac23}(t) = \frac{V_{dc2}}{\sqrt{3}} \cdot \sin(2 \cdot \pi \cdot f_g \cdot t \cdot t - 4 \cdot \pi/3) \tag{A.2}$$

If two rectifiers in Fig. 5.1 have their outputs left open, their final output voltages will be equal to:

$$\begin{aligned} v_{out-rect-1}(t) &= v_{p1} - v_{n1} = \max(v_{ac11}(t), v_{ac12}(t), v_{ac13}(t)) - \min(v_{ac11}(t), v_{ac12}(t), v_{ac13}(t)) \\ v_{out-rect-2}(t) &= v_{p2} - v_{n2} = \max(v_{ac21}(t), v_{ac22}(t), v_{ac23}(t)) - \min(v_{ac21}(t), v_{ac22}(t), v_{ac23}(t)) \end{aligned} \tag{A.3}$$

where min/max stands for the function that returns the lowest/highest value from given set of values. The final v_{cdc1} and v_{cdc2} are calculated using modified (5.4):

$$\begin{aligned} v_{dc1}(t_2) &= v_{cdc1}(t_2) = \max(v_{out-rect-1}(t_2), v_{cdc1}(t_1) - \frac{1}{C_{dc1}} \int_{t1}^{t2} \sum_{k=1}^{5} S_{1k}(t) \cdot i_k(t) \cdot dt)) \\ v_{dc2}(t_2) &= v_{cdc2}(t_2) = \max(v_{out-rect-2}(t_2), v_{cdc2}(t_1) + \frac{1}{C_{dc2}} \int_{t1}^{t2} \sum_{k=1}^{5} S_{2k}(t) \cdot i_k(t) \cdot dt)) \end{aligned} \tag{A.4}$$

This modelling approach can be easily extended to the 3L-OeW-2L topology, by representing the overall VSI_1 dc-link voltage as sum of two capacitor voltages, calculated as:

$$\begin{aligned} v_{cdc11}(t_2) &= v_{cdc11}(t_1) - \frac{1}{C_{dc11}} \int_{t1}^{t2} \sum_{k=1}^{5} (S_{1k}^{a}(t) \cdot S_{1k}^{b}(t) \cdot i_k(t)) \cdot dt \\ v_{cdc12}(t_2) &= v_{cdc12}(t_1) - \frac{1}{C_{dc12}} \int_{t1}^{t2} \sum_{k=1}^{5} (\overline{S_{1k}^{a}(t)} \cdot S_{1k}^{b}(t) \cdot i_k(t)) \cdot dt \end{aligned} \tag{A.5}$$

Finally, the dc-link voltages on VSI_1 side are calculated as:

$$\begin{aligned} v_{dc1}(t_2) &= \max(v_{out-rect-1}(t_2), v_{cdc11}(t_2) + v_{cdc12}(t_2)) \\ v_{mp}(t_2) &= v_{cdc12}(t_2) \end{aligned} \tag{A.6}$$

Similarly to this case, v_{cdc2}, i.e. the dc-link voltage of the conditioning inverter in Chapter 6 is calculated. Note that equations (A.1) - (A.6) can be implemented using function blocks and basic Simulink blocks (integrators). Similarly to the case of VSI blocks from the previous section, inclusion of additional parameters, such as capacitors' equivalent series resistance (ESR) is straightforward.

A1.5. SIMULATION PROCEDURE AND DATA ACQUISITION

General simulation parameters given in Table A1.2 are used in all simulations unless specified differently in certain cases. Built-in numerical solver Runge-Kutta of the 4th order is used, with a fixed simulation time-step. Undertaken simulations can be classified in two groups.

In the first group are those aimed for analysis of steady-state harmonic performances. A simulation script (m-file) is used for parameter initialisation, running the simulation and finally data acquisition in text files, which are later used for performance analysis. In those cases, samples of relevant signals (leg voltages, phase voltages, phase currents,

common mode voltage) are taken in every time step during the last fundamental period, while the overall simulated time is set to be equal to min(2 s, 30·T). This was proven to be enough to reach steady-state, if the machine electrical speed is initially set to be equal to $2 \cdot \pi \cdot M \cdot f_n$. Using nested *for loops* (usually 3 or 4), several variables of interest are swept through their full range: M, r, modulation method, SAR/SRA implementation.

The second group of simulations are related to transient analysis. Although simulation parameters are the same, data acquisition is performed in somewhat different manner. Since the initial drive speed is set to be equal to zero, the overall simulation run time is several times longer when compared to the first group of simulations. T_{stop} is set to be equal to min(5 s, 60·T). Hence, sampling of signals relevant for transient analysis (torque, speed, dc-link capacitor voltages, etc) is performed every 200·Δt, while electrical signals relevant for harmonic performance, are sampled every Δt but only during the last fundamental period.

Table A1.2. Model parameters for simulations.

Parameter	Value	Description
Δt	1 µs	Simulation time step
V_{dc}	600 V	The overall dc-link voltage
f_S	2 kHz	VSIs switching frequency
M_{min}	0	Minimal modulation index
M_{max}	1.05	Maximal modulation index
ΔM	0.05	Modulation index step
r_{min}	1	Minimal value of dc-link voltage ratio
r_{max}	4	Maximal value of dc-link voltage ratio
Δr	0.1	dc-link voltage ratio step
T_{stop}	min(2 s, 30·T)	Simulation end time

Appendix 2

EXPERIMENTAL VERIFICATION AND RIG PARAMETERS

A2.1. INTRODUCTION

This appendix describes the experimental setup used in this research. As already mentioned, the control is implemented using a dSPACE platform, which enables rapid prototyping, based on Matlab/Simulink simulation files. This approach also enables real-time control from personal computer, using Control Desk (Unicode standard version 2.6) integrated development environment. The exact workflow of dSpace control files preparation, based on previously developed control algorithms in Matlab/Simulink is explained in Section A2.2. This is followed by descriptions of the two- and three-level inverters, as well as the power sources. Measurement equipment and data acquisition procedure are presented in Section A2.3.

A2.2. EXPERIMENT PREPARATION AND CONTROL HARDWARE DETAILS

Rapid prototyping, enabled by dSPACE and Matlab integration, still requires some modifications, before one can test algorithms developed in Matlab/Simulink simulations on real hardware. Firstly, the power stage of application, that is simulated in Matlab/Simulink (based on Appendix 1), has to be replaced by control blocks that represent dSpace modules (i.e. boards), available in dSpace Simulink library. The core of the system is a dSPACE DS1006 processor board (quad-core AMD Opteron™ x86 processor, with 2.8 GHz clock frequency). The generation of gating signals is performed using DS5101 digital waveform output boards (16 channels, time resolution of 25 ns). For measurement of electrical signals, a dSpace DS2004 analogue to digital conversion board (16 channels, 16 bit vertical resolution, conversion time of 800 ns per channel) is used. Mechanical speed and rotor position are measured using a dSPACE incremental encoder interface board DS3002 (6 channel, 32 bit position counter, supports up to 4096-fold subdivision between encoder lines).

Real-time control is organised as follows: one DS5101 channel sends an interrupt routine flag to all other channels on the same DS1006 board every 500 μs, which corresponds to the switching period. A corresponding interrupt routine applies the duration of time intervals in which gating signals should be on high and low voltage levels for each of the PWM channels. These are obtained in an additional Matlab function block, in terms of so-called *normalised time delay* signals. In order to enable easier implementation of different modulation strategies for the same drive configuration, a somewhat complex calculation algorithm is developed. Five different *normalised time delay* values are used per PWM channel, here referred to as $TD_{1..5}$, where TD_1, TD_3 and TD_5, correspond to high voltage level of gating signal (on state), while TD_2 and TD_4 determine low voltage level gating signal duration (off state) during one switching period. These are shown in Fig. A2.1. In order to produce the same switching pattern as in simulation, where phase voltage reference is compared with a triangular carrier signal, symmetry of switching times yields: $TD_1 = TD_5$ and $TD_2 = TD_4$. The phase voltage reference, sampled at the beginning of the switching period determines the overall on and off state in the corresponding drive phase, according to duty ratio calculations in Chapter 5. Finally, $TD_{1..5}$ are determined according to the desired carrier arrangement, which comes down to simple *if-then-else* statements, as shown in Fig. A2.1.

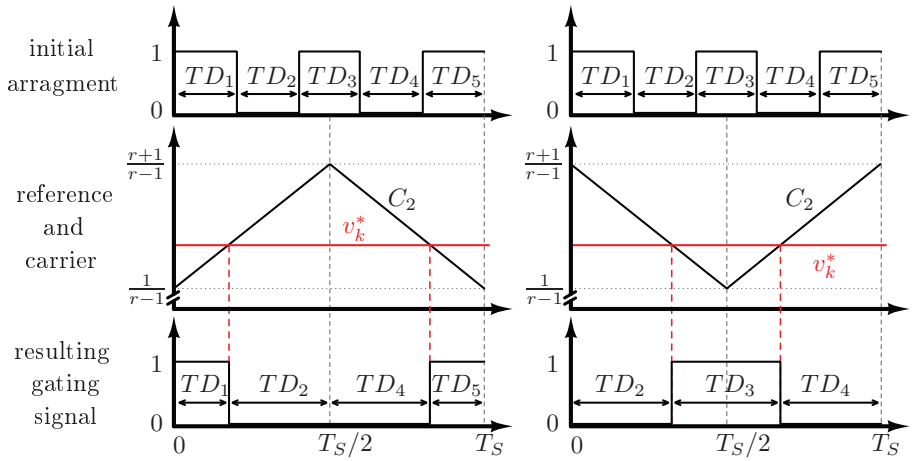


Fig. A2.1. Formation of DS5101 PWM outputs (gating signals) using n*ormalised time delay signals*. Equivalence between this method and reference comparison with carrier C_2 used in simulations is depicted for the case of 3L-OeW-2L configuration, for PD (a) and APOD (b) PWM. In the first case, $TD_3 = 0$, while APOD results in $TD_1 = TD_5 = 0$. In this case, *normalised time delay signals* are applied to VSI_2, due to the modulation strategy properties (Chapter 4).

For example, if a specific carrier orientation leads to a high voltage level of gating signal at the beginning and the end of the switching period, while a low voltage level of gating signal is expected in the middle, then $TD_3 = 0$, $TD_1 = d_{jk}/2$, $TD_2 = TD_4 = (1 - d_{jk}/2)$, for j^{th} inverter and k^{th} drive phase. For safety reasons, $TD_5 = 1 - (TD_1 + TD_2 + TD_3 + TD_4)$, which ensures that the overall duration of the switching period in each drive phase is equal to 500 μs, while in regular conditions it yields $TD_1 = TD_5$. Exact implementation of this PWM generation pattern includes modification of initial *PWM.src* and *rti5101dwo.c* files that describe the interface of DS5101 board with the rest of the dSPACE platform, i.e. its central processor board. The Matlab/Simulink function block that generates *normalised time delay signals* takes phase voltage reference as its input, as well as several constants:

- Normalised equivalent voltage levels ($l_{1..6}$);
- Modulation index values that determine borders for specific kind of modulation, i.e. borders between single-sided operation, multilevel operation, etc.
- For SRA implementation, this block includes calculations of phase current sign and application of corresponding reference offsets, as described in Chapter 3.

For the all 2L-OeW-2L drive configurations, a single DS5101 board is used, since only eight PWM channels are needed per inverter. A parallel interface from dSPACE provides gating signals for VSI_1 directly, on the lower eight channels. Since so-called *double* control mode is used, the VSI_1 input interface also processes the higher eight channels and transfers them to the VSI_2 PWM inputs, using the same interface. In the case of the 3L-OeW-2L drive, two DS5101 boards are necessary, since the three-level inverter (VSI_1) requires twelve gating signals for all of its six legs PWM control, while VSI_2 requires eight gating signals, since it has eight leg outputs. Hence, each inverter is controlled by a single DS5101 board, which are synchronised using one additional PWM channel per board. Synchronisation is realised externally in the following manner: the DS5101 board associated to VSI_1 sends an active high signal to the second DS5101 board (associated to VSI_2) channel that generates interrupt requests for other PWM channels on that board. Instead of measuring time independently, this channel on the second DS5101 board is configured as an input, waiting on the rising edge at the beginning of each switching period.

A2.3. POWER STAGE OF THE EXPERIMENTAL RIG

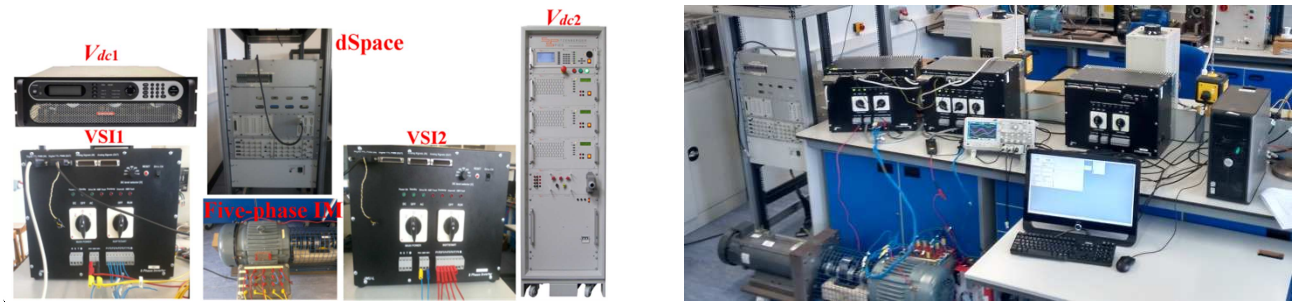
In all experiments, a custom-made five-phase induction machine is used, with the parameters given in Appendix 1. Two- and three-level inverters' key parameters are given in Table A2.1. Communication between inverters and dSPACE is realised with two parallel interfaces. The first one, inverter input signals, corresponds to PWM signals generated by DS5101. The second one provides electric signal measurements, obtained using inverter sensors (i.e. their output signals) to DS2004 board. The layouts of the two interfaces are available in the two- and three-level inverter manuals.

Table A2.1. Two-level (2L) and three-level (3L) inverters parameters.

Parameter	Name, value	Key facts
Number of phases	2L VSI: 8 3L VSI: 6	/ /
IGBT+D modules	2L VSI: Semikron FS50R12KE3	Two-level module, blocking voltage: 1200 V, nom. current: 50 A.
	3L VSI: Semikron KM50GB12T4	
Rectifier diodes	Both: Semikron SKKD46/12	Module with two diodes connected in series, blocking voltage: 1200 V, nominal current: 90 A.
Capacitors (dc-link)	Epcos B43456-A5158-M	Electrolytic capacitors, 1.5 mF, tolerance 20%, ESR_{typ} = 92 mΩ rated voltage 450 V.
	Itelcond ARX-HG	Electrolytic capacitors, 1.5 mF, tolerance 20%, ESR_{typ} = 80 mΩ rated voltage 400 V.
Sensors	LEM LV 25-P	Voltage transducer (10 V - 500 V), accuracy ±0.9%.
	Honeywell S&C CSNE 151-100	Current transducer (±50 A), accuracy ±0.5%.
Dead-time	$t_{d\text{-}t}$ = 6 μs	Analogue realisation
Gate drivers	Avago HCPL-316J	Gate drive optocoupler, integrated desaturation (VCE) detection and fault status feedback. Maximal current: 2.5 A.
Trips	Analogue protection and fault signalisation	Overvoltage, overcurrent, overtemperature and IGBT open circuit fault.

The inverter power supply, i.e. dc-link formation is realised in different manners, according to the specific experiment requirements. Each inverter has an incorporated three-phase diode rectifier, which enables usage of three-phase mains supply for dc-link formation, as shown in Figs. 5.1 and 5.13. This approach is implemented when stability of the dc-link voltage is guaranteed by modulation strategy characteristics. Isolation is provided by three-phase isolation transformers (rated for up to 400 V, 10 A at 50 Hz), while the exact dc-link voltage ratio is adjusted using three-phase variacs, installed between the transformer and the three-phase diode rectifier inputs. This kind of dc-link formation has several drawbacks, due to voltage drops on transformers and variacs (rated for up to 415 V and 20 A, per phase), which depend on the overall dc-link current. Detected 2-10% dc-link voltage drops during fast transients and under load conditions resulted in somewhat lower harmonic performance. For these reasons, a more sophisticated method for dc-link voltage formation is applied in the final experiments, based on isolated controllable dc sources Sorensen SGI-600-25, which is able to provide dc voltage output is up to 600 V and source up to 25 A. In cases where dc-link overcharging is expected a Spitzenberger & Spies four-quadrant linear power supply is used, based on three PAS-2500 amplifiers and a SyCore control system. Since PAS-2500 amplifiers are not mutually isolated, the four-quadrant supply can be used on one drive side only. The dc-link for the second inverter in those cases is realised using Sorensen dc sources. For the dynamic response tests, presented in Chapter 7, an additional braking hardware is used, based on controllable PWM braking and energy dissipation on external resistor bank, since the preliminary tests showed that integrated dynamic braking system of the inverters is not precise enough. For example, dynamic braking starts at 500 V if a desired dc-link

voltage is 400 V, which clearly affects the dc-link voltage ratio during braking, which has to be kept constant, due to applied modulation algorithms. Besides, it is based on analogue hysteresis control, which should result in somewhat lower dc-link voltage than desired, at the end of the braking process. This is a regular protection measure in systems where three-phase rectifiers are used for dc-link formation. However, controllable dc sources are preventing any voltage drop in dc-link voltage. This means that the braking process cannot end if integrated braking system of custom-built inverters is used, unless some of the trips are activated, caused by dc source overcurrent or braking resistor overheating. For these reasons, an external braking circuit is used, based on digital PWM control of dc-link voltage that employs an additional inverter leg with resistor bank connected to its output. As a result, only about 1% of the dc-link voltage increment is detected, during reversal tests, which does not have a significant impact on dc-link voltage ratio and modulation strategy performance, even under loaded conditions. The experimental set-ups for the OeW drive topologies considered in this thesis can be seen in Fig. A2.2.



a) b)

Fig. A2.2. Hardware structure for experimental verification of modulation strategies for 2L-OeW-2L drive with $r = 2$ (a) and for 3L-OeW-2L drive during testing (b).

A2.4. MEASUREMENTS AND DATA ACQUISITION

The measured waveforms are obtained using a Tektronix MSO2014 oscilloscope. The leg voltages of VSI_1 and VSI_2, associated with the first drive phase (v_{11} and v_{21}), and the corresponding phase voltage (v_1) are measured using Tektronix P5205A high voltage differential probes. Phase current (i_1) is measured using a Tektronix TCP0030 current probe. The same type of current probes is used for dc-link current measurements in Chapter 5, while the rotor speed is obtained from dSPACE, using DS2101 digital to analogue converter board. Results in Chapter 7, where transient performance of OeW drives operating under FOC is analysed, are recorded using the dSPACE system only.

In the case of oscilloscope measurements, data acquisition is performed in Open Choice Desktop (version 2.1) graphic user interface which supports TekVisa protocol (serial communication) between oscilloscope and personal computer. Obtained .csv files are later processed in Matlab, in order to calculate THDs and produce plots. THD calculation is performed using (3.14), without any window function, since deep-memory oscilloscope is used for data collection. Only samples from the first fundamental period are used for THD calculation. Every measurement is repeated at least three times. In order to minimise measurement error, the final results are obtained using mean values.

Appendix 3

DERIVATIONS OF EXPRESSIONS (5.13) AND (5.14)

The first step in this analysis is to determine the time instants in which the phase voltage reference intersects with equivalent voltage levels (i.e. goes from one reference zone to another, see Fig. 3.5c). Obviously, the phase voltage reference never intersects the lowest and the highest equivalent voltage level ($l_1 = 0$ and $l_4 = 1$, Fig. 4.3a). Therefore, it is sufficient to analyse under what conditions phase voltage reference belongs to the second reference zone. This can be written as:

$$l_2 < \frac{1}{2} + \frac{M}{2} \cdot \sin(\omega_m \cdot t - (k-1) \cdot 2 \cdot \pi / 5) < l_3 \tag{A3.1}$$

where l_2 and l_3 are two inner equivalent voltage levels in Fig. 3.5c. The expression (A3.1) can be written in more convenient form, with respect to t:

$$\frac{\arcsin(\frac{M}{2} \cdot (\frac{1}{r+1} - \frac{1}{2}))}{\omega_m} - (k-1) \cdot 2 \cdot \pi / 5 < t < \frac{\arcsin(\frac{M}{2} \cdot (\frac{r}{r+1} - \frac{1}{2}))}{\omega_m} - (k-1) \cdot 2 \cdot \pi / 5 \tag{A3.2}$$

Using (4.1), and trigonometric transformations (5.13) and $r = 2$ and $k = 1$ the above condition provides four time instants, in which v_k^* intersects with $l_2 = 1/3$ and $l_3 = 2/3$ ($f_n = 50$ Hz):

$$\tau_{11} = \frac{\arcsin(\frac{1}{3 \cdot M})}{100 \cdot \pi \cdot M}\text{s}, \quad \tau_{21} = \frac{T}{2} - \frac{\arcsin(\frac{1}{3 \cdot M})}{100 \cdot \pi \cdot M}\text{s}, \quad \tau_{31} = \frac{T}{2} + \frac{\arcsin(\frac{1}{3 \cdot M})}{100 \cdot \pi \cdot M}\text{s}, \quad \tau_{41} = T - \frac{\arcsin(\frac{1}{3 \cdot M})}{100 \cdot \pi \cdot M}\text{s} \tag{A3.3}$$

The final expressions for d_{1k} and d_{2k} are:

$$d_{1k} = \begin{cases} 3 \cdot v_k^*(t) & \text{if} \quad 0 < t \le \tau_{1k} \\ 1 & \text{if} \quad \tau_{1k} < t \le \tau_{2k} \\ 3 \cdot v_k^*(t) & \text{if} \quad \tau_{2k} < t \le \tau_{3k} \\ 0 & \text{if} \quad \tau_{3k} < t \le \tau_{4k} \\ 3 \cdot v_k^*(t) & \text{if} \quad \tau_{4k} < t \le T \end{cases} \tag{A3.4}$$

$$d_{2k} = \begin{cases} 3 \cdot v_k^*(t) & \text{if} \quad 0 < t \le \tau_{1k} \\ 3 \cdot (1 - (v_k^*(t) + 1/3)) & \text{if} \quad \tau_{1k} < t \le \tau_{2k} \\ 3 \cdot v_k^*(t) & \text{if} \quad \tau_{2k} < t \le \tau_{3k} \\ 3 \cdot (1 - (v_k^*(t) - 1/3)) & \text{if} \quad \tau_{3k} < t \le \tau_{4k} \\ 3 \cdot v_k^*(t) & \text{if} \quad \tau_{4k} < t \le T \end{cases} \tag{A3.5}$$

Note that (A3.4) and (A3.5) are dual with expressions in Table 5.2. The only difference is that Table 5.2 provides duty ratio expressions with regard to the vertical axis in Fig 3.5c (i.e. equivalent voltage levels), while (A3.4) and (A3.5) are considering the time domain (i.e. horizontal axis in Fig. 3.5c). Resulting duty ratios and $i_{dclink1k}$ and $i_{dclink2k}$ for several cases are shown in Fig. 5.7. The starting expressions for dc-link current mean values' calculations are:

$$\overline{i_{dclink1}} = \frac{5 \cdot I_m}{T} \cdot \left[\int_0^{\tau_{11}} (3 \cdot (\frac{1}{2} + \frac{M}{2} \cdot \sin(\omega_m \cdot t)) \cdot \sin(\omega_m \cdot t - \phi)) \cdot dt + \int_{\tau_{11}}^{\tau_2 1} (\sin(\omega_m \cdot t - \phi)) \cdot dt + \right.$$
$$\left. + \int_{\tau_{21}}^{\tau_{31}} (3 \cdot (\frac{1}{2} + \frac{M}{2} \cdot \sin(\omega_m \cdot t)) \cdot \sin(\omega_m \cdot t - \phi)) \cdot dt + \int_{\tau_4 1}^{T} (3 \cdot (\frac{1}{2} + \frac{M}{2} \cdot \sin(\omega_m \cdot t)) \cdot \sin(\omega_m \cdot t - \phi)) \cdot dt \right] \tag{A3.6}$$

$$\overline{i_{dclink\,2}} = -\frac{5\cdot I_m}{T}\cdot\left[\int_0^{\tau_{11}}(3\cdot(\frac{1}{2}+\frac{M}{2}\cdot\sin(\omega_m\cdot t))\cdot\sin(\omega_m\cdot t-\phi))\cdot dt+\right.$$
$$+\int_{\tau_{11}}^{\tau_{21}}(3\cdot(\frac{1}{6}+\frac{M}{2}\cdot\sin(\omega_m\cdot t))\cdot\sin(\omega_m\cdot t-\phi))\cdot dt+\int_{\tau_{21}}^{\tau_{31}}(3\cdot(\frac{1}{2}+\frac{M}{2}\cdot\sin(\omega_m\cdot t))\cdot\sin(\omega_m\cdot t-\phi))\cdot dt+ \quad \text{(A3.7)}$$
$$\left.+\int_{\tau_{31}}^{\tau_{41}}(3\cdot(\frac{5}{6}+\frac{M}{2}\cdot\sin(\omega_m\cdot t))\cdot\sin(\omega_m\cdot t-\phi))\cdot dt+\int_{\tau_{41}}^{T}(3\cdot(\frac{1}{2}+\frac{M}{2}\cdot\sin(\omega_m\cdot t))\cdot\sin(\omega_m\cdot t-\phi))\cdot dt\right]$$

The above expressions are obtained by summation of mean values (integral summands) that correspond to time intervals in which phase voltage reference belongs to one reference zone. This comes from the fact that duty ratios are calculated differently in each reference zone, according to the modulation strategy rules, i.e. equation (3.11) and Table 5.2. After integration in wxMaxima software and multiplication with number of phases, the expressions for $i_{dclink1}$ and $i_{dclink2}$ mean values are obtained:

$$\overline{i_{dclink\,1}} = \frac{5\cdot I_m}{8\cdot\pi}\cdot\left\{4\cdot\cos(\arcsin(\frac{1}{3\cdot M})-\phi)+4\cdot\cos(\arcsin(\frac{1}{3\cdot M})+\phi)+\right.$$
$$\left.+M\cdot\left[12\cdot\cos(\phi)\cdot\arcsin(\frac{1}{3\cdot M})-3\cdot\sin(2\cdot\arcsin(\frac{1}{3\cdot M})+\phi)-3\cdot\sin(2\cdot\arcsin(\frac{1}{3\cdot M})-\phi)\right]\right\} \quad \text{(A3.8)}$$

$$\overline{i_{dclink\,2}} = -\frac{5\cdot I_m}{4\cdot\pi}\cdot\left\{(4\cdot\cos(\arcsin(\frac{1}{3\cdot M})-\phi)+4\cdot\cos(\arcsin(\frac{1}{3\cdot M})+\phi)+\right.$$
$$\left.+M\cdot\left[12\cdot\cos(\phi)\cdot\arcsin(\frac{1}{3\cdot M})-3\cdot\sin(2\cdot\arcsin(\frac{1}{3\cdot M})+\phi)-3\cdot\sin(2\cdot\arcsin(\frac{1}{3\cdot M})-\phi)-3\cdot\pi\cdot\cos(\phi)\right]\right\} \quad \text{(A3.9)}$$

Those can be further simplified by using the trigonometric identities. The first two summands in (A3.8) can be considered as sum of cosines, i.e. $A\cdot\cos(x+y)+A\cdot\cos(x-y)$, where $x=\arcsin(1/(3\cdot M))$ and $y=\phi$. That sum can be transformed into a trigonometric product in the form $2\cdot A\cdot\cos(x)\cdot\cos(y)$. The same applies to the last two summands in square brackets in (A3.8). The final expression for $i_{dclink1}$ mean current value is:

$$\overline{i_{dclink\,1}} = \frac{5\cdot I_m}{4\cdot\pi}\cdot\left\{8\cdot\cos(\arcsin(\frac{1}{3\cdot M}))\cdot\cos(\phi)+M\cdot\left[6\cdot\cos(\phi)\cdot\arcsin(\frac{1}{3\cdot M})-3\cdot\sin(2\cdot\arcsin(\frac{1}{3\cdot M}))\cdot\sin(\phi)\right]\right\} \quad \text{(A3.10)}$$

When the same transformations are applied to (A3.9), the final expression for $i_{dclink2}$ mean current value becomes:

$$\overline{i_{dclink\,2}} = -\frac{5\cdot I_m}{4\cdot\pi}\cdot\left\{(4\cdot\cos(\arcsin(\frac{1}{3\cdot M}))\cdot\cos(\phi)\right.$$
$$\left.+M\cdot\left[6\cdot\cos(\phi)\cdot\arcsin(\frac{1}{3\cdot M})-3\cdot\cos(2\cdot\arcsin(\frac{1}{3\cdot M}))\cdot\sin(\phi)-\frac{1}{2}\cdot\pi\cdot\cos(\phi)\right]\right\} \quad \text{(A3.11)}$$

Equations (A3.10) and (A3.11) are used in Chapter 5 for further analysis as equations (5.13) and (5.14), respectively.

Appendix 4

PUBLICATIONS FROM THE THESIS

JOURNAL PAPERS

Darijevic, M., Jones, M. and Levi, E., (2016), An open-end winding four-level five-phase drive, *IEEE Trans. on Industrial Electronics*, vol. 63, no. 1, pp. 538 - 549.

CONFERENCE PAPERS

Darijevic, M., Bodo, N., Jones, M. and Levi, E., (2013a), Four-level five-phase open-end winding drive with unequal dc-link voltages, *in proc. European Conf. on Power Electronics and Applications EPE*, Lille, France, pp. 1 - 10.

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Darijevic, M. and Jones, M., (2014a), Closed-loop control for four-level five-phase open-end winding drive with unequal dc-link voltages, *Int.l Conf. on Modeling and Simulation of Electric Machines, Converters and Systems ELECTRIMACS*, Valencia, Spain, pp. 1 - 6.

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