Non-Destructive Evaluation of Solder Joint Reliability

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Ph.D. Thesis

April 2012

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A thesis submitted in partial fulfillment of the requirements of
Liverpool John Moores University for the degree of
Doctor of Philosophy

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April 2012

Abstract

A through life non-destructive evaluation technique is presented in which a key solder joint feature, nucleating at the bump to silicon interface and propagating across a laminar crack plane is captured and tracked using acoustic microscopy imaging (AMI). The feasibility of this concept was successfully demonstrated by employing the measurement technique in combination with Finite Element Analysis (FEA) to study the impact of component floor plan layout on the reliability of electronics systems subjected to thermal cycling.

A comprehensive review of current and emerging packaging and interconnect technologies has shown increasingly a move from conventional 2D to 3D packaging. These present new challenges for reliability and Non Destructive Evaluation (NDE) due to solder joints being hidden beneath the packaging, and not ordinarily visible or accessible for inspection.

Solutions are developed using non-destructive testing (NDT) techniques that have the potential to detect and locate defects in microelectronic devices. This thesis reports on X-ray and Acoustic Micro Imaging (AMI) which have complementary image discriminating features. Gap type defects are hard to find using X-ray alone due to low contrast and spot size resolution, whereas AMI having better axial resolution has allowed cracks and delamination at closely spaced interfaces to be investigated. The application of AMI to the study of through life solder joint behaviour has been achieved for the first time.

Finite Element Analysis and AMI performance were compared to measure solder joint reliability for several realistic test cases. AMI images were taken at regular intervals to monitor through-life behaviour. Image processing techniques were used to extract a diameter measurement for a laminar crack plane, within a solder joint damage region occurring at the bump to silicon interface. FEA solder joint reliability simulations for flip-chip and micro-BGA (mBGA) packages placed on FR4 PCB's were compared to the AMI measurement performance, with a reasonable level of correlation observed. Both techniques clearly showed significant reliability degradation of the critical solder joints located furthest from the neutral axis of the package, typically residing at the package corners. The technique also confirmed that circuit board thickness can affect interconnect reliability, as can floor plan. Improved correlation to the real world environment was achieved when simulation models considered the entire floor plan layout and constraints imposed on the circuit board assembly.

This thesis established a novel through life solder joint evaluation method crucial to the development of better physics of failure models and the advancement of model based prognostics in electronics systems.

Acknowledgements

I would like to acknowledge and thank the following people and companies for their generous support and help. Without them I would not have been able to complete this work.

Firstly I would like to thank my employers Delphi Electronics and Safety for providing the required financial and technical support to enable this research to be brought to fruition. I would particularly like thank Dr Marek Wojcik and Janusz Duralek for providing simulation support and a practical introduction to FEA, Pam Williamson for micro-sectioning of test samples and obtaining subsequent SEM images. Steve Graham for ensuring ECAD resource was available for test board design, and thanks also to David Parry for designing the layout of the test board and supervising its manufacture. Thanks also to Bob Schofield, for checking through my thesis and making recommendations for improvement. There are many people throughout Delphi who have contributed or supported in some way to the success of this work. Unfortunately I cannot list you all, but you know who you are and I sincerely thank you for giving freely your time for technical discussions or making available services at your disposal.

I would particularly like to thank Dr Scott Popelar for generously taking the time to discuss his original papers with me, providing encouraging advice and additional modelling information.

The seed of undertaking a PhD was planted in my mind by my good friend Dr Adrian Craven, the seed would never have taken root without the persuasive nature of Professor David Harvey, I thank you both for your enlightened views of my ability.

To my esteemed academic supervisors Professor David Harvey and Dr Guang-Ming Zhang, I sincerely thank you for your guidance, support and enthusiasm throughout my research, and in particular the final preparation of this thesis. I would also like to thank Ryan Yang for his assistance with AMI and X-ray imaging of test samples, sense of humour, and encouraging advice at critical times during my writing up. This thesis, and friendships developed would not have been possible without the many entertaining and inspirational discussions we have held in Dr Zhang's 'office'. I truly thank them for the inspiration, fun and sanity these discussions provided.

Also, I would like to thank my longstanding friends Steve Jeffries and John McColl for providing encouragement, humour and sense of perspective throughout this marathon project. We can now get back out on the mountains again! I also thank them for their thorough review of my written work.

Finally, undertaking and completing this work would not have been possible without the unconditional love and support from my wonderful wife, Angela. Her willingness to sacrifice so much, in order for me to complete this work is incalculable. As a sign of my love and gratitude I dedicate this work to Angela and my young son Samuel, for whom the adventure and wonders of the world are merely beginning. His daddy has now finished writing "his book" it's now time to play!

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1. **Ryan S.H. Yang, Derek R. Braden, Guang-Ming Zhang and David M. Harvey**, "Through lifetime monitoring of solder joints using Acoustic Micro Imaging": Soldering & Surface Mount Technology (SSMT), 24(1):30-37, 2012.

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12. **Derek R. Braden, Ryan S.H. Yang, Janusz Duralek, Guang-Ming Zhang and David M. Harvey**, Investigation into the impact of component floor plan layout on the overall reliability of electronics systems in harsh environments.

    3rd Electronics System Technology Conference (ESTC), 13th-16th September, Berlin, 2010.

13. **Ryan S.H. Yang, David M. Harvey, Guang-Ming Zhang, and Derek R. Braden,** Reliability of Solder Joints Assessed by Acoustic Imaging during Accelerated Cycling, 3rd Electronics System Technology Conference (ESTC), 13th-16th September, Berlin, 2010.

14. **Ryan S.H. Yang, David M. Harvey, Guang-Ming Zhang, and Derek R. Braden** Feature Extraction of Acoustic Images for Reliability Testing of Solder Joints, GERI Annual Research Symposium (GARS), Liverpool John Moores University, UK, June 2010.

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16. **Guang-Ming Zhang, Ryan S.H. Yang, Derek R. Braden, and David M.Harvey** Sparse representation Methods for Ultrasonic NDE Signal processing, 10th western Pacific Acoustics Conference, 21st-23rd September 2009, Beijing, China.

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Glossary of Terms

2D	Two dimensional
3D	Three dimensional
A_f	Acceleration Factor
Al	Aluminium
AMI	Acoustic Micro Imaging
β	Shape parameter term in Weibull distribution function
BD	Beam diameter
BGA	Ball Grid Array
BT	Bismaleimide-Triazine – A resin based laminate material used in the construction of the interposer within an area array packaged device.
CBA	Circuit Board Assembly
CD	Compact Disc
cdf	Cumulative distribution function
CGA	Column Grid Array
CIP	Chip In Polymer technology
C-SAM	C-mode Scanning Acoustic Microscopy
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DIP	Dual Inline Package
DNP	Distance from neutral point
DVD	Digital Versatile Disc
η	Scale parameter in Weibull distribution where the bulk of the distribution lies
ε	Strain
ε_0	Initial strain
$\dot{\varepsilon}_i$	Initial creep strain rate
$\dot{\varepsilon}_m$	Minimum creep strain rate
$\dot{\varepsilon}_f$	Material ductility coefficient
$\Delta\varepsilon_p$	Plastic strain range
$\Delta\varepsilon_e$	Elastic strain range
EUE	Electronic and Ultrasonic Engineering (Research Group at LJMU)
EDS	Energy Dispersive Spectroscopy
EEPROM	Electrically Erasable Programmable Read Only Memory
ESTC	Electronics Systems integration Technology Conference

ENIG	Electroless Nickel Immersion Gold
$F(t)$	Cumulative failure distribution function
FAMI	Frequency domain Acoustic Micro Imaging
fcBGA	Flip chip Ball Grid Array
FEA	Finite Element Analysis
FEM	Finite Element Modelling
FFT	Fast Fourier Transform
FiPoP	Fan-In PoP
FR-4	"FR" stands for Flame Retardant and "4" means woven glass reinforced epoxy resin. The most commonly used printed circuit board material.
FR-5	High temperature versions of FR-4 epoxy laminate with glass fibre reinforcement.
γ	Defines the location of the Weibull distribution in time
GERI	General Engineering Research Council
GBS	Grain Boundary Sliding
HASL	Hot Air Solder Levelling, involves coating the conductors with molten solder then blowing off the excess with a hot air knife
Hz	Hertz, the unit of cyclic frequency in cycles per second
IBM	International Business Machines
IC	Integrated Circuit
IET	Institute of Engineering and Technology, formally known as IEE
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
iNEMI	International Electronics Manufacturing Initiative
IMC	Intermetallic Compound
ITRS	International Technology Roadmap for Semiconductors
k	Boltzmann's constant - $1.3806503 \times 10^{-23}$ Joules per Kelvin
$^1/_\lambda$	Reliability – Average operation time per single failure
$\lambda(t)$	Instantaneous failure rate
LJMU	Liverpool John Moores University
m	Fatigue ductility exponent empirically derived and used in Coffin Manson acceleration equation.
Matlab™	Mathematical Computer Software Analysis Package from Mathworks
MC	Material Creep
MEMS	Micro-electromechanical Systems
Microns	Micrometres or 10^{-6} Metres
Microvias	Terminology describing through holes or circuit board layer interconnects of <150µm diameter.

MHz	One Million Hertz
mils	A US distance unit equal to 0.001 inch. One mil is exactly 25.4 microns, just as one inch is exactly 25.4 millimetres.
MPa	Mega Pascal
N_f	Number of stress cycle reversals or Cycles to fail in the field
N_t	Cycles to fail in the test environment or cycles to first failure
NDT	Non-Destructive Testing
NDE	Non Destructive Evaluation
P_r	Probability
Pb	Lead
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PGA	Pin Grid Array – Precursor to BGA and CSP
PiP	Package in Package
PoP	Package on Package
ppm	Parts Per Million
Pre-Preg	Epoxy impregnated glass fibre matting
psi	Pounds per square Inch
Q	Relative activation energy for creep
QFP	Quad Flat Pack
ρ	Density of material
RGI	Radial Gradient Index
R	Acoustic energy reflection coefficient
RAM	Random Access Memory
ROI	Region of Interest
RSS1	Reflow Solder Side 1
RSS2	Reflow Solder Side 2
σ	Stress or applied load stress
SAC	Lead free solder comprising tin(Sn), silver(Ag) and copper(Cu).
SAC305	Lead free solder comprising of 96.5% tin(Sn), 3% silver(Ag) and 0.5% copper(Cu).
SAM	Scanning Acoustic Microscopy
SCSP	Stacked Chip Scale Packages
SEM	Scanning Electron Microscope
SiP	System in Package
SLAM	Scanning Laser Acoustic Microscope
Sn	Tin

SoC	System-on-Chip
T	Temperature
T	Relative acoustic energy transmission.
t_f	Time to fail in field
T_g	Glass transition temperature of a material
t_r	Time to rupture or failure in the Monkman-Grant equation
t_t	Time to fail in test
ΔT_{Field}	Thermal range in field environment
ΔT_{Test}	Thermal range in test environment
TAMI	Time domain Acoustic Micro Imaging
TSOP	Thin small-outline package
TSV	Through Silicon Via – Interconnection technology
UBM	Under Bump Metallisation
V	Velocity of sound in metres per second
Via	Small plated through hole in a printed circuit board used solely to interconnect tracks on different layers of the circuit board.
W	Inelastic strain energy density in MPa or psi
W_{CR}	Creep strain energy dissipated per thermal cycle in mJ/mm^3. Note: $1mJ/mm^3 = 1MPa$. Can also be expressed in psi.
WLCSP	Wafer Level Chip Scale Packaging
Z	Acoustic Impedance

Chapter 1

Introduction

This research, supported by Delphi Electronics Group, Liverpool, investigates solder joint reliability of area array parts using Non Destructive Evaluation methods. The methods developed aim to enable through life condition monitoring of modern manufactured electronic systems. A further extension of the work is to examine the influence on reliability of component layout or placement on a printed circuit board.

Although this research has been focused on high reliability automotive applications, the knowledge gained can be used by many industry sectors using electronics in their products or which have complex interdependent material structures e.g. composite materials.

1.1 Background to Project

Electronics is used extensively across many different market sectors to-day to deliver advanced technology features and functionality expected by consumers.

For many high volume markets such as automotive, the increased level of functionality must be delivered at the lowest possible cost and work in extremely harsh environments whilst achieving the highest levels of reliability. In such automotive applications reliability expectations of 98.5% is not unusual.

The use of electronics in modern vehicles is extensive and continues to increase. In 2002, it was estimated that some 25% of a vehicle's manufacturing cost was due to electronic systems (Braden, 2000). By 2010 Donovan (Donovan, 2007) predicted this to increase to account for some 40% of a vehicle's overall cost base. To-day, electric and hybrid motor vehicles push this figure substantially higher.

As the electronic content in a motor vehicle continues to increase, so also does the complexity of the vehicle embedded systems. Likewise, the reliability expectation of both the customer and vehicle manufacturer has also increased. In the first twelve months of a vehicle's life electrical problems account for up to 70% of customer complaints and warranty problems (MIRA (Motor Industry Research Association)). This is a generalised figure that includes all electrical and electronic equipment. No figures were presented for the proportion of failures within the quoted percentage that were attributed to either Ball Grid Array (BGA) or Chip Scale Packaged (CSP) devices. To put this in context, within Delphi Corporation as a whole it is estimated that the daily production of solder joints is approximately 1 billion. This represents some 1 billion or more failure site opportunities at the component to circuit board assembly interface.

Ever growing consumer expectations are driving manufacturers of electronic products to increased levels of functionality and miniaturisation in their products. This in turn has

accelerated the use of densely packaged electronic components in new designs (Braden, 2000). Consequently increased use is being made of Area Array packaged devices such as Ball Grid Array and Chip Scale Packaged components.

Such packaging technologies offer input/output connection pitches in the range 1.50mm to 0.5mm (BGA) and 1.0mm to 0.5mm (CSP). The benefit of using such technologies is not just seen in terms of bottom line product cost and circuit board real estate savings; it can impact on both product yield and quality. It also has the advantage that it may be processed using existing surface mount manufacturing techniques (Di Giacomo, 1997) (Fielstad, et al., 2003) (Viswanadham, et al., 1998).

Inside the semiconductor industry, Moore's law is driving significant changes in packaging technologies of electronic devices. Increasing transistor count relates directly to an increase in the number of interconnections emerging from the package (Perkins, 2007). As a result, packaging-interconnect density has experienced a six fold increase over the last five years. Subsequently designing 2D or 3D area array packaging is the future trend of electronics, leading to the development of further variations of BGA and CSP packaging; System-on-Chip (SoC), System in Package (SiP), Package on Package (PoP), Stacked Chip Scale Packages (SCSP) (Tyndall National Institute, 2006) and Chip In Polymer technology (CIP) (Ostmann, et al.).

Given that many complex silicon designs are realised using SoC or PoP, a point has now been reached where the decision to integrate on silicon is no longer an easy one (Edwards, 2010).

In order to readily adapt to market trends and cost, it is considered beneficial to use multiple chips in the realisation of a design by deploying scalable 2D or 3D area array packaging concepts as illustrated in Figure 1-1.

Figure 1-1: Example of Package-on-Package (PoP) (Statschippac)

Moreover, this is driving development of increasingly detailed non-destructive failure analysis tools in order to understand the reliability of micro and nanometric components subjected to

environmental testing (Krastev, 2007) (Dias, et al., 2005). This is particularly true of the automotive, avionics and defence industries due to reliability concerns. Automotive electronics systems operate in harsh environments, particularly those located under the bonnet or on the engine, where thermal cycling, vibration and high levels of moisture are present.

The package to printed circuit board (PCB) solder joint interconnections are extremely important since it represents, in many cases, the weakest link in terms of product reliability. Solder joints however do not solely perform the job of providing an electrical connection; they mechanically affix the component to the PCB, provide thermal conduits for heat dissipation into the circuit board and help match expansion differences between printed circuit boards and components.

The continued 'up integration' of electronics functions into single silicon building blocks offers significant advantages in automotive applications, allowing complex products to be produced at low cost whilst achieving high levels of reliability. Unlike the 'white goods' market, which performs primarily regulatory and compliance testing, automotive applications additionally require extensive reliability life tests to be performed, thus assuring design reliability, safety and robustness. This subsequent testing and product validation adds considerable cost to the finished product. The design of these tests is based on a 'physics of failure' approach in which the application of thermal or mechanical energy is used to initiate a defect and then propagate the defect until a failure occurs in the product or an individual component.

For electronics applications solder joint failures are the most commonly experienced and of these the majority can be can be attributed to three main factors:

1) **Fracture** - Tensile rupture/fracture through mechanical overloading.

   In this type of failure, the shear strength of the solder has been exceeded either as a result of design, for example fixing a warped PCB into an enclosure, or as a result of an accident or abuse such as dropping a product or knocking a component during the manufacturing process.

2) **Creep** - Long lasting permanent loading

   The solder joint or joints are subjected to continuous stress loading which results in degradation of the joint over time. Although such failures are more prominent through exposure to high temperature, solder joint cracks can occur at room temperature. Stress figures are of the order of $<1N/mm^2$ at 20°C and preferably $\leq 0.1N/mm^2$.

3) **Low Cyclic Fatigue** – Cyclic loading

   Cyclic fatigue induced failures are the result of the deformation of solder joints or component materials. This in turn may be due to a combination of coefficient of thermal expansion (CTE) mismatch differences in materials and cycling between temperature extremes. Deformation in solder joints is typically larger than with other material systems used in the manufacture of

electronics products. Solder joint cracking forms in all solder joints that are subjected to low cycle fatigue stress over long periods of time.

For large BGA, CSP or SiP packaged components, thermal cycling in conjunction with self-heating introduces thermal gradients across the component. Thermal gradients interacting with the CTE of various materials used in the fabrication of a component produces stress and strain. Accumulated stress and strain over time giving rise to fatigue failures.

Many physics of failure models exist that describe how the operating environment induces a given failure mode within the electronic devices and their packaging. Such models are not only used to predict operating performance and theoretical life expectancy but they are also used by reliability engineers to determine test durations and sample sizes. This is particularly important in the automotive industry. Products typically have an expected life of 600,000km or 15 years in the case of light duty applications such as cars and vans.

The models in many cases are verified through laboratory testing of Circuit Board Assemblies (CBA) which are not fully representative of the characteristics and dynamics of the actual boards used in production.

In order to detect solder joint degradation or joint failure over a period of time, samples are either removed from the test at various points during the test cycle for micro-sectioning or are monitored for signs of deterioration throughout the test using electrical resistance measurement. Destruction of the test sample is inherent with micro-sectioning. Thus samples removed from an environmental test and subsequently micro-sectioned cannot be returned for further exposure. There are further unwanted issues with this technique. Firstly, it is assumed that all generated defects behave consistently and occur across the entire sample batch in the same manner. Secondly, by destroying the sample, the technique does not allow for a detailed investigation of solder crack initiation or how the environmental exposure affects crack propagation. Finally, any defects of interest and solder joint cracks irrespective of size can easily be missed due to the 2D nature of micro-sectioning and is very reliant on selecting the correct sectioning plane.

Such detailed failure site information is core to understanding component/product reliability. Clearly it is difficult in a non-destructive manner to visually inspect hidden solder joints on area array type packages. As device features and packaging get ever smaller, traditional non-destructive failure analysis tools such as X-ray and Acoustic Microscopy are becoming increasingly less effective. Furthermore, 3D structures that include stacked die packages and SiP, with associated heat sinks and thermal dissipation solutions present further challenges for non-destructive evaluation techniques.

1.3 Motivation and Contribution to Knowledge

Several non-destructive testing (NDT) techniques have been proposed to investigate, detect and locate defects in microelectronic devices, their associated packaging and their interconnection to a substrate, which for this research is an organic printed circuit board (PCB). These include optical inspection using microscopes, X-ray microscopy (Moore, et al., 2002), acoustic micro imaging (AMI)/scanning acoustic microscopy (SAM) (Pahl, et al., 2004), electronic speckle pattern interferometry (Lee, et al., 2004), scanning electron microscopy (SEM) and laser ultrasound coupled to interferometry (Liu, et al., 2004). No single method has been able to satisfy present NDT requirements, so this work is motivated at advancing techniques to measure and extend product reliability knowledge for current and future products. The work presented in this thesis follows a multidisciplinary approach to gain better understanding of the interconnect behaviour of area array packaged devices populated on organic substrates.

Comparison is made between Finite Element Analysis and AMI techniques as applied to the measurement of the reliability performance of solder joints for the test cases studied. Test cases were carefully designed to investigate the influence on joint reliability of floor plan layout and substrate thickness. AMI has not previously been used to perform through life monitoring and study the effects of thermal cycling on crack growth through a solder joint. In the proposed method AMI images taken at regular intervals throughout the environmental exposure are post processed to measure the diameter of a 2D plane (termed crack plane) within a damage region of the solder joint occurring at the bump to silicon interface. Subsequently testing the hypothesis that crack plane diameter is related to fatigue cycle exposure and joint degradation can be monitored for the first time, using AMI to assess lifetime performance.

The crack plane diameter values for each bump, recorded at regular intervals throughout the testing were used to generate a 3D graphical representation of the reliability of the package interconnections. Interconnection reliability graphs obtained from measurement and simulation results were subsequently used to study the influence of floor plan layout and substrate thickness on joint reliability. Component layout influence on solder joint reliability has been studied by Ye (Ye, et al., 2007) and Primavera (Primavera, et al., 2004) for BGA packaged components. In their work no through life monitoring was deployed and destructive testing techniques were used to evaluate joint degradation only at the end of the environmental test exposure. This subsequently gave limited information regarding healthy and failed joints, with no intermediate data available for monitoring through life performance.

As joint geometries and packaging dimensions reduce it is suggested that the influence of floor plan layout, PCB constraint points and substrate thickness will significantly influence solder joint reliability (Braden, et al., 2010). The new metrology method proposed in this work will be crucial to the study of this emerging area of interest and may ultimately lead to better physics of failure models and prognostics in electronics systems.

1.4 Thesis Outline

The thesis is divided into six chapters and five appendices.

Chapter 1 outlines the background to the research, identifying the key problems encountered along with motivation and contribution to knowledge and a thesis overview.

Chapter 2 presents a detailed review of area array packaging technology to develop an understanding of the packaging roadmap and the need to develop new improved metrology to inspect hidden joints. The chapter also develops understanding of package interconnection techniques, structures, materials deployed in their fabrication and the likely interconnect reliability problems which will be encountered. This underpinning information is required in order to assess the difficulties of deploying Non Destructive Evaluation methods to the inspection of solder joints, and as an aid to the specifications required to develop and run Finite Element Analysis (FEA) simulations.

Chapter 3 studies the application of AMI and X-ray NDT techniques to the through life assessment of solder joints. The two contrasting methods are compared for their ability to resolve component features. Reliability and experimental testing setups are compared, including a discussion of common acceleration factors and how they are derived. Advanced signal processing and novel acoustic time-frequency domain imaging techniques were developed to improve the resolution of conventional AMI.

Chapter 4 designs the modelling methodology used in the evaluation of flip chip solder joint reliability performance. Specific modelling scenarios were developed that would investigate the influence of substrate thickness and component floor plan layout on joint reliability.

Chapter 5 develops an innovative through life measurement method for post processing the AMI image in order to non-destructively obtain the bump crack plane diameter and hence produce a thermal cycle's exposure estimate.

Chapter 6 Presents the conclusions from the work and suggestions for future studies are identified.

Chapter 2

Area Array Packaging Technologies

2.1 Introduction

It is projected that worldwide, advanced electronic packaging will account for revenue streams exceeding $42 billion by the end of 2012. The fastest growth being experienced in Chip Scale Packaging with the United Kingdom being poised to emerge as the second largest European market by 2012, with revenues projected to exceed $1.52 billion (Sadanaga, 2009).

In order to be world class in the field of microelectronics and packaging requires a detailed understanding of the reliability of emerging packaging technologies and the development of metrology and forensic inspection techniques in order to examine the interconnection and packaging performance.

2.2 A Brief Review of Packaging

The term packaging describes the process of mounting, interconnecting and encapsulation of microelectronic parts which increasingly includes combinations of passive parts in a compact and efficient manner.

It is this ability to package complex electronic functionality into a compact footprint which enables many modern day size constrained products to be realised and which provides increased available circuit board real estate.

Often packaging is considered as the low technology part of the semiconductor device manufacturing process. However, within packaging lies a multitude of materials technology and engineering problems (Grovenor, 1989) which can limit the overall performance of the device in its application. Electronics packaging provides four main functions:-

1. Provision of electrical interconnection between semiconductor die and/or passive components within the packaging and the outside world.
2. Provides thermal management for the silicon through power distribution and heat dissipation from the active regions of the silicon.
3. Provides protection of the silicon and their interconnections from harsh chemical and moisture laden environments.
4. Provides mechanical protection of the silicon and interconnections as well as providing a way of physically being able to handle the device during automated manufacturing processes.

Modern area array packaging such as Ball Grid Array (BGA) (introduced primarily by Motorola in the late 1980's) and Chip Scale Packaging (CSP) offers high packing density, better heat

dissipation and higher I/O count at lower cost and better reliability. BGAs have small conductive solder balls or columns that are soldered directly onto the surface of printed circuit boards as illustrated in Figure 2-1.

Figure 2-1: Cross section of Plastic Ball Grid Array (PBGA) (ETAC data sheet)

Unsurprisingly this makes it difficult to inspect the connections between the package and the PCB because the solder balls are located underneath the package. Consequently, special microscopes and micro-focus X-ray systems have been developed for joint inspection but are expensive and not useful as a 100% inspection tool. Therefore ensuring quality of the assembly process for products using BGA technology must be precise, having the minimum of tolerance errors (Denning, 2001).

Area array packaging covers a wide variety of packaging styles, types and configurations, however in all cases the principle interconnection techniques between the device package and the printed circuit board remain the same; each variation addressing a particular technology or packaging need.

The basic construction of an area array device is illustrated in Figure 2-1. The base material of the package is formed from substrates such as alumina (ceramic material), glass reinforced epoxy based laminate such as FR-4 or FR-5 or polyimide flex-film. The substrate which provides a mounting structure for die attachment also functions as a compliant interposer between the silicon die in the package and the printed circuit board onto which the package is soldered.

The electrical connection between the interposer and silicon is made either through wire bonding or reflow of high temperature solder balls attached to 'flip chips'. To protect the interconnections and silicon from the harsh environments to which it will be exposed the entire configuration is encapsulated or over-moulded with plastic.

2.3 Next Generation Packaging

The continual trend to increase functionality and pursuit of extreme miniaturisation within a single integrated circuit package, combined with dramatic increases in interconnection density is driving the development of next generation packaging.

Wafer level Chip Scale Packaging (WLCSP) and System-in-Package (SiP) are emerging as the future packaging technologies for semiconductor system architectures. Both pose significant reliability and metrology challenges as fabrication dimensions continue to shrink and unlikely combinations of 3D die and package stacking are deployed.

By definition, wafer scale packaging involves undertaking all packaging operations prior to sawing the wafer into individual die. This overcomes the increasing gap between silicon and PCB interconnection geometries, and the rising cost of packaging which is directly linked to the cost of I/O interconnections (Yannou, 2008).

WLCSP or flip-chip Ball Grid Array (fcBGA) as it is sometimes referred to offer extremely small outline geometries by stacking the die vertically within the same package footprint. Stacking the die in this way also contributes to an overall reduction in system cost. Electrical connection inter-die, and die and substrate are usually made using wire bonds, although solder balls or combinations of the two may be used when flip chips are deployed.

There are three common die stack versions of wire bonded packages, firstly, pyramid stacked die where smaller die are placed on top of larger die Figure 2-2, secondly, same size die with a silicon spacer placed between the two die Figure 2-3, and thirdly, die with overhang where rectangular die are placed at 90 degrees on top of each other Figure 2-4. In this example, two dies are thinned using a grinding process to 203µm - 254µm, to achieve when stacked an overall maximum package height between 1.4mm and 1.2mm respectively.

Although the following figures only show two stacked packages, in reality there are many variations of multiple stacked die packaging methods with three and more stacked chips available. Within the foreseeable future, it is expected to be practical to stack up to eight die, each 50 µm thick, in a 1 mm thick package (Dias, et al., 2005).

Figure 2-2: Pyramid stack configuration (i2a Technologies website)

Figure 2-4: Overhang cross stack configuration (i2a Technologies website)

System-in-Package technology is a variation on WLCSP which allows more functionality to be realised in a single package outline than is achievable using the conventional two or three die stacked packaging described earlier. System in Package is defined as being any combination of more than one active electronic component of different functionality, plus optionally passives and other devices like MEMS or optical components assembled into a single standard package that provides multiple functions associated with a system or sub-system (ITRS, 2009).

The technology enables complex functionality to be built using bespoke silicon building blocks from different suppliers, which are then integrated on the same substrate, thereby reducing both time to market and overall systems cost. Demand is expected by many leading semiconductor and packaging companies to increase by an average rate of 12% per year from the 3.25 billion assembled SiP units in 2008, resulting in SiP becoming the packaging technology of choice for realising highly complex functionality in an extremely small package size (INEMI, 2007).

SiP like many of the technologies reviewed so far have numerous construction and interconnection variations either in use to-day or under development. The most common variations are Package on Package (PoP) where multiple die or area array packaged components are stacked vertically on top of one another with interconnections being made using wire bonding, solder bonds or both, as illustrated in Figure 2-5 below. The completed

assemblies are not normally over moulded and use a variety of interposer technologies and materials in their construction.

Figure 2-5: PoP packaging variations (INEMI, 2007)

Although similar in nature to PoP, Package in Package (PiP) technology physically integrates silicon into one another, with connections being made via wire bonds.
The completed system is then over moulded. Since silicon packages are integrated directly there is a significant reduction in the form factor of the completed PiP device compared to PoP packaging, particularly with regard to packaging height as illustrated in Figure 2-6.

Figure 2-6: PiP packaging variations (INEMI, 2007)

A further development of PoP and PiP architectures combines the advantages of both, resulting in the creation of a fan-in PoP (FiPoP) structure as shown in Figure 2-7 (developed by STATSChipPAC Ltd.).

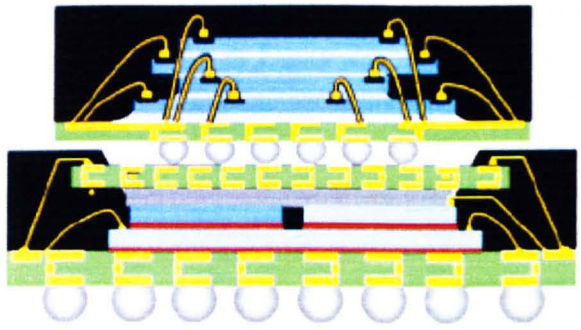


Figure 2-7: Example of a Fan-In Chip PoP (FiPoP)

This stackable 3D packaging solution comprises two halves in the overall design. The bottom half of the package allows single or multiple stacked flip chips to be interconnected, either using wirebond or reflow solder balls. The numbers of die which can be stacked is limited by the height of the epoxy over mould for the bottom half of the overall package. Additionally, the bottom half of the package provides connection pads to allow for another package or component to be reflowed on top as illustrated in Figure 2-7. The figure also shows that the top half of the package can contain single or multiple interconnected flip chip devices. The FiPoP package addresses the future growing demands of miniaturisation, interconnect density within a small package form factor, and increased integration through stacked flip chips.

The FiPoP design has the added advantage that since the mould encapsulant or top surface of the package extends to the package edge, a package style results which is less prone to warpage than conventional PoP solutions (Stuber, 2008).

Figure 2-8: TSV usage and via critical dimensions (CD) (Lassig, 2007)

From the discussions so far it is clear that as device geometries reduce toward the nanometre range, interconnection between the silicon using peripheral wire bonds becomes less-viable as a connection method as highlighted by Lassig (Lassig, 2007) in Figure 2-8. INEMI predicted that

from 2010 onwards, SiP packaged components would increasingly use Through Silicon Vias (TSV) connection technology as shown in Figure 2-9 (INEMI, 2007). TSVs differ from the microvias currently used in multilayer interconnects primarily in their size (1-100μm diameter and 10-400μm depth) and their need to penetrate not only the various materials that compose the overlying circuitry but also the significant depth of the silicon substrate (Lassig, 2007).

Figure 2-9: Typical SiP packaging technology in 2010 (INEMI, 2007).

The continual drive by the semiconductor industry to aggressively move beyond Moore's law is also driving significant developments in 3D SiP packaging technology, by embedding silicon functionality within the layers of the organic circuit boards. This has many advantages not only in shortened interconnect length but also in a significant reduction in package/device height and cost. Although such complex circuit structures may on the surface appear futuristic; it is possible to create the packaging structures that are shown in Figure 2-10 since fabrication uses many of the existing established PCB manufacturing processes and materials.

Note: The thickness of the double sided FR-4 printed circuit board core is 500μm.

Figure 2-10: Four silicon die stacked in polymer PCB (INEMI, 2007)

2.4 Levels of Interconnection Technology for Area Array Devices

Irrespective of overall device construction, electrical interconnection must be made between the active silicon and dielectric substrate (interposer), and the substrate and printed circuit board (PCB). The semiconductor packaging industry describes the hierarchical interconnect structure by levels as illustrated in Figure 2-11. The work described in this thesis, although concentrated on silicon to organic substrate interconnects, applies to all levels in which solder ball structures are deployed and in which acoustic inspection can be undertaken.

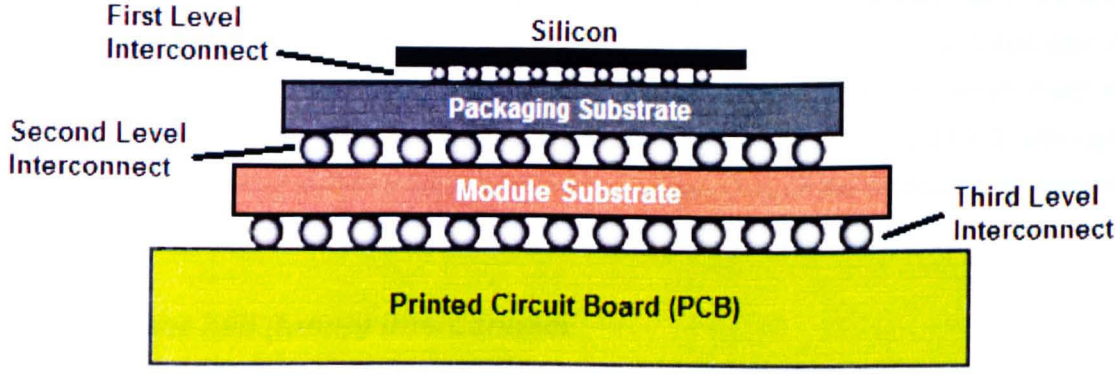


Figure 2-11: Hierarchical interconnect level structure

First level electrical routing from the silicon is undertaken using either wire bond or flip-chip technology. The die being either "face-up" in the case of wire bonding or "face-down or flip chip" as illustrated in Figure 2-12 in order to make the attachment. As discussed previously, multiple die may be stacked in a single package; interconnections being achieved using either wire bonding, reflow of solder balls on the flip chip or a combination of both.

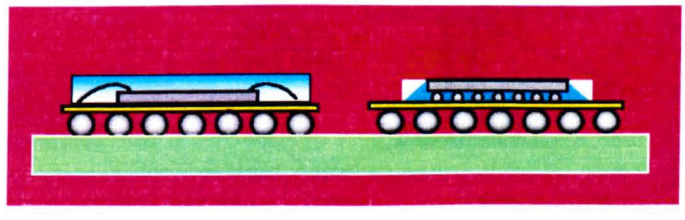


Figure 2-12: Die face up (left) or face down (right)

For wire bonding, the bond pad site must be uppermost; the back of the silicon die being bonded to the interposer using an epoxy resin. In the case of flip chip, due to the wide coefficient of thermal expansion differences between the silicon die and the PCB interposer the composition of interconnect materials and lead design are selected to provide thermo-mechanical compliance. The solder spheres are placed by first coating the land pads on the interposer with flux, which retains the solder spheres after placement; the flux paste also acts as

a stimulant for the solder to wet to the landing pad. Once placed, spheres and interposer are subjected to an optimized reflow profile which bonds the solder ball to the landing pad. Cleaning processes post reflow wash away remaining flux residues. Epoxy adhesive underfill is applied to provide both thermal management and improved reliability performance of the solder joints.
Figure 2-12 also shows that direct chip-attachment to the interposer with the die "face down" can maintain a smaller package outlines than with the die "face up".
Second level interconnection at the package to PCB interface comprises of either a solder ball or column. Attachment of the solder balls (or bumps) onto the interposer pad areas being performed mechanically after package encapsulation. Differences exist between level one and level two solder joint interconnects, primarily interconnect material composition and diameter of the solder balls. Solder alloys being typically either a near eutectic SnPb alloy which melts at 183°C or a lead-free alloy such as SAC305 which melts between 217°C and 219°C, although different compositions of lead free are available for use depending on the properties required by an application.

2.4.1 Solder ball (bump) interconnect

The majority of area array soldered interconnects are realised using solder balls; however there are applications where double stacked solder balls or columns are used instead as illustrated in Figure 2-13. The columns (usually copper) provide additional height which could not be achieved using an increased solder ball size.

Figure 2-13: Pictorial of solder ball and solder column interconnections (Fillion, 2006).

In both cases, the increased height provides additional compliance when the joint is under thermally induced cyclic stress conditions, which in turn increases joint reliability. However, the increased height has a detrimental effect on reliability in high vibration applications.
Whether discussing ball or column interconnects the bumping processes are very similar. The first stage in the process is providing a metallic base layer over the conductive bond pads of the silicon, known as Under Bump Metallisation (UBM). This is extremely important since many of

the bumping processes are not compatible with the very thinly deposited (via sputtering or vacuum deposition) aluminium or copper metallisation used in the wafer fabrication process.
Although the UBM base material may be thought of as aluminium or copper, there is in fact no standard UBM metallisation formula; many semiconductor manufacturers developing their own proprietary material sets. Currently the most commonly seen UBM is electroless nickel, although copper is increasingly being deployed since it is more compatible with the bump materials used and has higher electrical conductivity than aluminium or nickel finish.
The next stage in the process is application of the solder bumps; this can be done pre or post UBM processing.
There are five primary ways in which to form the solder bumps:-

Evaporated bumping - The process was originally developed by IBM over 40 years ago and in some applications is still used to-day, primarily in the deposition of high quality lead content solder bumps since it is not suitable for lead free or large diameter wafers. This is due to the low vapour pressure of tin making it evaporate slower, giving rise to high deposition times and therefore increased manufacturing cost.

Electroplating - This is the preferred method for producing high quality fine pitch solder bumps. However it is not suitable for lead free applications due to the process difficulties (also high processing cost) in forming bumps containing tin and silver in the material set.

Stencil printing – Balls are formed by screen printing solder paste onto the UBM bond pad area of the silicon; the deposited paste is reflowed using infrared heating, the molten material solidifying to form a solder ball as shown in Figure 2-14. Stencil printing cannot be used for bump pitches <200µm. The limiting factor being that the paste area must be bigger than the required bump in order to overcome the shrinkage resulting from the reflow process. The molten spheres must be well separated during reflow to avoid 'solder bridging'. Moreover, the printing process can introduce bump height variation and produce voids within the spheres. One advantage of this process is that it can be used for producing bumps in both lead and lead free material sets.

Figure 2-14: Reflowed printed bumps onto UBM (Courtesy of Pac Tech)

Solder Sphere Attachment – This process is very similar to the stencil printing approach in that the pre-formed solder sphere/balls are mechanically placed onto the UBM and reflowed. The spheres can either be singly or batch placed, however it does restrict the minimum size of sphere which can be placed to 100µm. In the case of singly placed spheres, the reflow process may be performed using a single laser pulse (termed jetting). The laser jetting technique can be used to place bumps on top of one another in order to increase bump height. Both lead and lead free bumps may be formed using this process.

Injection Mould – This process is particularly suited to producing fine pitch, high quality bumps onto wafers using any desired material set. The bumps are formed independently from placement process, by filling a cavity mould which matches that of the wafer bond pads with molten material. In the second part of the process, the formed bumps contained in the mould are attached to the wafer by heating both wafer and mould to 20°C above the solder material reflow temperature, the expansion of the molten solder is such that it makes contact with the wafer UBM and is transferred from the mould, which is in close proximity to the wafer. The process does not require the use of flux and is able to produce solder bumps of 25 µm diameter on a 50µm pitch. On cooling the resulting bump is hemispherical in appearance with a slightly flat top.

The reliability of the first level solder bump interconnect is influenced significantly by the uniformity of the solder ball, with electrical open circuits occurring in undersized balls and short circuits in oversized. Equally, ball or column height can affect the reliability performance of the package both at the level 1 and level 2 interconnect. Increased height allowing better thermal compliance, but poorer mechanical vibration performance; the opposite being true for low bump height. The application of underfill to the silicon is used to increase the ability of the device to survive both thermal and vibration induced cyclic forces. However, as ball sizes reduce, the

height between the silicon and interposer are reduced to such a point that limits the flow of underfill e.g. 100µm pitch, gives approximately 25 µm of height. (Frear, 1999)
Currently the first level interconnection in high reliability applications can only be met using leaded solder bumps. Although tin rich lead free solder materials can in some cases offer comparable joint compliance to their leaded counterparts, in many cases they are they are less mechanically compliant. Increased thermal expansion mismatch is experienced between silicon die and organic packaging during either reflow due to the required higher reflow melting point (~30°C higher than leaded (SnPb)) or during cyclic thermal events in service. Subsequently solder joints experience higher levels of stress and have a lower overall mechanical strength.

2.4.2 *Through silicon vias (TSV)*

As the interconnect density of stacked silicon increases and geometries of active silicon reduce to 28nm and beyond, interconnection between stacked silicon becomes more difficult in SiP devices. The use of traditional organic glass fibre interposers between the silicon and package bumps becomes impractical. Although it is possible to laser machine microvias of <25µm, the limits of current UV laser technology are being reached. Equally, where active silicon is stacked it is highly desirable to have direct interconnection between the layers of silicon to reduce parasitics, the CTE mismatch between devices and provide better thermal management.
TSV's overcome both the issues identified, allowing the silicon itself to act either as a combined active circuit plus interposer or act as an interposer on its own.

Figure 2-15: Micro-section of TSV interposer (Institute of Microelectronics (IME), Singapore).

The TSV's are formed by dry or wet etching of a cavity, of the desired depth into the silicon; the resulting cavity is then dry or wet filled with copper as illustrated in Figure 2-15 to create a

conductive path. The interconnection between TSV's in this example being achieved through reflow solder bumps, although it is possible to connect directly with the silicon using TSV's alone.

2.5 Packaging Substrate Technology

Packaging Interconnection substrates (or Interposer) play a pivotal role in the performance and construction of area array devices. In addition to providing fan out to the level two interconnect points; the substrate must be capable of providing thermal management, signal matching and mechanical support to the attached silicon die which provides the electronic functionality.

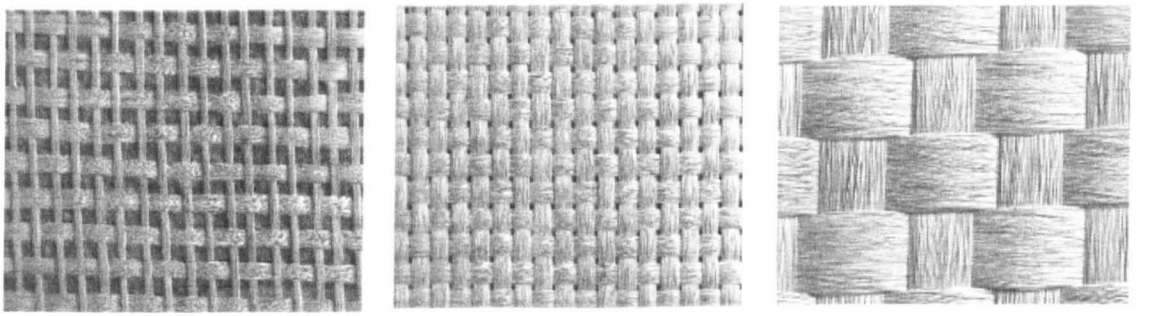
Although early packaging used tape substrates made from high-strength, high-temperature polymer materials such as polyimide which allowed significant mechanical compliance and ease of fine line circuit feature and micro via fabrication, they did suffer problems of warpage and large values of CTE mismatch with other materials used in the packaging process.

The majority of package substrates today, particularly complex 3D packaging makes use of rigid or laminate substrates.

There are a wide range of rigid substrate material options, each having specific areas of application. Currently for 90% of packaging applications, organic resin based printed circuits are used, with ceramic substrates being used in the remaining 10% in order to overcome complex thermal management issues associated with high power electronic devices, where moisture absorption is likely to be a problem or for Coefficient of Thermal Expansion (CTE) issues.

In extremely dense packaging applications such as SiP and PoP, silicon is also being used combined with through silicon via (TSV) technology.

The manufacturing process is similar to existing multilayer circuit board technology, where the wiring layers are etched from copper foil that is bonded onto one or more insulating sheets. To prevent inter-diffusion of the copper-solder materials, the outer most copper layers of the substrate are finished in a layer of electroless nickel; Gold is then applied over the nickel through a process of immersion which inhibits oxidation and enhances solderability. The entire process is frequently termed ENIG.



(a) Glass fibre style 1080 **(b) Glass fibre style 2116** **(c) Glass fibre style 7628**

Figure 2-16: Standard industry laminate pre-preg weaves

The insulating sheets are formed from laminating (under pressure) a series of epoxy impregnated glass fibre matting known as 'pre-preg'. The weave or interlaced glass fibres of the pre-preg material changes depending upon required circuit board performance. Three typical fibre styles are shown in Figure 2-16 (a) to (c); 1080 giving a smooth, expensive resin rich surface finish in comparison to the heavier and less expensive 7628 of Figure 2-16 (c). The more gaps there are in the weave as illustrated, the more resin which can be included in the finished board, thus affecting not only the dielectric constant of the PCB but also its thermo-mechanical performance.

For higher density area array devices, higher grade styles of glass reinforced epoxy pre-preg are used in the construction of the interposer; particularly in respect of glass transition temperature (T_g). T_g is important since it determines the mechanical stability of the board during the manufacturing reflow process, both in terms of the device package and in the manufacture of the CBA. T_g also limits the maximum temperature a component or product can be subjected to in its end use environment.

For common epoxy laminate resin systems used in the production of interposers, increased temperature causes a corresponding change in the coefficients of expansion of the materials as illustrated in Figure 2-17. T_g is defined by Guiles (Guiles, et al., 2008) as "The temperature at which the mechanical properties of a laminate begin to change rapidly." Glass Transition Temperature is just what its name suggests: it is that temperature at which a material changes from a hard, brittle "glass-like" form to a softer, rubberlike consistency.

Figure 2-17: Glass transition temperature (T_g) curves for various laminates (Ritchey, 1999)

This phase change in resin material properties results in a corresponding significant change in the coefficient of thermal expansion (CTE) from a low value to a high value. Ritchey (Ritchey, 1999) contends that for temperatures less than Tg the CTE in the X and Y direction have values approaching that of copper and glass of the pre-preg used to make up the PCB. When temperatures exceed Tg, the resin becomes the dominant feature in the laminate system expanding at a much faster volumetric rate than the other materials.

Since the resin cannot expand in either the X-Y directions due to the constraints of the copper and glass materials virtually all the volumetric growth of the PCB takes place in the Z axis. It is typical for the Z-direction CTE to increase about four-fold, from 50-60 ppm/ °C below the T_g to 180-250 ppm/°C above it (Guiles, et al., 2008).

Because Z-direction expansion causes strain on the copper plated in holes, the extra expansion above T_g is often responsible for micro-vias and plated through hole copper cracking during processing or rework or cyclic thermal testing. It may also result in "latent defects" that will show up later during normal in-service use, for example Frear (Frear, 1999) recognised that this can also result in delamination of the layers making up the PCB. Bismaleimide-Triazine (BT) is the preferred resin based laminate material used in packaging to-day due to its higher T_g (170 - 180°C) and comparatively cheaper cost compared to alternatives such as FR-4 and FR-5 used in the manufacture of traditional epoxy based laminates. The higher T_g allows the package to withstand high temperature reflow process which occurs during solder sphere attach and mounting of the part to the next layer board (level 2 interconnect).

In designing area array packaging it is important to match the CTE of the interposer to the host PCB of the system. In this way a mechanically compliant system is created in which the main PCB will expand and contract at similar rates during temperature excursions, thus reducing the stress incurred by the solder sphere connection to both objects. BT in this case is ideally suited to main PCB's constructed from FR-4 and FR-5 since they have similar coefficients of thermal expansion of 17-19 ppm/degree C.

Due to the interconnect density of area array packaged parts, the connection between the various layers of a multilayer interposer are achieved using microvias, illustrated in Figure 2-18; in the packaging industry it is generally accepted that these are 'through hole' interconnections of less than 150µm diameter.

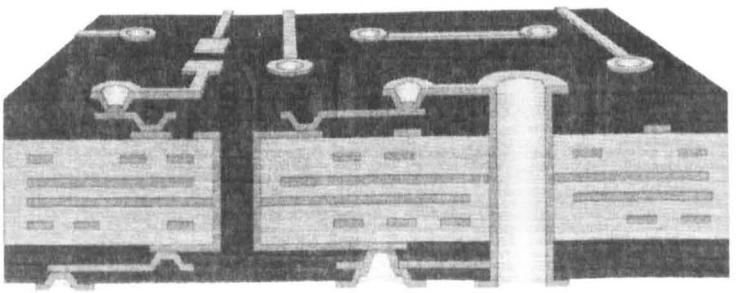


Figure 2-18: Illustration showing microvias used in combination with standard through and buried vias to interconnect multiple layers in interposer substrate.

2.6 Package Overmoulding Technology

Package overmoulding or encapsulation provides mechanical, moisture, vibration and shock protection to the die surfaces as well as the wire bonds and solder bumps of the level one interconnects; in addition it provides thermal management improvements approaching 100 times better than that of bare flip chip mounted on an FR 4 printed circuit board.

As interconnects shrink in size they become less compliant resulting in a corresponding increase in stress observed within the solder joint. This is true whether it is a level 1 or level 2 interconnect and results in a less reliable package. The encapsulation, in combination with any device underfill, plays a critical role in package reliability through ameliorating the stresses caused by the differential expansion of the chip and its substrate (Fielstad, et al., 2003).

Thermoset epoxies, Silicone and to a lesser degree Polyimide's (more often used as underfill) are the primary materials used in the encapsulation process. These resin materials are then bulked out by up to 80% using fillers. Apart from the obvious reduction in cost achieved by the use of fillers they are also included to control the CTE properties of the encapsulant and provide flame retardant properties.

Package encapsulation of area array parts is performed using two common processes:-

2.6.1 Dam and fill encapsulation.

A high viscosity material is dispensed around the periphery of the encapsulation area to form a "dam" into which the fill or encapsulant material is dispensed. This is a time consuming and expensive process which generally is not used for high volume product applications. The dispense technique can generate co-planarity issues with regard to the encapsulation and the interposer board. Stresses introduced by the dispensed dam can cause the interposer board to warp, resulting in a 'potato chip effect' across the package which can make the finished package difficult to mount on the next layer board shown in Figure 2-19.

Figure 2-19: Warpage of un-encapsulated package (Fielstad, et al., 2003).

2.6.2 Transfer moulding encapsulation

Transfer moulding was developed for high volume, low cost encapsulation of parts. In this process the lead frame or finished interposer complete with silicon is placed into the mould tool which restricts the flow areas of the encapsulant. The encapsulant material which has been liquefied through combined heat and pressure is transferred into the mould; resulting in a well defined, flat encapsulation surface with very little warping of the interposer board.

2.7 Summary of Packaging Issues Affecting Reliability

Area array packaged components, like surface mount components experience mechanical interconnect stresses which are the result of CTE mismatches between the device package and circuit board assembly (CBA). This can occur either through thermal excitation (low cycle fatigue) or vibration (high cycle fatigue), which can in turn cause the PCB of the CBA to flex relative to the package. Such primary shear stresses are applied during both the manufacturing process as well as during the mission life of a product, resulting in cracking of the solder joint.

Solder ball interconnections of area array packaged devices, whether level 1 or level 2 are less compliant than peripherally leaded package styles such as QFP, TSOP or PGA which have inherently longer leads.

In combination with moving to lead free solder material configurations, from a coefficient of thermal expansion point of view joint compliance is worsened as die structures, packaging and bump interconnect dimensions reduce. A number of packaging interconnect design features may be implemented to mitigate such risks; namely the inclusion of a 'compliant layer' or interposer in the package which allows the solder balls to physically move in relation to the package and CBA. Increased compliance can also be achieved through changing the connection from solder balls to solder columns improving the CTE compliance by increasing the stand-off height between the silicon and the CBA. A second common approach is modifying the CTE differences and mechanical stress applied at CBA to packaging interconnect through "under filling" the device post soldering.

Here an epoxy mixture is injected between the package and CBA which envelopes the solder ball interconnects and effectively bonds the underside of the package including solder balls to the CBA. Depending on package style and the application, underfill can be selectively applied to just the corners or to the entire underside of the package.

Although helpful in improving board level reliability, underfill voiding, which can occur during the application process, poor underfill material selection or failure of the underfill material to adhere to the silicon or CBA, leading to delamination, can result in both joint and thermal failures of the packaged device. Such failures occur irrespective of whether lead or lead free solder is deployed. Macro or process voiding can also occur in the solder joint which can significantly affect reliability. Primavera (Primavera, 1999) points out the existence of many independent theories on the presence of voids and their formation. Most sources in this paper agree that

voids are formed during the metal oxide reduction and flux outgassing stages of reflow. In addition voids can be formed by entrapped air, mask residue and other debris

For area array packaged components, the principle failure region identified both in the literature and through practice is at the bump to die interface or at the bump to PCB copper pad (Ye, et al., 2007) (Mo, et al., 2009). Zhang and Xie (Zhang, et al., 2001) comment that the strains caused by thermal cycling are more severe at the corners of the die package, the resultant impact on the joint being that coarsening is observed in the microstructure of the eutectic solder, this coarsening being more pronounced near the interface between the solder joint and die bond pad. This interface is rich in intermetallics. Furthermore, Popelar (Popelar, 1997) reports that solder joints located at package corners or outer rows are likely to fail first since they are furthest from the neutral axis of the package or die and are likely to experience larger levels of shear force deformation under cyclic thermal loading.

Bearing this in mind and knowing the solder bump failure distribution of packages it is often the case that an alternative to underfill is to use packaging in which peripheral or corner balls in the package are not used for electrical connections.

Understanding the varieties of interconnect and constructional technologies used in area array packaging and how they influence reliability are instrumental in the correct selection of failure inspection methods and the creation of physics of failure and FEA models.

Chapter 3

Reliability Assessment of Solder Joints

3.1 Introduction

Solder joint performance and reliability are dependent upon the mechanical behaviour of materials which make up the interconnect system and their response to thermo-mechanically induced stresses and strains. Such stress may be encountered either in the field or as a result of accelerated testing in which field observed stresses are replicated and applied in a manner that provides time compression. Time compression is essential since it is clearly not practical, given ever reducing design life cycles, to test in the laboratory for long periods of time in order to replicate years of operational service in the field.

Although such tests are designed to apply stresses representative of the intended operational or mission life of the product, they can never realistically simulate actual use. No single environmental test can replicate a product's end user environment. Therefore, a key element in the development of an environmental test is the determination of the technologies used both in the design or test samples and on the end life usage conditions. Wherever possible there should be a linkage back to real world conditions else the ensuing results will be meaningless (Klyner, 2005).

Stress applied to solder joints through cyclic thermal fatigue is considered in the literature to result in the most dominant failure mechanisms. Bhate observing that 'in essence this is fatigue crack growth problem' (Bhate, et al., 2007) and is frequently studied empirically. The continual reduction in joint and packaging geometries, combined with moving to lead free solder makes the study of solder joint fatigue failures and life prediction one of the most extensively researched areas of electronics and packaging reliability.

The reliability assessment of solder joints may be evaluated in one of two ways. Firstly life prediction modelling in which physics of failure models are used to determine the number of fatigue cycles to fail, and secondly accelerated testing in which components or products are subjected to increased levels of stress until failure occurs. The failure intervals are subsequently analysed using statistical methods to deduce an estimate of in-field reliability and potential failure times.

Naturally the methods are co-dependent, with physics of failure models developed in order to provide prediction of cycles to fail. Subsequent rearrangement produces generalised models describing test environment acceleration factors, which in turn define life test durations.

As dimensions of both interconnect and package become smaller, the ability to observe and track the initiation and propagation of fatigue cracks becomes increasingly difficult, requiring detailed sectioning of samples which is a problematic technique since it is primarily 2D, expensive, time consuming to perform and destructive.

In order to improve our understanding and thereby develop better modelling of solder joint fatigue and cracking requires the development of non-destructive inspection techniques which can be utilised for reliability life testing. This would drive improvements in the demonstration testing that is currently deployed in reliability studies of complex and safety critical product applications.

3.2 Fundamentals of Reliability and Environmental Testing

Reliability is of primary concern both to consumers and those working within the automotive industry, since it is a key indicator of a product's durability or useful life. Poor design, manufacturing and component quality all substantially influence the overall reliability of a product. Often, products and parts may contain defects, which although not severe enough to fail the applied production tests, over time may develop into failures. Thus reliability may be considered as the ability of a product to retain its quality with the progression of time, but this is only one measure of a product's perceived quality (Bentley, 1998).

Although inextricably linked, reliability and product quality are frequently incorrectly used interchangeably. Often the reason for this confusion is because reliability is concerned with performance of a product over its entire lifetime, whereas quality control is concerned with a product's performance at a single point in time, usually during the manufacturing process. Quality control is a vital link in the reliability process as it assures conformance to specifications and reduced manufacturing variance (Reliasoft Corporation, 2008).

A more widely used definition of reliability based on MIL-STD-721C (Defense, 1981) defines reliability as the probability that an item will perform its intended functions without failure in specified environments for a specified period of time under stated conditions.

Mathematically this definition may be expressed as:

$$R(t) = P_r\{T > t\} = \int_t^{\infty} f(x)dx \qquad \textit{Equation 3-1}$$

Where $R(t)$ is the probability of no failures occurring for a given period of time t, t being the operational mission time of the system, assumed to start from time zero.

P_r is probability; T is the time to the first failure and $f(x)$ the failure probability density function describing the failure behaviour of the system. This definition of reliability introduces a number of factors which must be understood and precisely defined in order for a products operational reliability to be accurately assessed through demonstration tests.

3.2.1 Probability

Reliability is quantified in terms of a probability estimate, since the generation of failures or defectives may be considered as being due to random or chance events causing increased levels of stress. Such events can and do occur during a product's manufacture and operating

life and will either shorten useful or operational life, or cause a catastrophic failure of the product.

Clearly by expressing reliability in this probabilistic way gives no information on individual failures, the causes of failures, or any indication of relationships between failures, except that the likelihood for failures to occur varies over time according to the given probability function. Thus reliability engineering is concerned with meeting the specified probability of success, at a specified level of statistical confidence.

3.2.2 Time period

No product has an infinite operational lifetime. Therefore in order to design a product and demonstrate operation without failure, expected product lifetime must be specified. For automotive products this is typically 10 to 15 years. However, it can be specified in units other that time e.g. it may be expressed in terms of distance covered (miles or kilometres) or cycles of operation.

In statistical reliability theory, since the probability of failure occurrence is related to an interval of time or other such continuous variables then it may be expressed by the parameter λ which characterises the incidence of failures, and the reciprocal value $^1/_\lambda$ characterises the average operation time per one failure (Statistics.com, 2009). Defining the operational life of a product is key to determining the duration of testing required to demonstrate reliability compliance.

3.2.3 Intended function and failure definition

Reliability of a product can only be determined through analysis or testing on 'intended function', for a specific failure mode and/or categories of similar failure modes.

Since reference is made to the probability of an unsuccessful or 'failed' outcome in the reliability definition, which by explanation is when the product does not perform as intended or required. It is extremely important to define under what range of environmental conditions the product is expected to function, and the level of product functionality that is deemed acceptable. The term failure can immediately conjure up the notion of a non-recoverable catastrophic event but in real life the actual spectrum of events can range from being a mere parametric deviation outside of a prescribed limit to non-operation of a given function. A failure or several failures, depending on the test acceptance criterion, will usually terminate the reliability testing and initiate an analysis of both the failed product and process. Conversely, a reliability test may be considered successful if over the duration of the testing (which should represent at least one product lifetime) no failures are encountered.

3.2.4 Failure life distribution

It is well established in published literature that products may exhibit failure characteristics defined by a cumulative failure distribution function ($F(t)$) describing the 'failure life' of a product over infinite time, known as the 'bathtub' curve, as shown in Figure 3-1.

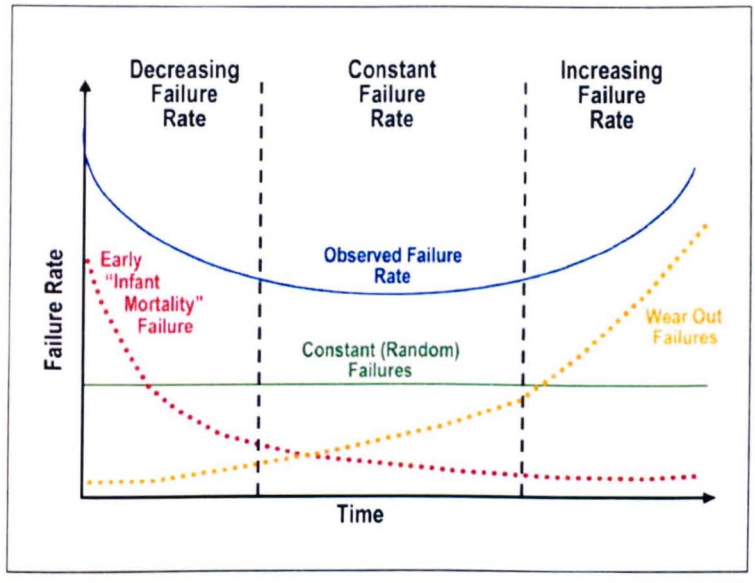


Figure 3-1: Reliability bathtub curve

Examining the instantaneous failure rates ($\lambda(t)$) of a system, product or component over infinite time reveals three distinct phases or regions.

3.2.4.1 Early life failures

During the early part of a product's life cycle, failures may be attributed to design and manufacturing faults interspersed with random or chance component failure events which are the result of poor quality incoming parts. The failure rate falls as design faults are rectified, weak or marginal components are removed and newly introduced product manufacturing processes become stable. The deployment of new manufacturing techniques and technologies can be often-overlooked as a potential cause of early life failures. Here, individual component reliability is affected through overstress of intrinsically weak components. A typical example might be an incorrectly set solder machine temperature which may cause IC delamination effects or assembly line transportation pallets that may introduce high levels of stress (measured in micro-strains) into the printed circuit board.

3.2.4.2 Constant failures

The useful life region of a product is typified by the failure rate reducing to a constant (low) level where failures are generally considered unpredictable and the result of 'random' or 'chance'

failure events. Although failure rate (λ) values in this region may be very low, say ten parts per million, you can rarely have zero failure rate.

3.2.4.3 Wear out or end of life failures

The wearout region, characterised by an increasing failure rate is due to component wearout. For electromechanical type components, this effectively controls the life of the product, since mechanical fatigue comes into play. For electronics based products the general wearout slope is gradual, with product lifetimes running into tens of years. Primarily this is because most wearout is due to chemical and material changes within the components, which are influenced by thermal excitation.

A good example of this is an electrolytic capacitor, which ages rapidly when exposed to high temperature. This is due to the electrolyte within the capacitor drying out as a function of operational hours, temperature of the environment in which it is operating and also the loading to which it is subjected. For semiconductors the wearout is gradual, the bulk of failures being the result more of inherent defects or electrical overstress.

Ebling (Ebling, 1997) describes the bathtub curve as a composite of several failure distribution curves as illustrated in Figure 3-1. For well-designed products, the design life should meet the customers expected design life prior to wear out i.e. over the flat portion of the bath tub curve. All products follow the outline of the bath tub curve although each product will have their own unique shaped curve. This can aid in the characterisation of not only the behaviour of a product or of a specific failure mode, but also in the development of empirical or statistically based fatigue and acceleration models.

Life data or 'Weibull' analysis provides a substantive link between field, test and modelling in reliability engineering studies. Predicting the life behaviour of products in a given test population (typically 63.2% of the population failing) is performed by fitting a statistical distribution to life data for a representative sample set obtained through test or from warranty/field returns.

The Weibull distribution formulated by Waloddi Weibull in 1951 (Weibull, 1951), is an extensively used distribution for analysing life data since it includes distributions of increasing, constant and decreasing failure rates. The values applied to the parameters of *Equation 3-2* are selected to give the best fit to the available data; controlling the scale, shape and location of probability distribution function (pdf).

$$f(t) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \qquad \textit{Equation 3-2}$$

For the 3-parameter Weibull model of *Equation 3-2*, the scale parameter, η, defines where the bulk of the distribution lies (illustrated in Figure 3-2). The shape parameter, β a dimensionless number, defines the slope of the distribution. Populations with $\beta < 1$ exhibit a failure rate that decreases with time, populations with $\beta = 1$ have a constant failure rate (consistent with the exponential distribution) and populations with $\beta > 1$ have a failure rate that increases with time.

All three life stages of the bathtub curve can be modelled with the Weibull distribution and varying values of β as illustrated in Figure 3-2.

Figure 3-2: The effect of β on the Weibull failure rate function (Reliasoft, 2010)

Finally γ, defines the location of the distribution in time. The distribution and its associated function being moved either to the right (if $\gamma > 0$) or to the left (if $\gamma < 0$).

Figure 3-3: The effects of η on the Weibull *pdf* for a common β (Reliasoft, 2010)

In performing reliability studies, reference is made to the characteristic life of the Weibull distribution. Characteristic life is defined by considering the 2 parameter Weibull cumulative distribution function (cdf) equation described in Weibull's original paper (Weibull, 1951) which is commonly written as:-

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \qquad \textit{Equation 3-3}$$

Where β is the shape or slope parameter and η the scale parameter as previously described in *Equation 3-2*. The mean of the Weibull distribution is equal to the characteristic life if the shape parameter is equal to one. This occurs when $t = \eta$ resulting in *Equation 3-3* reducing to:

$$F(\eta) = 1 - e^{(-1)} = 0.632 \qquad \textit{Equation 3-4}$$

Therefore, $F(\eta)$, the characteristic life, is the time by which 63.2% of the units in the population will have failed.

3.3 Fatigue Failure Models, Acceleration Models and Accelerated Testing

There are two ways in which to demonstrate or assess the reliability of solder joints: either perform demonstration tests or simulate joint performance using techniques such as FEA. As interconnect dimensions continue to decrease in size and component constructions become more complex as in SiP, FEA becomes a more viable proposition due to the limited inspection methods currently available for monitoring crack initiation and propagation and the high costs associated with lengthy testing (Zhang, et al., 2003). However it should be noted that the complexity of the models also increases as component construction complexity increases. This may result in modelling in some instances being a less viable alternative to test and inspection.

There are many solder joint fatigue life prediction models proposed in the literature, the most frequently referenced being the plastic strain based approach of Coffin Manson (Coffin, 1954) (Manson, 1966).

Solder fatigue life prediction models are developed based upon the stress, strain and energy data that is obtained from experimental testing of sample products subjected to thermal cycling. These empirically based fatigue life prediction models can be categorised into four groups based on the fundamental process inducing damage in the joint: a) plastic-strain based, b) creep-strain based, c) energy based and d) fracture mechanics based.

The number of available models is further increased with the introduction of lead free solder formulations, where each lead free formulation adds new or additional elements and parameters to existing models in order to replicate or fit the available test data. Clearly the selection of a de facto 'correct model' is difficult and highlights the problems of assessing solder joint reliability and life estimates under field conditions.

Many of the methodologies in the literature are borrowed from established creep and fatigue phenomena of steels observed through long term experimentation (Lee, et al., 2000).
Solder joints are difficult to model due to their exposure in field to multiaxial stresses in which joints are subjected to creep based stress in combination with cyclic strain. There are also additional boundary condition influences affecting life prediction results such as joint geometry, dwell times at thermal extremes, usage factor, soldering defects, grain size and microstructure of the solder. Residual circuit board assembly strains introduced during the manufacturing process complicate the issue even further. The inclusion or exclusion of such behaviours contributes significantly to the ability of existing models to replicate real world applications.
Since fatigue and test acceleration models are based on experimental observations, it is extremely important to have detailed and accurate understanding of the joint behaviour. The development of a non-destructive measurement or observation technique which does not influence joint behaviour results is therefore an important step forward in model development and verification.

3.3.1 Plastic and creep strain based fatigue model approach

Creep is defined as slow dimensional changes in a material resulting from prolonged stress (σ) loading. In metals the time-dependent deformation (creep strain, ε) is also influenced by temperature and the metal alloy being considered. Higher temperatures resulting in increased deformation and reduced mechanical strength. A typical curve of strain versus time is shown in Figure 3-4. The curve showing the instantaneous predominantly elastic strain which occurs on application of a load, followed by plastic strain which occurs over time.

Figure 3-4: Strain *v* time graph, indicating the stages of creep (Plumbridge, et al., 2003)

Plumbridge (Plumbridge, et al., 2003) states there are three stages of creep in metals. Elastic deformation occurs instantaneously on application of a force (or stress) loading represented in Figure 3-4 from time = 0 to ε_0. This is the initial strain rate. Beyond this is the *Primary creep* region in which there is a continuous fall in creep strain rate or material deformation. Continued

loading beyond the primary creep region results in *Secondary Creep*, a region or time period in which the creep strain rate is considered essentially constant or having a linear increase. This in turn is followed by the *tertiary creep* region in which the creep strain rate increases continuously until rupture.

3.3.1.1 Life prediction based on creep

In order to analyse solder joint reliability and provide acceleration factor models for test time compression, physics of failure models must relate the creep energy to useful life, irrespective of a field or test environment.

In the literature, many of the creep life prediction models are based in some way on the Monkman-Grant equation stated as

$$\dot{\varepsilon}_m t_r = C \qquad \textit{Equation 3-5}$$

Where the minimum creep strain rate ($\dot{\varepsilon}_m$) is linked to the dominant creep mechanism, t_r in this equation being the time to rupture (failure) and C a constant related to the material or system ductility (Plumbridge, et al., 2003).

The nature of creep is complex, involving a number of material deformation mechanisms such as 'diffusion controlled dislocation motion' or 'migration of voids', either through the material grain matrix or along grain boundaries as in the principle of grain boundary sliding. Given the existence of multiple deformation mechanisms $\dot{\varepsilon}_m$ could ultimately comprise a number of dominant creep processes and may be defined as:-

$$\dot{\varepsilon}_m = \sum_{i=1}^{n} \dot{\varepsilon}_i \qquad \textit{Equation 3-6}$$

Where $\dot{\varepsilon}_i$ is the i^{th} initial creep strain rate and n the number of nth dominant mechanisms.

For creep life prediction the minimum creep strain rate is linked to the applied stress (σ) by various equations based on the dominant or cumulative creep mechanism

$$\dot{\varepsilon}_m \propto \sigma^n \quad \text{Power law Creep} \qquad \textit{Equation 3-7}$$

$$\dot{\varepsilon}_m \propto \exp(a\sigma^n) \quad \text{Exponential Creep} \qquad \textit{Equation 3-8}$$

$$\dot{\varepsilon}_m \propto [\sinh(b\sigma)] \quad \text{Combination Creep} \qquad \textit{Equation 3-9}$$

Where a and b are temperature dependent constants and n is the power or exponent value.

3.3.1.2 Components and influences on creep

Creep strain rate is predominantly influenced by temperature and stress; increasing temperature providing an exponential increase in creep strain rate. The stress component of creep strain rate on the other hand is more complex since its influence on creep strain rate is entirely dependent upon the dominant controlling creep mechanism which in turn is somewhat material and property dependent.

A common expression for the steady state creep rate given in the literature is (Plumbridge, et al., 2003):-

$$\dot{\varepsilon}_m = A\sigma^n g^{-p} exp\left[\frac{-Q}{kT}\right] \qquad \textit{Equation 3-10}$$

Where g is the grain size of the material and A, n, p are constants, Q the activation energy of the dominant creep process, k is Boltzmann's constant and T is absolute temperature.

Although useful, this equation only defines a steady state system. However in many product field and test environments, failures are more likely to be induced through repeated or cyclic applications of a number of stresses or strains such as those due to thermal cycling. In ductile materials the failure mechanism produced by repeated cycling involves the initiation of a crack, usually at the site of a pre-existing defect or at intermetallic regions in a joint. Gradual growth or propagation of the crack occurs until the material can no longer support the applied strain load, resulting in failure. In less ductile, high strength materials the effects are more pronounced in respect of a more immediate propagation of cracks. In the literature this is often referred to as *Cyclic Fatigue*. For fatigue or cyclic fatigue failures, direct application of the stress and strain energies on their own are not of a sufficient magnitude to induce component failures. However the combination of cyclic stress and strain produces sufficiently high microstrain energies (in the order of 10^{-5} to 10^{-2}) which generate increased localised strain, deforming the material and invoking failures. Plumbridge (Plumbridge, et al., 2003) states that plastic deformation in metals is a permanent deformation of the material caused through sufficient stress being applied to push the material beyond its elastic strain range. For metals used in packaging interconnect the total applied strain, $\varepsilon_{combined}$, is a combination of an elastic component, ε_e, and a plastic component, ε_p.

Thus in terms of strain ranges:-

$$\Delta\varepsilon_{combined} = \Delta\varepsilon_e + \Delta\varepsilon_p \qquad \textit{Equation 3-11}$$

Of particular interest to reliability practitioners and modellers is defining the relationship between stress/strain or strain range and the number of cycles to failure (S-N curves).

Depending on the dominant strain range, a linear relationship may be derived for the combined strain range (Mughrabi, 2000) (Norris, et al., 1969). Plumb (Plumbridge, et al., 2003) writes this as:-

For the Basquin or Elastic strain Range region:-

$$\Delta\varepsilon_e {N_f}^b = C_1 \qquad \textit{Equation 3-12}$$

And similarly for the Coffin Manson or Plastic Strain Range region:-

$$\Delta\varepsilon_p {N_f}^c = C_2 \qquad \textit{Equation 3-13}$$

Where b and c are the respective fatigue strength and ductility exponents, C_1 and C_2 are empirical constants, N_f corresponds to the number of stress cycle reversals.

For solder interconnects the elastic strain rate is deemed relatively small such that the plastic strain becomes the predominant factor. The majority of plastic strain based models use Coffin-Manson (Coffin, 1954) (Manson, 1966) in some form for life prediction.

Empirically derived strain based fatigue models are less useful for making comparative evaluations of reliability performance compared to energy or fracture mechanics based approaches. Lee (Lee, et al., 2000) suggests that this may be the result of many simplifications made in the models and the general complex non-linear behaviour of solder alloys.

3.3.2 Energy-based models

Energy based fatigue life models describe the non-uniform energy dissipation experienced during thermal cycling within the interconnect solder volume. Fractures occurring at a specific susceptible region in the joint volume, usually at the silicon to bump or bump to substrate interface.

Figure 3-5: Hysteresis loop showing stress-strain relationship during a mechanical fatigue cycle (Plumbridge, et al., 2003)

The energy absorbed during the thermal cycle, which comprises of a summation of all applied stress and strain forces on the interconnect is described using the hysteresis loops of Figure 3-5 and Figure 3-6.

Hysteresis loops are frequently used to describe Stress-Strain relationships, due to the complex interaction of both cyclic temperature, dwell time and cyclic stress on the creep behaviour of the material or in this case solder joints. The width of the hysteresis loop being used as a measure of the plastic ($\Delta\varepsilon_p$) and elastic strain ranges ($\Delta\varepsilon_e$) over the applied stress range ($\Delta\sigma$) as illustrated in Figure 3-5. The stress range for the work reported in this thesis is based on controlled thermal profiles.

Figure 3-6: Thermo-mechanical hysteresis loop response (Plumbridge, et al., 2003)

Cycling both temperature and strain produces an asymmetric loop about the stress axis which is the result of the strength of the material varying in response to variation in temperature as illustrated in Figure 3-6. The area of the curve also changes (reduces) in response to the number of cycles the solder joint is subjected to. This can be the result of the inherent strain energy built into the PCB during the manufacturing and assembly process. But can also be due to the geometry of the joint, package under consideration and the thermal cycle parameters. For example thermal cycling applied in a manner which induces shock to the structures invokes higher strain energies. Creep naturally occurs in the solder joints at room temperature; however during thermal cycling stress relaxation of the components and joints occurs during dwell periods at high temperature.

The area inside the loop describes the creep energy dissipated in a single thermal cycle (W_{CR}) at a specified zone in the solder joint (*Damage Integral*). This forms the basis of the Popelar and Wong-Helling model used by Delphi (Chengalva, et al., 2006) to determine the relative damage

of solder joints on a package. Many strain energy based methods are reported in the literature but the general form is usually expressed as:-

$$C(W)^{-\delta} = N_f \qquad \textit{Equation 3-14}$$

Where δ and C are material constants and W is the inelastic strain energy density. Although Dasgupta et al point out that in some cases when using *equation 3-14*, the total strain energy (W) actually comprises of elastic, plastic and creep strain energies as denoted in the hysteresis curves (Dasgupta, et al., 1992).

3.3.3 Fracture mechanics-based models

Fracture mechanics fatigue models are based on the principle of microscopic flaws or defects existing in any solder joint and having the ability to form a nucleation site. From this a crack may propagate through the material volume during the application of an applied stress, in this case thermal cycling.

Solder joint life predictions may therefore be derived from characterising crack propagation behaviour through stressed materials as a function of time geometry and environmental conditions as suggested by Liu (Liu, 2001).

The progression of the crack and growth velocity through any stressed material is a function of time, interconnect geometry and the applied environmental conditions. A basic velocity equation cited by (Liu, 2001) is given as:-

$$\frac{da}{dt} = B(Y\sigma\sqrt{\pi a})^n \qquad \textit{Equation 3-15}$$

Where a is the crack length, σ is the applied stress, Y is an interconnect geometry parameter, B and n are empirical constants which are thermally dependent.

A typical fracture mechanics equation stated in the literature is the Paris-Erdogan equation which relates the crack length propagation per cycle as (Paris, et al., 1963):-

$$\frac{da}{dN} = C\Delta K^q \qquad \textit{Equation 3-16}$$

Where a is the crack length, C and q are material constants, N cycles and ΔK which is equivalent to $\Delta\tau\sqrt{\pi a}$ the stress intensity factor.

3.3.4 Accelerated test models

In performing reliability assessment or demonstration testing, stress conditions are usually applied at higher magnitudes than seen in the field. The duration of testing being either until failures occur (test to fail) or time terminated, in which all samples subjected to the test

environment must survive in order to show compliance to the required level of reliability. The latter is an example of Type I censored testing sometimes referred to in the literature as 'Binomial' or 'Test to Bogey'.

In the development and execution of reliability demonstration tests the physics of failure fatigue models discussed earlier for a given failure mechanism are used to determine the predicted time or cycles to fail. 'Time compression or acceleration being determined through a time transformation of the high stress level applied during the test to normal stress levels observed in field that induce the same modes of failure and produce the same failure distribution' Viswanadham comments that in applying this strategy, the stress conditions applied must not significantly change the material properties. For example at extremely low temperatures embrittlement of materials occurs, whilst the converse is true at high temperatures where softening of mould compounds takes place (Viswanadham, et al., 1998).

The acceleration factor (A_f) used to determine test time durations may be written as follows:-

$$\text{Acceleration Factor } (A_f) = \frac{\text{Time to fail in Field } (t_f)}{\text{Time to fail in Test } (t_t)} \qquad \textbf{Equation 3-17}$$

Equation 3-17 may also be written as:-

$$\text{Acceleration Factor } (A_f) = \frac{\text{Life Duration }_{\text{Normal}}}{\text{Life Duration }_{\text{Accelerated}}} \qquad \textbf{Equation 3-18}$$

From experience, reliability tests assume that different stress conditions observed in the field and test laboratory environment will present the same mode of failure in the materials or structure. Therefore acceleration factors may be expressed in terms of either time to first failure as shown in *Equation 3-17* or in the case of thermal cycling tests as the number of cycles (N) to failure as shown in the generalised equation of *Equation 3-19*. In this equation, t can be either time to first failure or the percentage of first time failures.

$$A_f = \frac{t_f}{t_t} = \frac{N_f}{N_t} \qquad \textbf{Equation 3-19}$$

Moreover, since the time or cycles to failure in *Equation 3-19* for a specific failure mode is entirely dependent on Physico-chemical interactions, then many physics of failure models such as those listed in Table 3-2 result. The most widely deployed model being Coffin-Manson (Coffin, 1954) (Manson, 1966) which also forms a key component of many lead and lead free acceleration factor models in use to-day.

$$\text{Coffin Manson Acceleration Factor} = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \qquad \textbf{Equation 3-20}$$

Where m is an empirically derived ductility constant for the material or failure mechanism under consideration. Table 3-1 shows a selection of commonly used values for m. Typical values covering lead solders lies between 1.9 and 2.5.

Table 3-1: Empirically derived ductility constants (Source GMW3172 Handbook)

The thermal range to which the sample is exposed in the test chamber and field environment respectively is denoted ΔT_{Test} and ΔT_{Field}.

A number of alternative models referred to as 'modified Coffin-Manson', have been used with varying degrees of success to model crack growth in solder joints due to repeated thermal cycling. For the more complex versions of the basic Coffin-Manson model, we are principally identifying the constituent effects within the thermal cycle which may cause damage. The acceleration factors from each of these components are multiplied together to derive the overall acceleration factors as illustrated in Table 3-2.

Increased strain resulting from the thermal range over which the cycle takes place acting on the different CTE's of materials used in the construction of a product is cited as one of the primary damage mechanisms. The larger the increase in thermal range the greater the strain. In Mo's work on BGA area array packaging (Mo, et al., 2009) it was found that solder joint cracks formed between the Intermetallic Compound (IMC) and PCB pad and the interface of the IMC and solder bump. Thick IMC and irregular grain size being quoted as primary contributory factors. Additionally, Ye (Ye, et al., 2007) reports that in double-sided BGA packaging tests all

joint fractures appeared at the package side irrespective of whether they were located top or bottom side of the substrate and that the outer rows of balls failed first.

For each temperature excursion, dwell at minimum and maximum temperature allows material creep to continue until the thermal stress applied to the system has dissipated into the material. There is much argument in the literature with regard to the actual damage being invoked. It is argued that for lead free testing, dwell times should be significantly longer than those used to test lead components to ensure the same inherent solder microstructure damage. Grossmann (Grossmann, et al., 2002) points out that accelerated testing having short dwell times at thermal extremes influences the reliability performance in terms of cyclic fatigue life. Selection of dwell time must be long enough to enable the full strain introduced by the temperature swing and CTE mismatch of materials involved to relax. Solder alloys which creep slowly have a better performance than those having fast creep rates. Grossmann's measurements showed that lead free alloys creep 10 to 100 times slower than tin lead. The impact dwell time has on test acceleration factors was established through empirical testing and sectioning of solder joints. Within defined boundaries, ramp rates of 3-4°C/min have little impact on fatigue crack growth. However at gradients of 10°C/min or more, changes are induced at the molecular level in the interconnect which provide increased acceleration and reduced time to failure due to Grain Boundary dislocation and Sliding (GBS). This postulate is supported by work undertaken by Clech (Clech, 2005) in which he observed that ramp rate has minimal effect on cyclic reliability interconnect performance. Interestingly in this work the effect of ramp rate goes in the opposite directions for lead and lead-free alloys. This supports the commonly held belief that slower ramp rates generally produce small acceleration factors in Lead free solders whilst the converse is true for fast ramp rates in leaded solders.

There are a number of significant points to be gained from Table 3-2. Firstly, no single model is correct. In many cases they are principally derived from the Coffin Manson (Coffin, 1954) (Manson, 1966) low cycle fatigue model and then tailored using added correction factors or parameters in order to make the model fit the observed data or material set. Secondly, for each of the models in the table their usage is limited to the 'calibrated' thermal range over which they were evaluated. For example in the Clech model (Clech, et al., 2009), the thermal range of the test samples was -10°C to +100°C, clearly not an automotive or avionics environment. Thirdly, the Coffin Manson model, although used extensively, is conservative in its estimation of solder joint fatigue life. This could be due to the fact that it was developed for temperatures below 50% of the solder melting temperature in Kelvin, but it is also suggested that the conservative nature is a result of its development history. Much of model development being based on observing solder material grain structure post testing using micro sectioning techniques. In summary, all fatigue models used in both FEA and when transformed to provide acceleration factors for test time calculations, must be calibrated to real life over a defined thermal range.

Model Identifier Name	Acceleration Model	References
Coffin Manson	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m$	*(COFFIN, L F Jr, 1954) (MANSON, S S, 1966)*
Coffin Manson with inclusion of dwell time.	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \left[\frac{Dwell\ Time_{Test}}{Dwell\ Time_{Field}}\right]^{0.136}$	*Environmental Specification GMW3172, 2004*
Norris Landzberg Classic frequency component	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \left[\frac{Thermal\ Cycle\ Frequency_{Field}}{Thermal\ Cycle\ Frequency_{Test}}\right]^{\frac{1}{3}} exp\left(1414\left\{\frac{1}{T_{max\,Field}} - \frac{1}{T_{max\,Test}}\right\}\right)$	*(NORRIS, K C and Landzberg, A H, 1969)*
Norris Landzberg Modified, dwell duration component	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \left[\frac{Dwell\ Time_{Test}}{Dwell\ Time_{Field}}\right]^{0.136} exp\left(2185\left\{\frac{1}{T_{max\,Field}} - \frac{1}{T_{max\,Test}}\right\}\right)$	(PAN, N et al., 2005)
Clech (HP, SMTAI 2009) Principally derived for lead free	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \left[\frac{1 - c.\Delta T_{Test}{}^{-1}\left(t_{cold,Test}{}^{-0.19275}.e^{705.5/T_{min,Test}} + t_{hot,Test}{}^{-0.19275}.e^{705.5/T_{max,Test}}\right)}{1 - c.\Delta T_{Field}{}^{-1}\left(t_{cold,Field}{}^{-0.19275}.e^{705.5/T_{min,Field}} + t_{hot,Field}{}^{-0.19275}.e^{705.5/T_{max,Field}}\right)}\right]$	*Proceedings of SMTAI October, 2009*
General Motors	$A_f = \left[\frac{\Delta T_{Test}}{\Delta T_{Field}}\right]^m \times \left[\frac{Dwell\ Time_{Test}}{Dwell\ Time_{Field}}\right]^{0.136} \times [1.22 \times (Ramp\ Rate)^{0.757}] \times \left[e^{2185 \times \left(\frac{1}{T_{max\,Field}+273} - \frac{1}{T_{max\,Test}+273}\right)}\right]$	*GMW3172 Electrical Component Testing User Guide Revision 19 – 13/02/2008 Larry Edson*

Table 3-2: Comparison of acceleration factor models

The principal novelty in the proposed ultrasound inspection method is that it opens up the possibility to develop more accurate models based on observing crack formation and propagation. This has not been done in a non-destructive manner before.

3.4 Non-Destructive Inspection Methodologies

Several non-destructive testing (NDT) techniques have been proposed to investigate, detect and locate defects in microelectronic devices, their associated packaging and their interconnection to a substrate, including an organic printed circuit board (PCB) under investigation here.

Table 3-3: Current and future state inspection requirements for next generation packaging, updated from original table by Dias (Dias, et al., 2005)

These include Optical inspection using microscopes, X-ray microscopy (Moore, et al., 2002), Acoustic Micro Imaging (AMI) / Scanning Acoustic Microscopy (SAM) (Pahl, et al., 2004), electronic speckle pattern interferometry (Lee, et al., 2004), scanning electron microscopy (SEM) and laser ultrasound coupled to interferometry (Liu, et al., 2004). Optical interferometry-based techniques can measure in-plane or out-of-plane thermal displacement in flip-chip packages to indirectly evaluate solder joints, but their applications are limited.

Such inspection and imaging tools can be used to observe problems with adhesion, delamination, cracking, wetting, and voiding and assist solution verification process. Optical techniques are limited in their assessment of solder joint surface finish or visible deformation and cracking of the solder joint. They are not able to inspect either inside the packages or hidden solder joints.

Although X-ray imaging and SAM are presently widely used, none of the techniques are able to examine next generation packaging. This is highlighted in Table 3-3 where the resolution limits are reached as the structures under investigation e.g. solder joints; shrink below a few tens of microns.

3.4.1 X-ray

The primary information carrying medium of this technology is electromagnetic radiation in the high frequency region (10^{18} Hertz) of the electromagnetic spectrum. Although real-time X-ray inspection is a mature technology it is challenged by the continual reduction in component packaging and interconnect technology sizes, new potting materials and increased number of substrate layers.

Inspection is performed by using the variation in the transmission absorption of X-ray energy due to differing materials used in the construction of a component. A material absorbs X-rays proportional to its atomic mass and density (Bernard, 2003). This makes X-ray inspection particularly suitable for the investigation of volumetric type defects.

Four primary X-ray inspection technologies are identified in the literature for deployment in the non-destructive inspection of area array packages, namely 2D through transmission X-ray, oblique angled viewing, 3D digital tomosynthesis and 3D tomography. In 3D X-ray tomography the volume of the object under examination is computationally reconstructed from a series of 2D X-ray images (Krastev, 2007), (Kroning, et al., 1995). The most commonly used X-ray inspection techniques are 2D, i.e. through transmission and oblique angled viewing. In these techniques X-rays are generated at a point source and pass through the entire sample and are vertically projected onto an image intensifier (detector) as shown in Figure 3-7.

Fundamentally, X-ray system resolution can be no better than the diameter of the X-ray source or spot size of the transmission tube. Current transmission tube designs are capable of achieving spot sizes at or below 1μm. The requirement to penetrate dense materials within area array and system in package (SiP) devices requires the use of high acceleration voltages and current in order to analyse fatigue and micro voiding in solder joints.

Figure 3-7: Diagram of 2D X-ray imaging principle (Focalspot, Inc.)

This translates to a larger spot size and therefore reduced contrast, contrast being the key feature of imaging using X-ray.

Like SAM the majority of conventional systems can only provide 2D imagery. Detection of cracks within the interconnect is extremely difficult due to the large amount of material within the structure absorbing the X-rays and therefore masking the crack. In order to view circuit board assemblies comprising of multilayer circuit boards, stacked area array packages and stacked die, it is often necessary to tilt the sample in order to get an unobstructed view of the feature of interest, thereby creating a pseudo 3D image. The key problem here is that feature resolution is difficult since the angular displacement introduces image distortion.

X-ray laminography and X-ray tomography alleviate this problem somewhat since the image intensifier is rotated over the sample and image 'slices' are collected. The reconstruction of each slice in tomography is done by computer, requiring major computing power and distortion of the image due to angular rotation must be accounted for (Pahl, et al., 2004). Laminography has been widely used in the semiconductor industry. This technology was developed to inspect PC boards for defective solder joints, but its resolution was limited because it required high X-ray flux for rapid pass/fail solder joint inspection (Moore, et al., 2002).

3.4.1.1 Resolution and feature imaging challenges

The lateral resolution or focal spot size in X-ray systems is primarily determined by the X-ray source (or tube) and the system geometric magnification. Open tubes with high magnification offer higher resolution than closed tubes. For 3D X-ray systems, axial resolution or layer separation is important and relies heavily on the development of processing algorithms to separate the images into layers.

Developments documented in the literature by Zhang et al (Zhang, et al., 2004) suggest improvements in both equipment and software have resulted in layer separation of 10μm for X-ray beams having a spot size of 5 to 10μm. Subsequent hardware improvements have also allowed 2D systems to offer detail detectability better than 0.5μm (Yxlon, 2011).

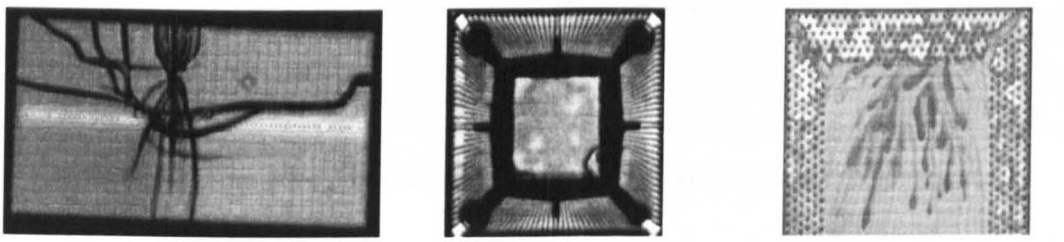
In addition to focal spot size, the imaging of component features is also influenced by material penetration which is power level dependent. The power level being determined by the acceleration of electrons in the tube, which in turn is controlled through adjustment of tube voltage and thermionic emission current over the range 30 to 160kV and up to 1mA respectively.

Bryant (Bryant, et al., 2001) identified a number of technology challenges, not least that current X-ray open tube design has in reality minimum feature recognition of 3μm. Aside from material penetration issues, limited pixel count and poor greyscale sensitivity make differentiating between very small and similar density materials not possible. The dark areas within an image correspond to regions of higher material thickness, and therefore higher X-ray radiation absorption is represented by grey scale levels determined from the digitised bit rate.

Therefore in the case of standard imaging technology which is limited to 8bits or 256 grey levels, significant improvement can be made by using digital imaging running 16bit technology improving significantly both the grey scale sensitivity up to 65,000 levels and pixel count. Smaller feature recognition has moved down to 0.6µm although this is still not good enough for nanotechnology.

3.4.2 Acoustic micro imaging (AMI)

AMI has been used for inspection and failure analysis of microelectronic packages. It has been effective in the measurement of gap type defects such as voids or material delamination typically found in adhesives or epoxy underfill as published by Semmens et al (Semmens, et al., 1996), Angrisani (Angrisani, et al., 2002) and Augereau (Augereau, et al., 2002). AMI can produce high resolution images capable of detecting gap-type defects inside packages as illustrated in Figure 3-8.



(a) Cracked Die (b) Voiding (c) Flip chip underfill Voiding

Figure 3-8: Gap type features imaged using scanning acoustic microscopy (Sonix Inc.)

Such defects are imaged by using the fact that all or part of an incident ultrasonic wave is reflected at the interface of two dissimilar materials. The materials forming the internal structure offer different acoustic impedances to the ultrasonic wave passing through the sample, the magnitude and phase of reflection being a function of the material acoustic impedance given in *Equation 3-21* :-

$$Z_i = \rho_i \times v_i \qquad \textit{Equation 3-21}$$

Where, Z_i is the acoustic impedance of the material in the i_{th} layer of the test artefact, ρ_i is the density of the material in the i_{th} layer and v_i is the velocity of sound in the i_{th} layer.

For area array components, typical values for acoustic impedance and material density are given in Table 3-4.

Material	Density (g/cm^3)	Wavelength (mm) at 25MHz	Acoustic Impedance ($kg/m^2s \times 10^6$ or MRayls)
Air (20°C)	0.00129	0.014	0.00041
Alumina	3.86	0.416	39.56
Aluminium	2.70	0.25	16.90
Copper	8.90	0.188	41.83
Epoxy Resin	1.20	0.104	3.12
Glass (Quartz)	2.70	0.223	15.04
Gold	19.7	0.130	63.8
Lead (Pb)	11.2	0.088	24.6
Moulding Compound	1.72	0.157	6.76
Nickel	8.84	0.224	49.5
Silicon	2.33	0.344	20.04
Silver	10.6	0.144	38.0
Tin	7.3	0.132	24.2
Water (20°C)	1.00	0.059	1.48

Table 3-4: Acoustic impedance of common electronics packaging materials

Note: Acoustic impedance values for various formulations of lead and lead free solder must be obtained empirically.

Figure 3-9: Diagram showing reflections through a material boundary and also when encountering an air gap (Courtesy of Sonoscan Inc.)

With reference to Figure 3-9(a), where the incident angle of the ultrasound energy entering the material boundaries is zero, the relative strength of the transmitted (T) and reflected (R) energy may be calculated from:-

Reflection Coefficient (R)

$$R = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$ ***Equation 3-22***

Transmission Coefficient (T)

$$T = \frac{2Z_2}{Z_2 + Z_1} \qquad \textit{Equation 3-23}$$

Since the acoustic impedance of air is low compared to solids, the incident pulse is fully reflected at a solid-air interface as illustrated in Figure 3-9(b).

The impedance differences of the dissimilar boundary materials also affects the polarity of the returned (echo) pulse energy which can be useful in determining the construction of the artefacts under examination as summarised in the following table.

Table 3-5: Impact of impedance on return pulse polarity (Courtesy of Sonoscan Inc.)

There are principally two types of acoustic microscope which can be deployed in the study of area array components; the Scanning Laser Acoustic Microscope (SLAM) and Scanning Acoustic Microscope (SAM). Although both instruments use high frequency ultrasound energy to image internal cracks and defects within the material structure of a component, their operation is fundamentally different. SLAM (Wey, et al., 1991) is a through transmission mode technique in which ultrasound energy is applied to the test artefact via a transducer, illustrated in Figure 3-10. As the ultrasound energy propagates through the entire volume of the sample any voids or dissimilar materials encountered will attenuate the transmission of the acoustic wave. On reaching the surface of the sample a scanning laser detector is used to detect variations in the transmitted ultrasound signal. This data is then converted into an image. The technique is not that dissimilar to X-ray inspection, having similar limitations.

However, unlike X-ray and SAM, SLAM is only good for the inspection of thin samples. One disadvantage of SLAM is that a protective coverslip must be applied to the component, usually via gold sputtering to protect the component surface since the energy of the laser induces localised heating that may damage the component surface.

Figure 3-10: Illustration of the two main AMI techniques (Courtesy of Sonoscan Inc.)

Unlike SLAM, SAM is a surface measurement technique in which a focused transducer and pulse-echo technique are used to both generate and receive ultrasound energy at different depths within the test sample as shown in Figure 3-10. The transducer is scanned across the surface plane of interest using a 3 axis scanner whilst emitting and receiving the ultrasound energy. The time separation between surface and internal reflections are used to determine the inspection depth within the sample, with Z axis movement being used to control the transducer focus.

In pulse echo systems, the returned ultrasonic signal contains multiple echoes from the various material interfaces at different depths within the inspection sample. Not all of these echo signals are useful when reconstructing the final image. To improve image quality a process known as 'gating' is used to select from the multiple signal returns a specific pulse reflection observed at a given depth within the sample as illustrated in Figure 3-11.

Figure 3-11: Gating at various depths within a sample (Courtesy of Sonoscan Inc.)

The 'gate', represented by vertical green lines in Figure 3-12 is placed around the signal region of interest which represents a time slice on the A Scan (real time oscilloscope waveform of the reflected acoustic signal). The segment of the signal lying within the gate region is then analysed and the result contributes to the final image.

Figure 3-12: Gating at various depths within a sample (Courtesy of Sonoscan Inc.)

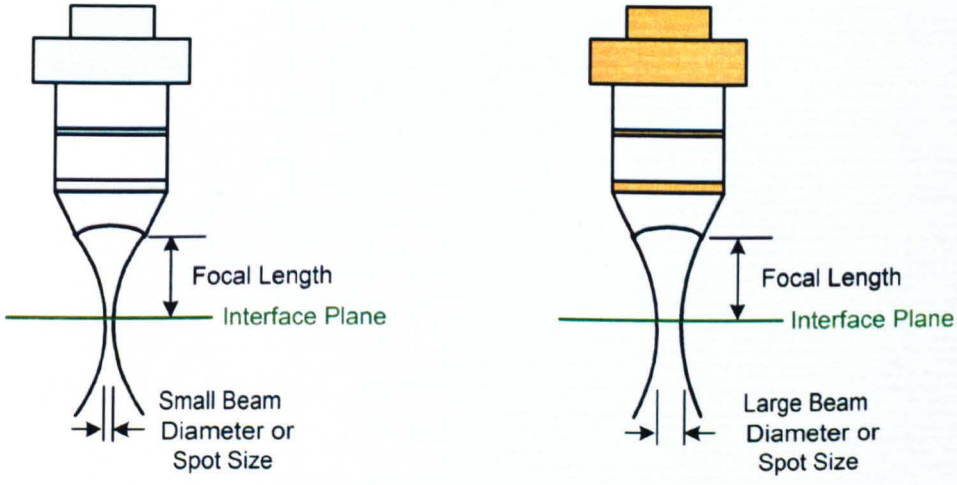
Various companies use different gating methods. Sonix for example use a 'box 'method in which ultrasound energy that exceeds the upper and lower horizontal box limits within the vertical time boundaries is processed. Sonoscan use an automatic gain control for the amplitude and a user variable time boundary setting.

The imaging results and feature resolution of SAM systems is determined largely by the fundamental frequency of the incident pulse in combination with the design and focal length of the installed transducer. SAM systems have the capability to measure very thin air gaps, typically better than 0.16μm for transducer frequencies of 230 MHz. The resolution data for the most commonly used transducers are detailed in Table E-1 of Appendix E.

Although higher frequency transducers are capable of higher resolution, the acoustic energy in the signal does not penetrate very deeply and improved performance can only be gained for

relatively thin samples. Lower frequencies give greater penetration but are unable to provide the required lateral and axial resolution.

It is this axial resolution i.e. the minimum separation between two interfaces located in a direction parallel to the acoustic beam that can be imaged as two separate interfaces which provides the main challenges with regards to imaging features such as delamination, cracks at closely-spaced interfaces and penetration through multiple interfaces with high ΔZ (acoustic impedance changes). Axial resolution is typically defined as being half the wavelength of the transducer frequency.



(a) High Frequency – High Resolution, Short Focus, Less Penetration

(b) Low Frequency – Lower Resolution, Long Focus, High Penetration

Figure 3-13: Diagram illustrating influence of transducer frequency on resolution

An equally important feature of the transducer is the beam diameter or spot size shown in Figure 3-13 which determines the detection capability or lateral resolution of the feature being imaged. From Table 3-3 we are informed that 1μm or better is required in order to image features found in new packaging styles.

Beam diameter or spot size may be estimated from Kino's (Kino, 1987) approximation stated in *Equation 3-24*:-

$$\text{Beam Diameter(BD)} = 1.22\ (\text{FL} \times v)/(\text{D} \times f) \qquad \textbf{Equation 3-24}$$

Where:

FL = Focal Length

v = Velocity of sound in material

f = Transducer Frequency

D = Diameter of piezo electric crystal

The feature resolution for a given transducer may be calculated from *Equation 3-24* given the following (Kino, 1987):-

$$\text{Resolution (reflection mode)} = \text{BD} \times 0.707 \qquad \textit{Equation 3-25}$$

And depth of field is given by (Kino, 1987):-

$$\text{Depth of Field } (\Delta Z) = 7.1 \times \left(\frac{\text{FL}}{\text{D}}\right)^2 \times \frac{v}{f} \qquad \textit{Equation 3-26}$$

For the work in this thesis a transducer frequency of 230MHz (SK230/MP with focal length of 0.375" (9.525mm)) was selected in order to view the fine features of the flip chip solder joints which are 140 microns in diameter.

Using equations *Equation 3-24* to *Equation 3-26* the feature resolution of the transducer can be specified as 15.9 microns spot size and 11.3 microns resolution. This is also confirmed in Table E-1 of Appendix E provided by Sonoscan, suggesting the smallest features we can observe to be 15 microns.

There are many scan modes possible with SAM, the most widely used being A-scan and C-scan modes. The A scan mode consists of the real time oscilloscope waveform of the reflected acoustic signal (data) collected at a single X-Y point on the sample at a specific focused depth (Z).

C-scan mode is the image display of the reflected acoustic data at a specific focused plane of interest within a sample. The acoustic data is collected along an X-Y plane at a depth Z and so may be thought of as an image formed from multiple A scan data points in the Z plane.

3.4.3 Acoustic micro imaging and X-ray inspection comparison study

From the work reported it can be seen that both AMI and X-ray imaging techniques possess the capability to assess the quality of hidden solder joints. However, each technology has distinct discriminating features which are suitable for the inspection of certain defects in particular applications. AMI has a high axial resolution and is an effective approach for detecting gap-type defects such as voids, delamination, disbond and thin cracks ($\sim 0.1\mu m$ in the z-direction) due to the strong reflection of ultrasound at a solid-air interface. These defects are difficult to find by X-ray inspection alone owing to low contrast and limitations on the resolution of the X-ray imaging tube. To investigate the potential of AMI and X-ray imaging for reliability testing of real electronic packages, a comparison study has been carried out on inspection of BGA and flip-chip packages.

Figure 3-14(a) shows an X-ray image of the solder bonds of a flip-chip, where one solder bump labelled A has not reflowed. The unreflowed joint is observed by examining the consistency of the geometric features, e.g. diameter and roundness. However, it cannot be identified from contrast alone. It could also be argued that the joint above bump A has not fully reflowed, since

they do not have the 'pear drop' shape of bumps at the top of the image which represent good joints.

Figure 3-14: X-ray and AMI images Flip-Chip on Ceramic substrate (Zhang, et al., 2004)

The corresponding C-scan image shown in Figure 3-14(b) shows not only the unreflowed bond labelled B, but also that there is a gap/void in the neighbouring bond labelled C which was missed by X-ray inspection. This supports the hypothesis stated earlier that this bond has also not reflowed. This clearly demonstrates that gap-type defects are difficult to find using X-ray alone due to low contrast, whilst the opposite is true for AMI which is highly effective at observing such defects.

Since 2D X-ray inspection has a high lateral resolution, it is able to identify volumetric defects such as solder bridges and broken wires as highlighted in the red circle of Figure 3-14(c). AMI is unquestionably the most appropriate non-destructive method to evaluate solder joint quality in flip-chips. However the same is not true for complex multilayer organic substrates populated with area array components. In such assemblies, the area array parts also contain multilayer substrates or interposers. Under such conditions, AMI of the solder joints is extremely challenging because of the high attenuation and scattering of ultrasound energy off the weave and multilayer tracks of the substrates and interposer.

This was deduced through investigating the behaviour of commercial SiP devices reflowed onto an organic circuit board and subjected to thermal testing using a 2D AMI inspection system.

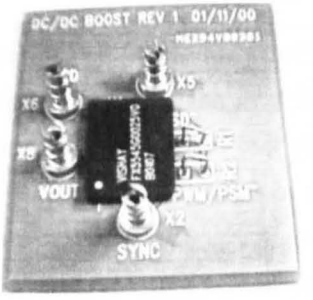
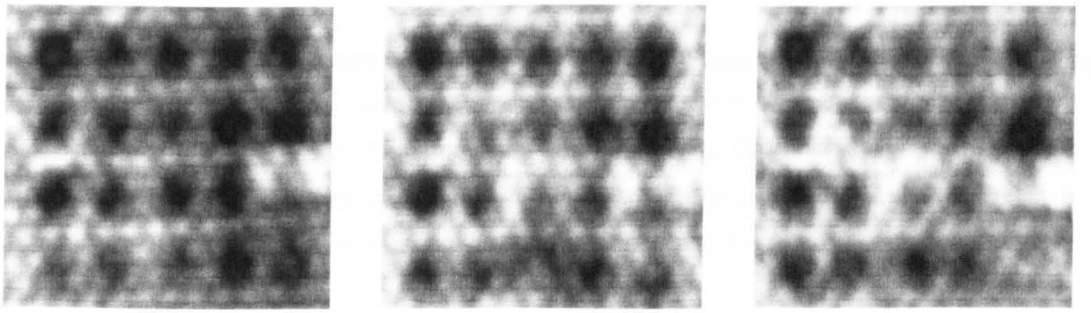


Figure 3-15: Vishay FunctionPAK® Power BGA DC-DC converter demonstration board

Four DC-DC converter demonstration boards shown in Figure 3-15, realised using FunctionPAK® Power BGA technology were manufactured using controlled processes and supplied by Vishay for testing. The FunctionPAK® power BGA comprises a number of surface mount passive and semiconductor devices interconnected using a multilayer FR-4 PCB interposer onto which solder balls are attached. This complex structure in itself is difficult to image both from an X-ray and AMI point of view. Prior to the start of environmental testing the boards were non-destructively inspected using X-ray and AMI. Typical results are shown in Figure 3-16(a) and Figure 3-17.

Test boards were instrumented with thermocouples and mounted to a fixture placed into the basket of a two zone thermal shock chamber. Additional wiring provided dc power and connections to resistive loads allowing functional operation throughout the powered portions of testing. The samples were pre-conditioned for 504 thermal cycles by subjecting them to an unpowered thermal profile comprising a -40°C cold soak followed by a hot soak of +85°C for a dwell time of 10 minutes at thermal extremes. Transition time between thermal extremes was less than 20 seconds and controlled by the basket transition time between hot and cold chambers of the thermal shock chamber. Ignoring the transition time this would result in a thermal cycle time of 20minutes. Following pre-conditioning the test boards were powered and subjected to -45°C to +85°C chamber thermal profile for 840cycles.



(a) Before thermal shock **(b) after 1344 cycles** **(c) after 2688 cycles**

Figure 3-16: Imaging of PowerBGA™ using 5MHz acoustic transducer

To ensure the desired thermal profile of -40°C to 115°C was achieved, the body of the PowerBGA's were instrumented with thermocouples and the chamber set point temperature lowered to -45°C. Thermocouple readings confirmed that when powered the BGA achieved -40°C and self-heating increasing the upper temperature of the BGA to 115°C when powered. This led to further studies on component self-heating influencing test profiles and acceleration factors experienced by the artefact under test were published at LJMU GERI's annual research symposium (Braden, et al., 2009). Although beyond Vishay's thermal specifications quoted for the device it provides accelerated ageing of the component as discussed earlier in this chapter.

Throughout the environmental exposure, voltage regulator output was monitored using a voltmeter to ensure functional operation. This is not ideal since solder joints can be cracked but

provide electrical connection resulting in many hundreds of hours of operation before total failure is encountered.

On completion of the 1344 thermal cycles the test samples were removed from the chamber and re-inspected. Typical AMI inspection results are shown in Figure 3-16(b).

Prior to the samples being returned to test for a further 1344 cycles following the same test regime sequence the samples were baked at 40°C for four hours to ensure any remaining water from the acoustic inspection process did not influence the test. On completion of the cumulative 2688 thermal cycles the test boards were re-inspected.

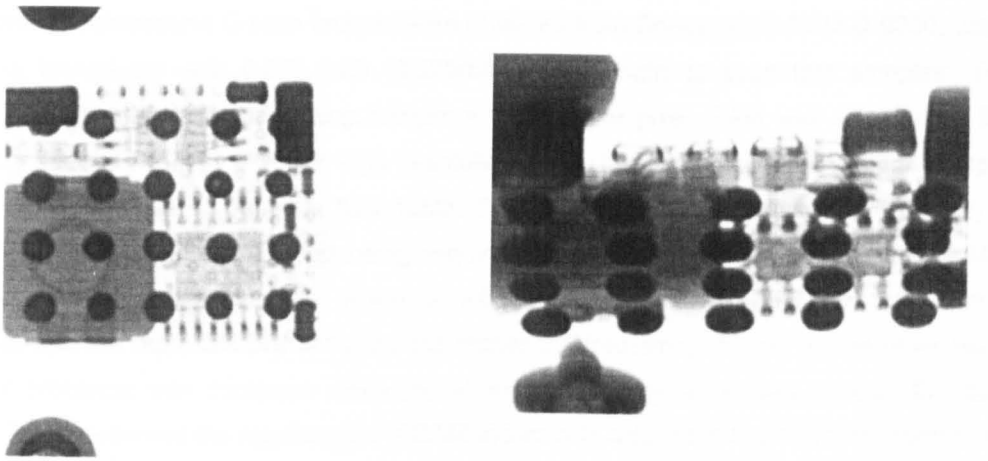
AMI inspection of the solder joints of the Vishay FunctionPak PowerBGA™ proved to be very difficult. When imaged through the component side of the circuit board and package assembly insufficient penetration was achieved using high frequency transducers (>30MHz) to allow detailed information to be gained from the solder joint interconnect. The internal multilayer 'interposer' of the SiP package made imaging difficult. All that could be viewed was the outline of components and fibre lattice structure of the interposer.

The same was also true when scanning through from the Circuit Board Assembly (CBA) substrate side of the board. Penetration of the multi-layer organic structures found in the CBA and interposer of the area array component present considerable challenges to high frequency AMI because of the high attenuation and scattering of ultrasonic energy at each interface within the layered construction. This in turn makes resolution of cracks, crack dimensions and propagation all but impossible.

Using a 5MHz transducer images were made of the Vishay PowerBGA™ at the start of testing, after 1344, and 2688 cycles of thermal shock as shown in Figure 3-16. Although penetration of the CBA substrate was possible using this frequency and the images show progressive degradation of the solder joint attachment, there is insufficient resolution and clarity in the images to reliably determine detailed solder joint integrity, resolve crack nucleation points and crack propagation features.

Moreover the use of higher frequency transducers would not give sufficient penetration and result in a poorer image. This clearly demonstrates that using lower resolution frequency small defects cannot be resolved. In fact from the images obtained we can detect some solder bump degradation resulting from the environmental exposure. However, we are not able to determine accurately if the joint is making an electrical connection or has cracks in it. We certainly cannot make estimates of fatigue life experienced. In this example, the 140µm size of the solder ball is of sufficient magnitude in diameter to be viewed amongst the weave of the substrate. As bump sizes reduce to <60 µm, then it becomes near impossible to discriminate between the bump and gaps in the laminate weave.

The problem is equally challenging for X-ray inspection of solder joints in this type of electronic packaging. The corresponding X-ray images for the Vishay FunctionPak PowerBGA™ are shown in Figure 3-17.



(a) Conventional 2D X-ray **(b) Oblique angled viewing**

Figure 3-17 X-ray imaging of PowerBGA™ after environmental testing

From the images obtained it is clearly difficult to evaluate the connection quality of the solder joints. There is little depth information contained in the images when using conventional 2D X-ray inspection machines even when imaged at an oblique viewing angle. As a result solder joints of interest may be shadowed by other structures within the package. 3D laminography can produce sliced images, but the resolution is low. One distinct advantage of X-ray imaging is that it does not suffer from 'edge effects' as seen in AMI.

3.4.4 Development of advanced acoustic micro imaging techniques

Conventional acoustic micro imaging is a time domain imaging technique (TAMI). For thin/small packages, however, detection of the internal features and defects in the packages are approaching the resolution limits of AMI. As a result, the reflected echoes from internal features are superimposed, resulting in degraded ultrasonic images. One way to increase AMI resolution is to use higher acoustic frequencies. However, higher frequencies provide less penetration through materials. A better alternative is to utilize digital signal processing methods to improve the resolution. Recently, acoustic frequency domain imaging (FAMI) has been introduced by Semmens and Kessler (Semmens, et al., 2002) where Fast Fourier Transform (FFT) algorithms were used to separate the reflected echoes into individual frequencies. Many anomalies can be imaged more meaningfully by FFT images, but frequency domain imaging will degrade or even fail if the reflected echoes are overlapped in the frequency domain. Several novel methods to improve the resolution and robustness of AMI without increasing ultrasonic frequencies have been developed in the host research group within LJMU under the leadership of Dr Guang-Ming Zhang and to which the author was a contributor. The accumulated body of work is summarised in and published by Zhang et al, (Zhang, et al., 2005), (Zhang, et al., 2006a), (Zhang, et al., 2006b), (Zhang, et al., 2006c).

In this work, the ultrasound C-scan images were obtained from Sonoscan C-SAM D-9000, using a 230MHz transducer with 0.375 inch (9.525mm) focal length to scan test samples. The acquired images scan resolution being 8.89µm × 8.89µm per pixel. SAM was selected as the preferred inspection tool due to its high resolution and sharp imaging capabilities, sharper imaging making it easier to estimate flaw depth. The higher frequency ultrasound (230MHz) in combination with slower scan speed being required to resolve micro flaws within the solder bump. For high thickness samples, which is not the case in this research application less penetration into the materials are achieved the higher the frequency. SLAM on the other hand has fewer problems with thickness since the ultrasound energy is passed through the bulk material. This overcomes the requirement in SAM systems to adjust the focal spot for each scan depth to ensure precision in the flaw definition. However, SLAM does require access to both sides of the test parts unlike SAM.

Although SAM imaging is not instantaneous due to slow scan speeds of 0.1 images per second compared to 30 images per second achieved using SLAM inspection SAM does have the advantage of only requiring access from one side of the board in order to make the measurements.

3.5 Experimental Design and NDE of Solder Joints

Experiments were developed to study solder joint through life behaviour using non-destructive techniques. The fatigue life failures of solder joints are monitored by crack plane diameters measured using AMI. Area array components including flip-chips were mounted on a test board and subjected to highly accelerated thermal cycle testing. The experimental design also considered the application of AMI to through life inspection to examine the hypothesis that component floor plan layout and substrate thickness all interact to influence the reliability of solder joints in area array packages.

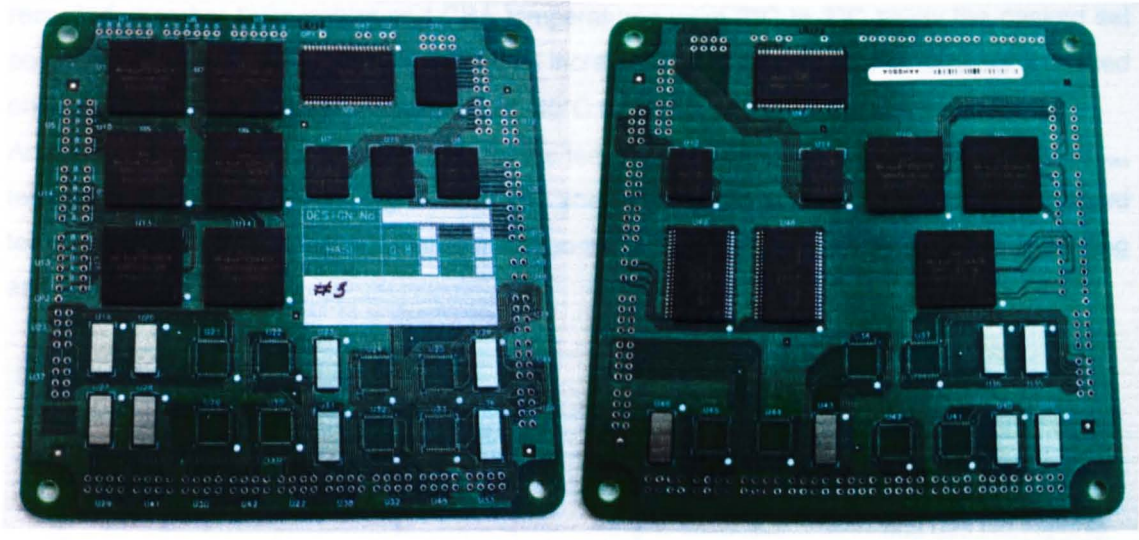
3.5.1 Floor plan layout test board design and construction

An organic test circuit board assembly containing a number of area array part styles, circuit board finishes and substrate material thicknesses was designed and fabricated. This multipurpose test assembly is detailed in the table of Appendix A.

Parts were placed on either side of the circuit board in three configurations in order to study the effects of floor plan layout and PCB dynamics on solder joint reliability, as illustrated in Figure 3-18. The configurations comprised double-side mirror (back to back) assembly, double-side mirrored placement 50% offset relative to one another and single-side assembly. The study only considered double-side mirrored and single-side placed flip-chip components on organic FR-4 substrates of 0.8mm and 1.6mm thickness having a Hot Air Solder Levelling (HASL) lead finish.

The flip chip packages used contained 109 solder bumps of 125µm height positioned in a staggered fashion as two rows at the periphery of the package. The rectangular die 3948µm ×

8898µm in size having a thickness of 725µm was reflowed without underfill to the organic substrate. This enabled failure generation in the shortest possible time, since the lack of any underfill maximises component stresses when the CBA is thermally cycled.



Layout solder side 1 (L01) Layout solder side 2 (L02)

Figure 3-18: Photograph of completed circuit board (RSS1 and RSS2)

3.5.1.1 Test set up and thermal profiling of test boards

Prior to commencing accelerated testing, Circuit Board Assemblies (CBA) were instrumented with type T thermocouples to evaluate the thermal profile of the CBA as well as the flip-chip components. Thermal profiling representative test samples prior to undertaking environmental testing is essential since the thermal mass of products combined with the thermal characteristics of the chamber can produce an on-board thermal profile which does not replicate the desired test profile. This can result in significant errors in test acceleration and simulation results. It is a particular issue when performing powered thermal cycle testing, where product self-heating whilst powered can add significant temperature increases to the PCB temperatures (Braden, et al., 2009).

Eleven thermocouples were connected to a computer controlled data logging system comprising of an Agilent 34970A fitted with two 34901A 20 channel multiplexer modules. Agilent Bench link 3 software was used for data collection in order to minimise programming time.

Two instrumented boards of 0.8mm and 1.6mm substrate thickness were placed into a thermal shock chamber. The boards were suspended vertically by their mounting screw holes using wire clips. The clips were suspended from a wire mesh fixed to the chamber basket. This method of suspension was chosen in preference to simply placing the boards horizontally into the chamber basket. As the large thermal mass of the basket, compared to the test boards would

substantially skew the results of the thermal profiling activity and the thermal profile applied to the boards during test.

The profiling activity was undertaken twice. The first time the theoretical or desired acceleration profile (-40°C to +130°C) was programmed into the chamber controller. Over two full cycles the recorded chamber temperature and CBA temperatures were 2°C to 3°C below the desired set point. The chamber T_{max} set point value was increased to 134°C in order to achieve a desired on board homogeneous test temperature of -40°C to 130°C on the components and PCB.

Analysis of the logged temperature data for the test samples revealed an average on board T_{max} temperature of 132°C was being achieved as shown in Figure 3-19. These resultant on-board temperatures for the increased chamber set points were used as input data for the modelling and simulations.

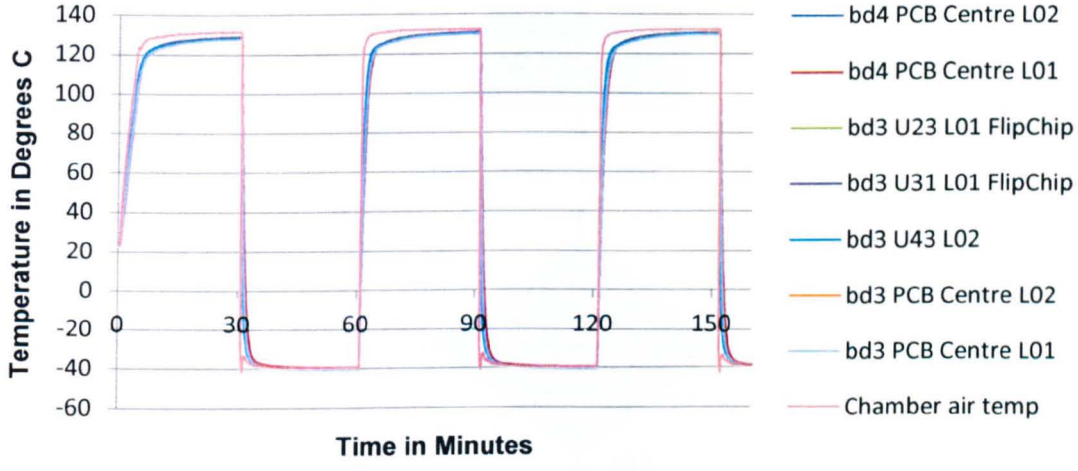


Figure 3-19: Test thermal profile - chamber set point -40°C to +134°C

3.5.2 Test regime / setup

Two HASL Pb finish test boards of 0.8mm and 1.6mm substrate thickness were subjected to the thermal profile described in Figure 3-19 and test and inspection sequence of Figure 3-20. Prior to starting the test, the flip chips on the boards were X-rayed and ultrasonically imaged using a 230 MHz transducer. AMI Images were taken of the die to bump interface since in the literature this is an undisputed region in which cracking will occur, and is the predominant failure mode. From experience, cracking does not usually occur in the centre of the solder bump and is less likely at bump to organic substrate interface. The test profile used was -40°C to +132°C with a 30 minute dwell at minimum (T_{min}) and maximum (T_{max}) for 96 thermal cycles.

This is equivalent to 96 hours testing since 1 cycle = 1hour. Observations in an earlier experiment had shown catastrophic failure of the flip chip solder bumps at greater than 100

cycles. Bumps were so badly cracked that in many cases the devices either fell off the circuit board during the thermal cycling or when the test samples were handled.

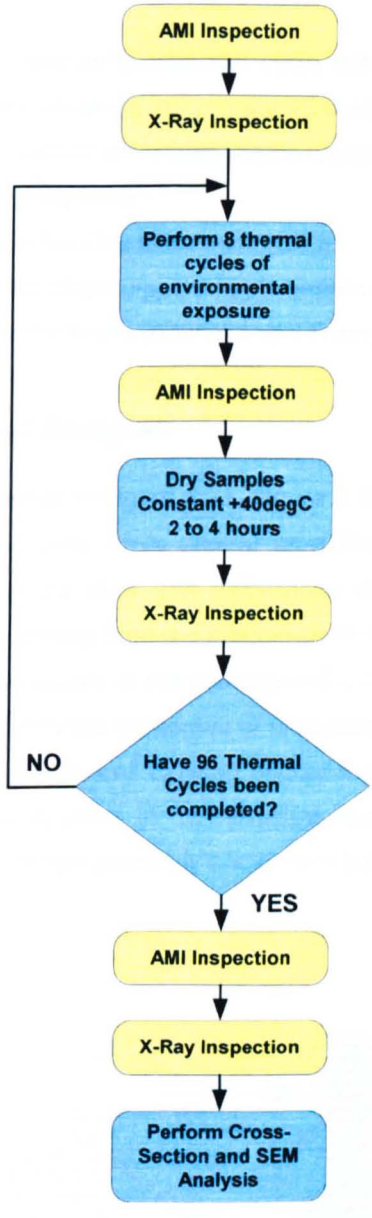


Figure 3-20: Flow Chart of Test and Inspection Regime

The 96 cycles were further broken down into 8 cycle inspection intervals where the test boards were taken out of the chamber to perform AMI and X-ray imaging to examine for cracks as indicated in the test flow chart of Figure 3-20. Post AMI imaging the CBA's were carefully dried in a thermal chamber at a temperature of +40°C for several hours to drive out additional moisture collected by the circuit board material and plastic packaged parts prior to continuing the testing.

This prevents additional stress being applied to the CBA due to ice formation during the -40°C exposure of the first thermal cycle in each 8 cycle exposure. The presence of cracks at the chip to bump interface was determined by tracking the image intensity level changes at the solder joint regions of interest.

Although ultrasound inspections were performed at 8 cycle intervals, in this chapter due to the large quantity of data and images obtained, only images taken at 0 cycles and 96 cycles are considered. A full dataset is archived on electronic media located at the rear of the thesis. The primary CBA case studies investigated were:-

(a) Single side flip chip placement (U23).

(b) Mirrored flip chip component placement (U31 and U43).

(c) Substrate thickness (0.8mm and 1.6mm) for scenarios (a) and (b).

3.6 AMI Inspection of Test Samples

It can be seen from the images shown in Figure 3-21, Figure 3-22, Figure 3-23, Figure 3-24 and Figure 3-25 (a) and (b) that the solder joints appear as a black ring with a dark grey area generally located in the centre of the joint. The differences in the greyscale intensity levels within the images are determined directly from the magnitude of the reflected signal.

The dark grey region indicating the quality of the bonding and a connection between the die and bump exists. However, due to the intrinsic properties of ultrasound, waves striking the edge of a material results in the signal being scattered causing degradation and loss of information. This reduction or loss of return signal appears in the resultant image as a missing black region surrounding the grey of the bump centre as clearly shown in Figure 3-21 image A and image C.

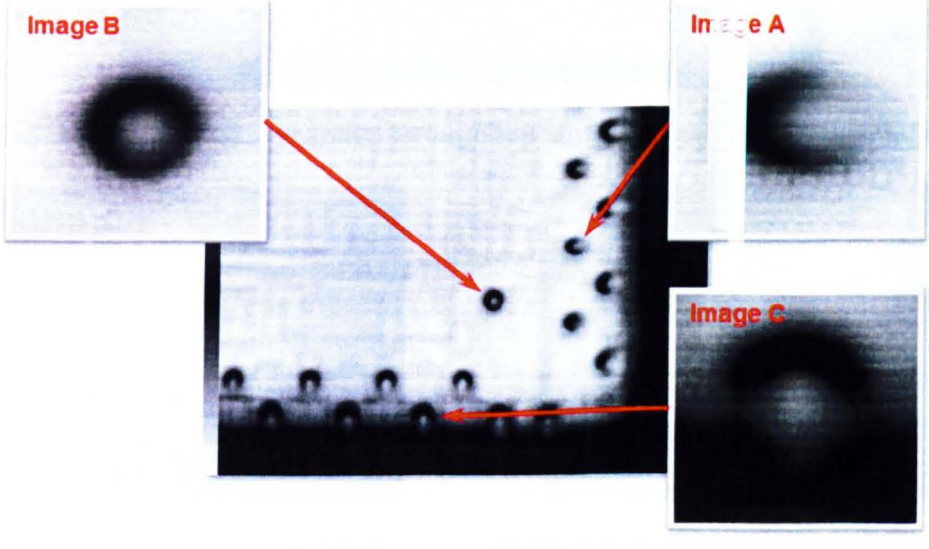


Figure 3-21: Solder joints at different locations on the Flip- Chip

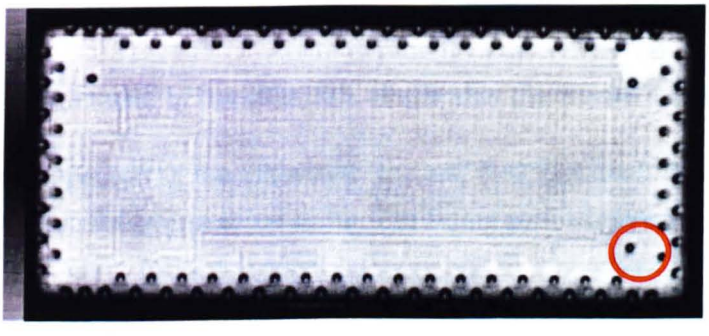
This phenomenon is known as an 'edge effect' and occurs for solder bumps in close proximity to the edge of the silicon, resulting in elongation of the solder ball image and in some cases a

black region around part of the bump. For solder joints located away from the edge of the silicon, a full black outer ring encloses the grey region of the connected bump signifying that it is least affected by the peripheral edge effect as shown in image B of Figure 3-21.

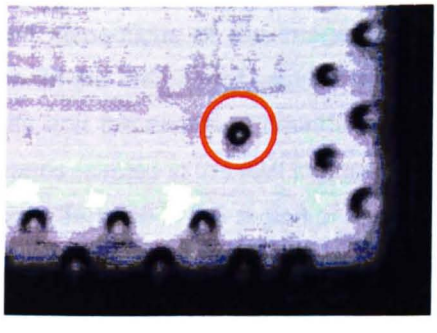
This suggests the inner rows of solder joints on the flip chip package are likely to provide more accurate sources of cycle to fail information since they suffer less edge effect. Hoh (Hoh, et al., 2008) and Semmens (Semmens, et al., 1997) suggest that for inboard solder joints, edge effects are created as a result of the spherical nature of the bump surface.

Moreover, in the post 96 cycle images of solder joints it is evident that ageing of the joint increases the diameter of the grey area in the centre of the bump in addition to the intensity changing from grey to white. In doing so the black outer ring becomes less visible. In some images there is fading of the black ring which leads to blurring of the brightest region boundary as illustrated in image A and image C of Figure 3-21. This creates added challenges when post processing the image to determine the crack plane diameter estimate.

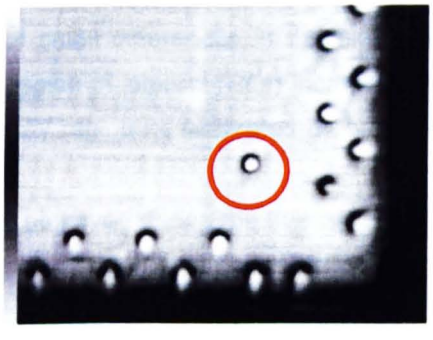
Figure 3-22, Figure 3-23(c), Figure 3-24 and Figure 3-25 (c) and (d) shows the image of flip chips after 96 cycles of exposure to the highly accelerated thermal cycle test. The lower right corner was selected in order to illustrate and examine the changes resulting from continuous thermal cycling. Solder bump 107 (circled in red) was selected since it is inbound of the die edges and so is less susceptible to edge effects.



(a) C-Scan image of U23 (scanned through top surface of package) 0 thermal cycles

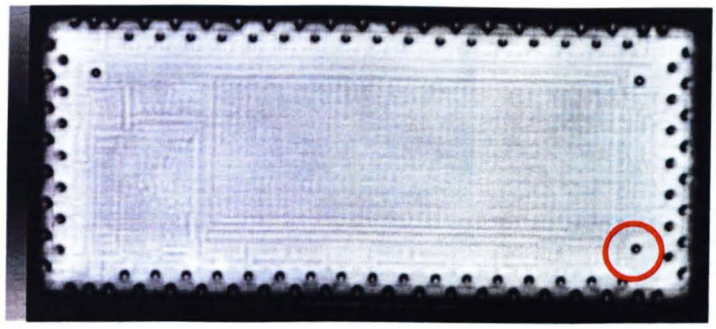


(b) Magnified image (a), bottom right corner at zero cycles.

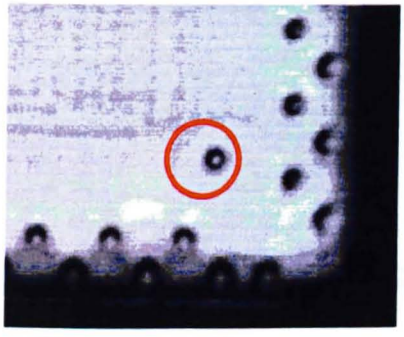


(c) Magnified C-scan image, U23 bottom right corner after 96 thermal cycles

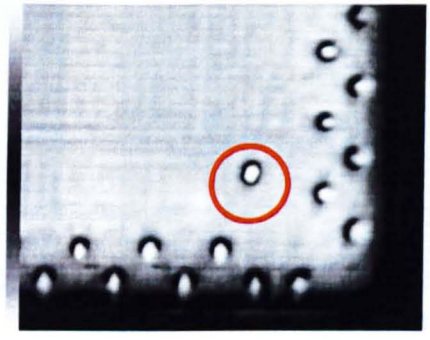
Figure 3-22: AMI images of flip chip U23, single side placement 0.8mm substrate



(a) C-Scan image of U23 (scanned through top surface of package) 0 thermal cycles



(b) Magnified image (a), bottom right corner at zero cycles



(c) C-scan image, focused on U23 bottom right corner after 96 thermal cycles

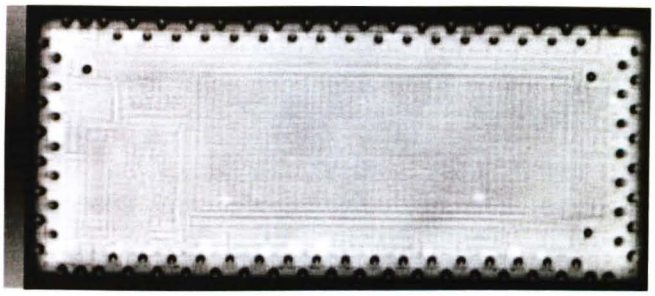
Figure 3-23: AMI images of flip chip U23, single side placement 1.6mm substrate

Clearly from visual inspection of the ultrasound images, it can be seen that defective bumps have brighter intensity in the middle of the bump. The higher pixel intensity level being the result of the air gap formed when there is a crack between silicon and solder bump. As discussed previously, the gap produces a large acoustic impedance mismatch resulting in most of the ultrasound energy being reflected back to the transducer and consequently producing regions of higher image intensity.

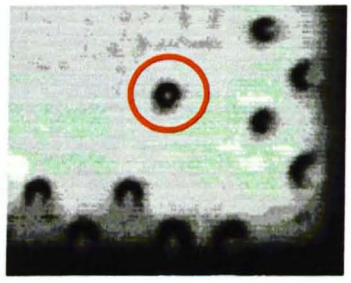
Detailed inspections of the images show evidence of small differences in the high intensity regions. In the majority of cases it was seen that the region of interest (ROI) increased in both intensity and the enclosed boundary of the high intensity region as illustrated by bump 107 in the images (circled in the AMI images).

It is this difference in the region of high image intensity observed during the thermal cycling test to which further novel analysis has been applied in order to quantify the crack plane diameter, and therefore provide an estimate of the number of cycles to fail lifetime (Chapter 5).

It is clear that the task of visually interpreting the images apart from being time consuming is not practical and that further post processing of the images is required in order to objectively obtain discernible features. Differences are noted between the 0.8mm and 1.6mm substrate.

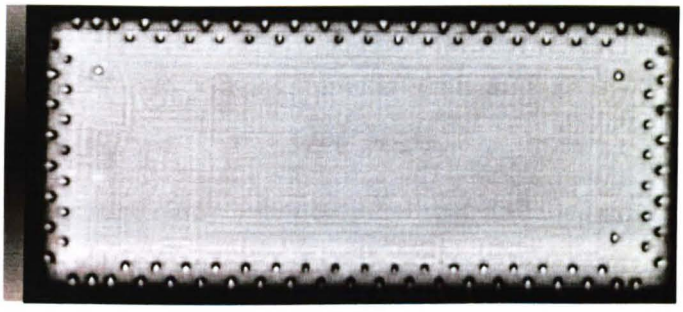


(a) C-Scan image of U31

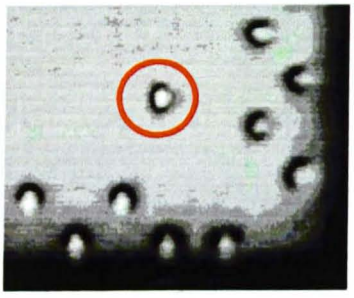


(b) Magnified bottom right corner on U31

Zero Thermal Cycles Performed



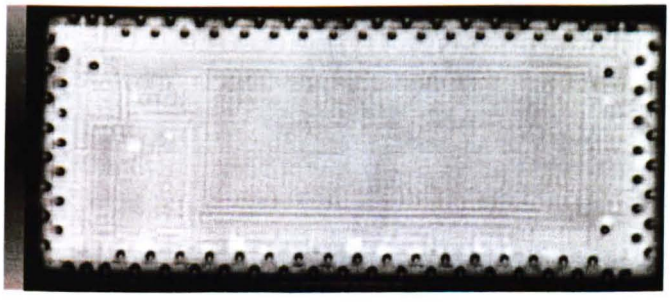
(c) C-Scan image of U31



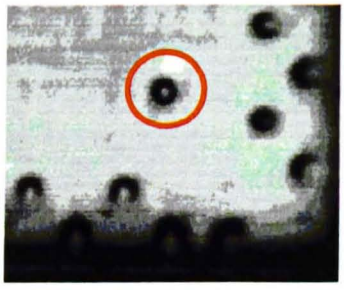
(d) Modified bottom right corner on U31

96 Thermal Cycles Performed

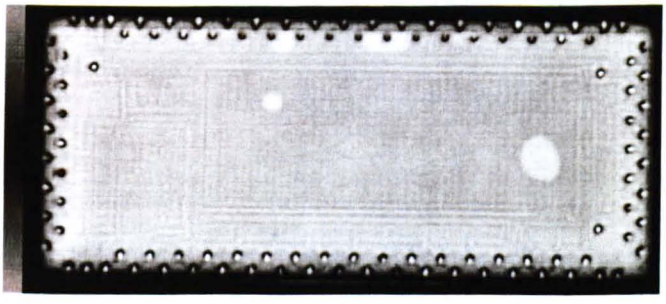
Figure 3-24: Mirrored Component Placement U31 reflow side 1, 0.8mm substrate



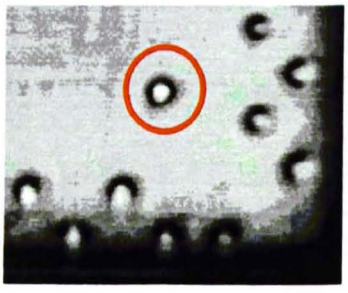
(a) C-Scan image of U43 at zero thermal cycles



(b) Magnified bottom right corner on U43

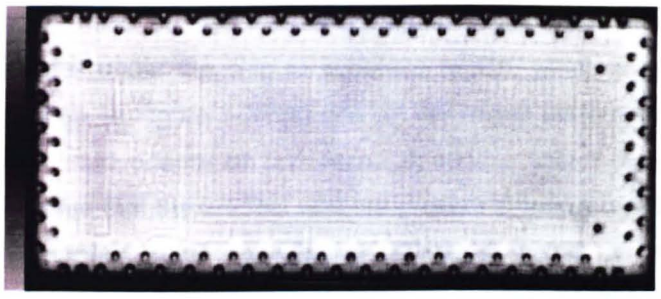


(c) C-Scan image of U43 at 96 thermal cycles

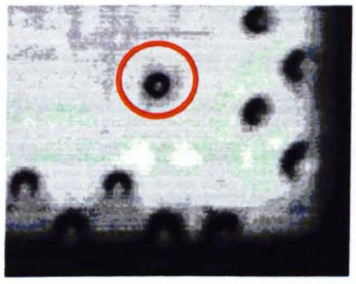


(d) Modified bottom right corner on U43

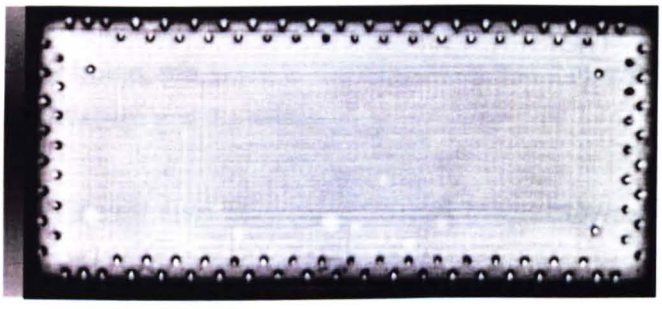
Figure 3-25: Mirrored Component Placement U43 reflow side 2, 0.8mm substrate



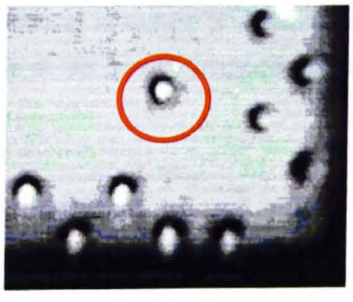
(a) C-Scan image of U31 at zero thermal cycles



(b) Magnified bottom right corner on U31



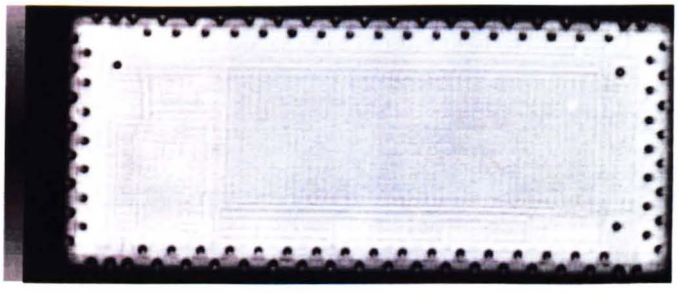
(c) C-Scan image of U31 at 96 thermal cycles



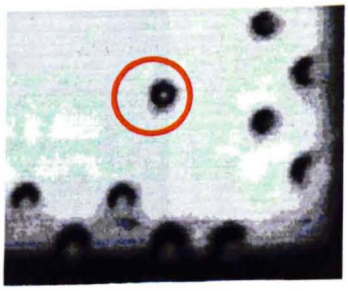
(d) Modified bottom right corner on U31

Figure 3-26: Mirrored Component Placement U31 reflow side 1, 1.6mm substrate

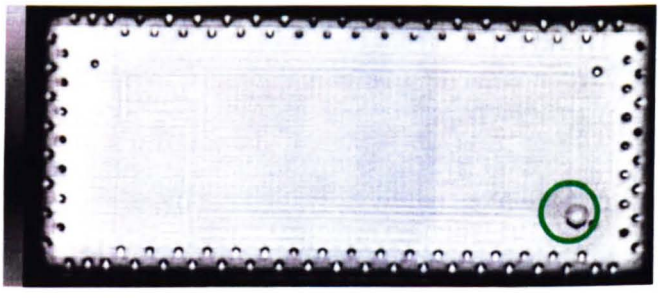
One point to note with AMI imaging, and this is illustrated in Figure 3-25 (c) and Figure 3-27(c) and (d) is that other artefacts are visible within the images.



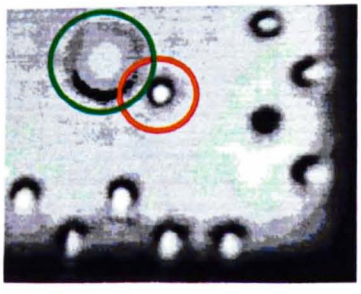
(a) C-Scan image of U43 at zero thermal cycles



(b) Magnified bottom right corner on U43



(c) C-Scan image of U43 at 96 thermal cycles



(d) Modified bottom right corner on U43

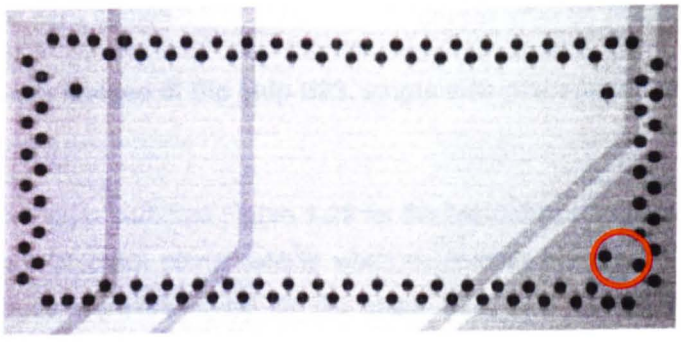
Figure 3-27: Mirrored Component Placement U43 reflow side 2, 1.6mm substrate

In the case of Figure 3-25 (c) lighter regions are observed which may be attributed to air bubbles under the chip to substrate region, which is an artefact from the AMI measurement process. In Figure 3-27 (c) and (d) the region surrounded by green circles is an artefact which could inadvertently be processed as another solder bump. Review of the collected image data revealed that the artefact was not present in earlier inspection images. This would suggest that the artefact could be either a particle or defect on the surface of the die, although from experience it is more likely to be an air bubble. Inspection with a high magnification microscope did not confirm this or identify a possible root cause.

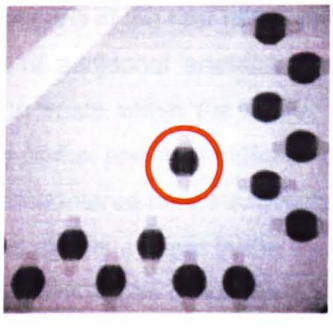
Since image outline of the artefact indicates that it may be spherical in nature and similar to a solder bump, this leads to the hypothesis that it may in fact be an air bubble trapped between the substrate and the silicon.

3.7 X-ray and Microsectioned Inspection of Test Samples

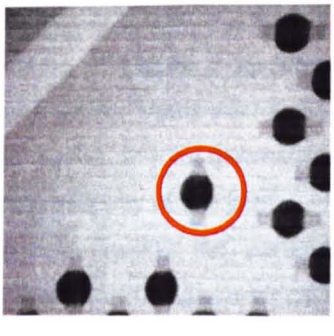
Selected X-ray images, imitating those captured for AMI were taken throughout the environmental exposure cycles. This included images for flip chips U23, U26, U31 and U34 for both the 0.8mm and 1.6mm substrates. All images are available on the electronic storage medium at the back of the thesis.



(a) X-ray image of U23 0 thermal cycles

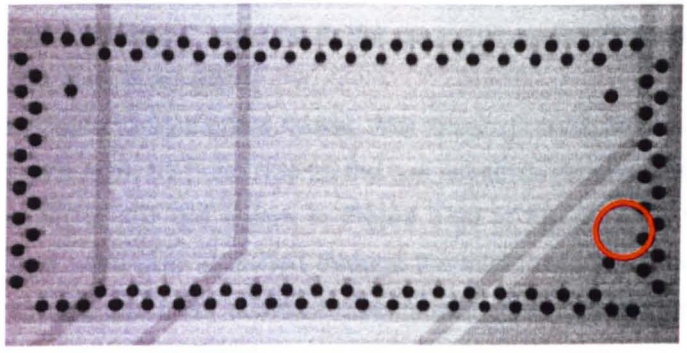


(b) Magnified image of U23 bottom right corner zero cycles

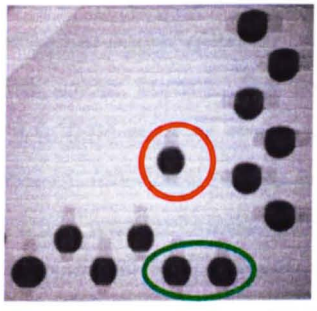


(c) Magnified image, U23 bottom right corner after 96 thermal cycles

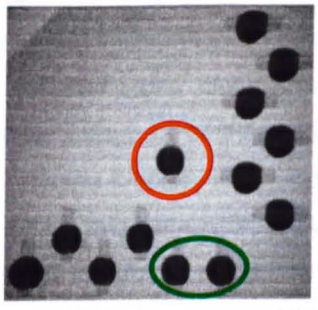
Figure 3-28: X-ray images of flip chip U23, single side placement 0.8mm substrate



(a) X-ray image of U23 0 thermal cycles



(b) Magnified image of U23 bottom right corner zero cycles



(c) Magnified image, U23 bottom right corner after 96 thermal cycles

Figure 3-29: X-ray images of flip chip U23, single side placement 1.6mm substrate

The X-ray images in Figure 3-28 and Figure 3-29 for the two substrate thicknesses do not show any solder joint crack or crack plane defects when comparing images at 0 cycles and at 96 cycles. Similar images were observed for flip chips U26, U31 and U34 and conclusively demonstrate that 2D X-ray is not an appropriate inspection tool for the through life monitoring of gap type defects. Further images of the various configurations and inspection points are archived on DVD at the rear of this thesis.

A number of additional artefacts can be seen in the images of Figure 3-29 which may be attributed to voids within the solder (bounded by the green lines). Voids can result from the outgassing of flux and may indicate manufacturing process issues. In joint geometries as small as those encountered here such voids can impact the overall reliability of the joint.

Distortion is clearly evident in the X-ray images of the complete flip chip die, particularly in the upper and lower edges of the die and bump rows. Such aberrations or geometrical distortions occur even in the best designed and constructed lens and is the result of small errors in alignment and centring of multi-element optical systems.

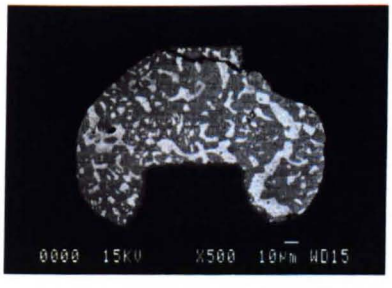
They can never be avoided completely, but can be minimised. The smaller the geometry of systems being measured the worse the problem becomes. Lens or 'Pin Cushion' distortion is a

unique aberration, since there is no degradation in the sharpness and focus of the image merely the shape of the object is altered, resulting in the poor true scaled duplication of the original object being inspected (Liu, et al., 2000).

On completion of exposure to 96 thermal cycles, AMI imaging results were validated by micro-sectioning flip chips U23, U26, U31 and U34 for the two substrate thicknesses studied.

Although images for bump 107 are shown in Figure 3-30 to Figure 3-33, the remaining 108 bumps on the package were also sectioned through the interconnect mid-point. The complete data set including images has been archived electronically and is available on the electronic storage medium at the back of this thesis.

Samples were encased in epoxy resin to ensure planarity and prevent further joint damage occurring during the potting and grinding process. Potted samples were either cut or subjected to low deformation planar grinding using silicon-carbide papers of increasingly smaller grit sizes to reveal the solder bumps. The exposed bumps were polished using diamond or alumina particles of 6 to 0.05 microns in size and held in suspension to remove surface damage from the grinding process. Individual bumps were imaged using a Scanning Electron Microscope (SEM); an imaging scale was included allowing crack lengths to be manually measured if required. By sectioning the joint through the centre of the bump it is argued whether the diameter of the 2D crack plane is being measured. Consequently this value could then be verified with the crack plane diameter results obtained from the proposed non-destructive measurement method described in Chapter 5.

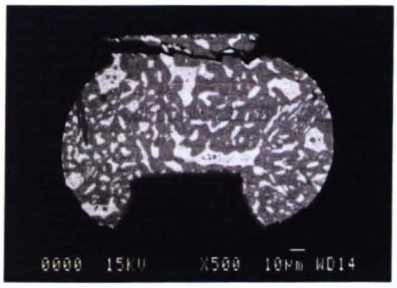


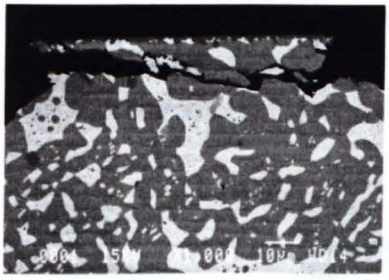
(a) U23 Bump 107 after 96 cycles (x500)

(b) U23 Bump 107 after 96 cycles (x1000)

Figure 3-30: Micro sections of flip chip U23, single side placement 0.8mm substrate

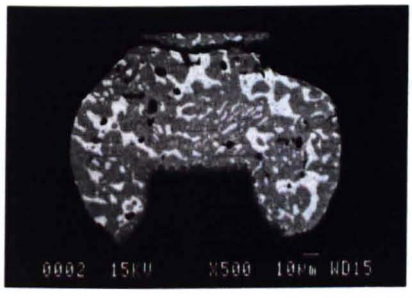
The mid grey areas in the images of Figure 3-30 to Figure 3-33 show the presence of larger coalesced tin-rich and lead-rich grains, the light areas being the lead rich grains. This is consistent with a solder joint which has been aged by thermo-cyclic applied stresses. Engelmaier postulates that grain structure is inherently unstable (Werner, 1997).

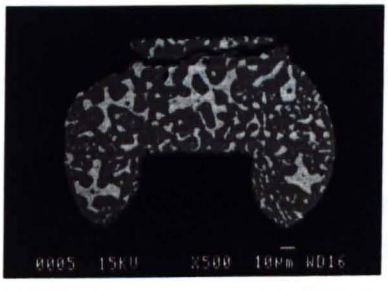




(a) U23 Bump 107 after 96 cycles (x500) **(b) U23 Bump 107 after 96 cycles (x1000)**

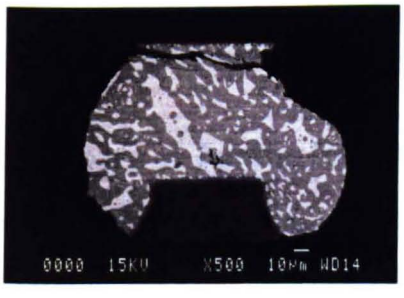
Figure 3-31: Microsection of flip chip U23, single side placement 1.6mm substrate

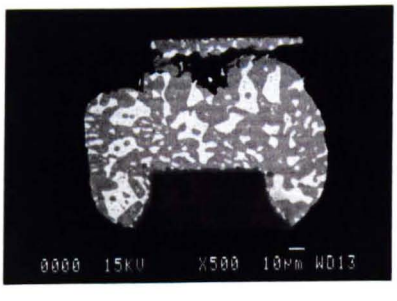




(a) U31 Bump 107 after 96 cycles (x500) **(b) U43 Bump 95 after 96 cycles (x500)**

Figure 3-32: Microsection of U31 and U43, mirrored placement 0.8mm substrate





(a) U31 Bump 107 after 96 cycles (x500) **(b) U43 Bump 95 after 96 cycles (x500)**

Figure 3-33: Microsection of U31 and U43, mirrored placement 1.6mm substrate

Grain size is known to increase over time as the grain structure reduces the internal energies of initial fine grain structure occurring when the joint was first produced. This growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. Grain growth is therefore an indication of the accumulated fatigue damage. At the grain boundaries there is an accumulation of lead oxide contaminants; increasing contaminant levels causing the grain boundaries to weaken.

Micro-voids occur in the grain boundaries when ~25% of the fatigue life has been consumed; these micro-voids grow into micro-cracks at ~40% fatigue life and in turn continue to grow and coalesce into macro-cracks leading to total fracture of the joint as illustrated in Figure 3-34.

Figure 3-34: Accumulation effects of fatigue damage in solder joints (Werner, 1997)

The dark specks in Figure 3-30 and Figure 3-32 are indicative on initial inspection of voiding within the solder joint. In this instance since the copper track at the bottom of the SEM image is also showing similar dark specks it would indicate that such artefacts in the image are likely to be 'pull-outs' and polish residue rather than pre-existing voids in the solder joint. This is a direct result of the grinding and polishing operation integral to the cross-sectioning process in which solder weakened through thermal cycling allows particles to become detached. Reviewing the sectioned joint images confirmed good reflow of the solder bump and that cracking was occurring within 16μm of the chip to bump interface.
Comparison of selected crack plane diameter measurements obtained from Ultrasound and SEM images are compared in Chapter 5 for selected solder bumps.

3.8 Summary of Testing Results

The experimental work confirmed the complementary nature of X-ray and AMI, showing that AMI, particularly C-SAM is a feasible approach by which to pursue through life monitoring and inspection of area array solder joints. One limitation identified being that solder joints cannot be inspected by "looking" through organic substrate PCB's with current ultrasound technologies.
Variation of the grey region residing typically in the middle of the AMI image of the solder joint is an important indicator of solder joint integrity and quality, measurable throughout accelerated testing. Undeniably this region grows in both size and intensity as the applied thermal cycles increases. This observation forms the basis of the novel method described in Chapter 5 in which the grey area or region of interest is simplified to a circular plane making it possible to estimate the number of thermal cycles experienced by the joint prior to failure. In addition it is suggested that the intensity level of the pixels also contains information and if calibrated would give an indication of possible z plane dimension or gap distance.

The X-ray results do not show any significant differences in the joint condition during the through life testing. However voiding has been seen in some of the joints which may be indicative of poorly manufactured interconnects. This may impact on the fatigue life response of the flip chips, and could be a potential source of cracking.

Micro-sectioning confirmed severe ageing had occurred in many of the solder joints from the highly accelerated test exposure. Moreover, the cracking seen in many of the solder joint AMI images were consistent with the physical state of the joints at the end of the 96 cycles.

In this chapter an understanding of reliability terminology, testing and physics of failure models have been developed. Furthermore X-ray and ultrasound non-destructive inspection techniques were reviewed, leading to the selection of C-SAM as the most feasible method through which images of hidden solder joints could be obtained.

The experimental work of this chapter provided imaging results from which the crack plane diameter and fatigue cycle information could be extracted using the methodology developed in Chapter 5. In the next chapter, FEA modelling case studies, replicating those of this chapter, are presented allowing both measured and simulation results to be compared.

Chapter 4

Solder Joint Failure Analysis Using Finite Element Modelling

4.1 Introduction

A number of circuit board and component configurations were analysed using a combination of a nonlinear two dimensional Finite Element Modelling (FEM) and Popelar's solder fatigue life model for flip chip on Organic Substrates (Popelar, 1998).

Although there are many different published models which could be applied to the performance analysis of solder interconnects, the modelling outlined is used extensively within Delphi due to its particularly good prediction accuracy. Accuracy has been achieved through diverse experimental studies of measured fatigue life of Flip Chips, BGA and CSP by varying component sizes deployed on ceramic and organic substrates, with and without underfill and by varying solder joint geometries. The data sets also represent varying thermal cycle profiles ranging from 0°C/100°C, 20 minute cycles, to -50°C/150°C, 80 minute cycles (Popelar, et al., 2000). The methodology of combining NDE examination and FEM employed in this thesis has enabled the effect on reliability of PCB floor plan layout, substrate thickness and mechanical circuit board constraints to be studied for the first time.

The numerical simulation method is essentially a two stage process in which a two dimensional plane strain FEM is created, and for specific material data supplied the model is solved using the ABAQUS FE software. This has enabled the creep energy dissipation (W_{cr}) in a specific solder joint volume to be obtained (Chengalva, et al., 2006).

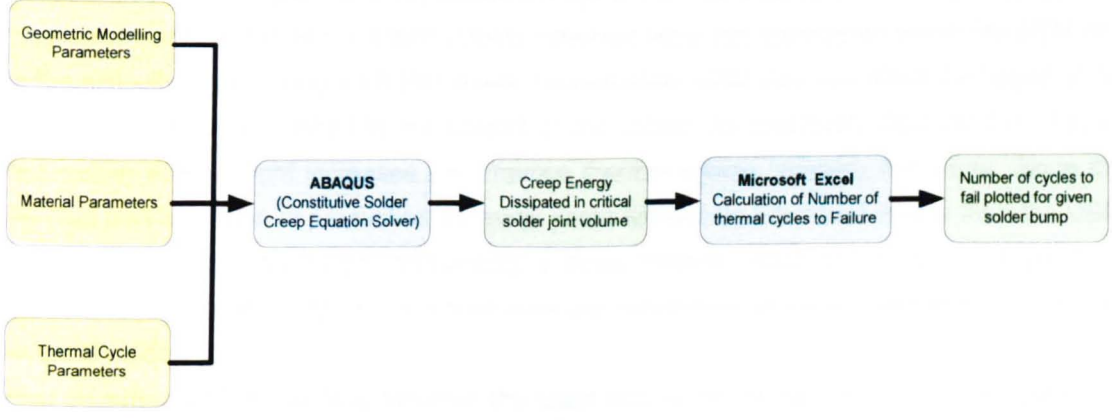


Figure 4-1: Block diagram showing the simulation process

Using the creep energy dissipation value for an individual solder joint obtained from the FEM simulation, and the rearrangement of equation 4 in Popelar's paper (Popelar, 1998) the numbers of cycles to failure are then calculated using Microsoft Excel. This is discussed in

section 4.3 of this chapter. The results for the individual solder bumps were then plotted showing the predicted cycles to fail for the system configuration under consideration.

4.2 Solder Joint Fatigue Model

Area array components are typically modelled and simulated using sub-modelling or reduced order modelling techniques in order to reduce complexity. This can include the use of symmetry or anti-symmetry. Natural lines of symmetry and anti-symmetry are used to allow a structure or system to be analysed by only modelling a portion of it. Symmetry in this context meaning a model is identical on either side of a dividing line or plane of symmetry. In the same way anti-symmetry indicates the loading of a model is oppositely balanced on either side of a dividing line or plane.

This technique reduces the total number of nodes and elements and therefore the size of the model which in turn can reduce analysis run time as well as demands on computer resource. Often this can be achieved by increasing the mesh density of the symmetrical model for greater accuracy and still have fewer elements than modelling the whole structure.

However the simplified arrangement and reduced number of interconnects of the flip chip package used in this research allowed a two dimensional strain model of the entire component inclusive of all interconnects to be used.

Heuristically the silicon to solder interface is the most common failure region for this package style. Moreover the bumps at the extreme corners are considered critical solder joints failing first due to their increased distance from the neutral point (DNP) of the rectangular package.

Simplified solder bump geometry, as illustrated in Figure 4-2, was used to build the bump interconnect characteristics in the FEM. The known failure region within the bump being described by the 'damage zone' (Z) shown in Figure 4-2. The substrate copper pad, its surface finish and Under Bump Metallisation (UBM) materials were not considered within the FEM due to the difficulty of modelling such thin layers. Nevertheless UBM size can affect the height of the solder bump through controlling the spread of the solder. As previously discussed in chapter two, solder bump height increases can improve thermal cycling reliability behaviour. Since the flip chip part has been in production for many years without reported field issues then the UBM materials developed by Delphi comprising a three material stack of Al/NiV/Cu (Aluminium, Nickel- Vanadium and Copper) and their size are considered already optimised to give high levels of reliability.

Also occurring at the interface between the UBM and solder bump interface, lying within the damage zone is a diffused zone comprising of intermetallic compounds (IMC). The precise material characteristic for the intermetallic compound (IMC) layer are not generally known since they are formed during the solder liquid to solid phase change and is a complex mixture of two or more elements from the substrate and solder ball which forms a new structure in a stoichiometric ratio (Hwang, 1992). It is widely acknowledged that solder joint strength and fatigue life are reduced by excess intermetallics or having a thicker IMC region at the joint

interfaces. In a controlled manufacturing process the intermetallic layer thickness will be minimised. Therefore the FEM considers the intermetallic layer to be thin relative to the solder bump and Silicon, so it is considered to have little or no effect on the simulation results.

Popelar (Popelar, et al., 2000) restates that all materials comprising the simplified bump geometry model are assumed to behave in a linear manner with the exception of the solder. As such, only the elastic modulus, coefficient of thermal expansion (CTE) and Poisson's ratio are supplied as a function of temperature.

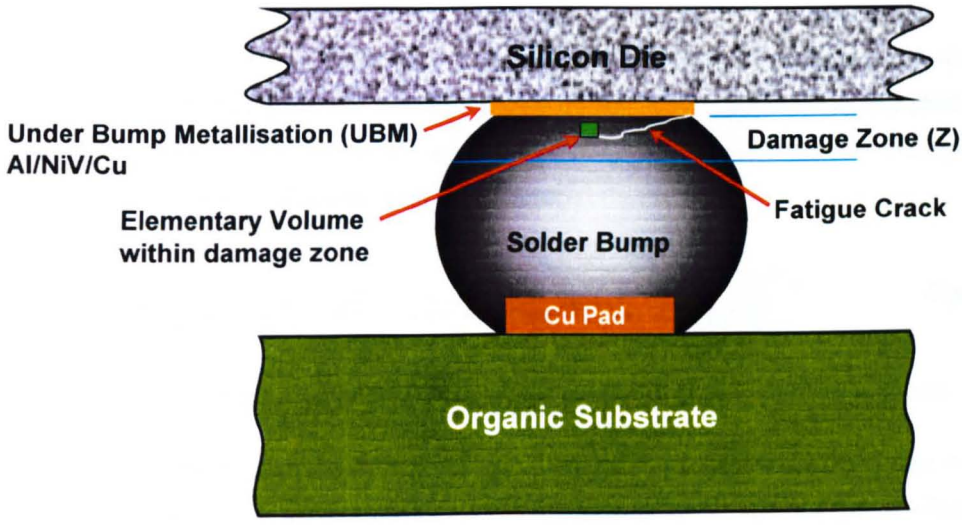


Figure 4-2: Pictorial representation of flip chip interconnection

Since the solder is considered non-linear an additional Creep Constitutive Equation derived from Wong et al (Wong, et al., 1988) is required which correlates the amount of steady-state creep strain energy $d\varepsilon_{cr}/dt$ of the solder with temperature and applied stress load (σ).

From the work of Wong (Wong, et al., 1988) and Popelar (Popelar, et al., 2000) this equation takes the form:-

$$\frac{d\varepsilon_{cr}}{dt} = e^{\left[-\frac{Q}{kT}\right]}\left\{B_{GBS}\left[\frac{\sigma}{E}\right]^{N_{GBS}} + B_{MC}\left[\frac{\sigma}{E}\right]^{N_{MC}}\right\} \qquad \textit{Equation 4-1}$$

Where:

E is the Elastic Modulus

$e^{\left[-\frac{Q}{kT}\right]}$ is termed the diffusivity function (D) used to normalise the steady state strain rate.

Q is the relevant activation energy for creep.

k is Boltzmann's constant and T is absolute temperature.

B and N are material constants for the solder.

σ is the applied load stress.

Subscript GBS denotes grain boundary sliding occurring in the solder at combinations of low stress and high temperature.

Subscript MC denotes an added component accounting for creep occurring in the material matrix due to high stress and low temperature.

Note that Q, B_{GBS}, B_{MC}, N_{GBS}, and N_{MC} are solder alloy dependant and need to be determined experimentally from the steady-state creep data for tin lead eutectic solders. In this case the characteristics used were from Popelar's Creep Characterisation of Solder Alloys work (Popelar, 1997).

The applied load stress (σ) of *Equation 4-1* is defined as the *Von Mises* equivalent stress, which is a combination of three principle stresses acting on any single point within the joint in the x, y and z axis. The equivalent creep strain is found from the normal and shear components of creep strain defined by Popelar (Popelar, et al., 2000) as:-

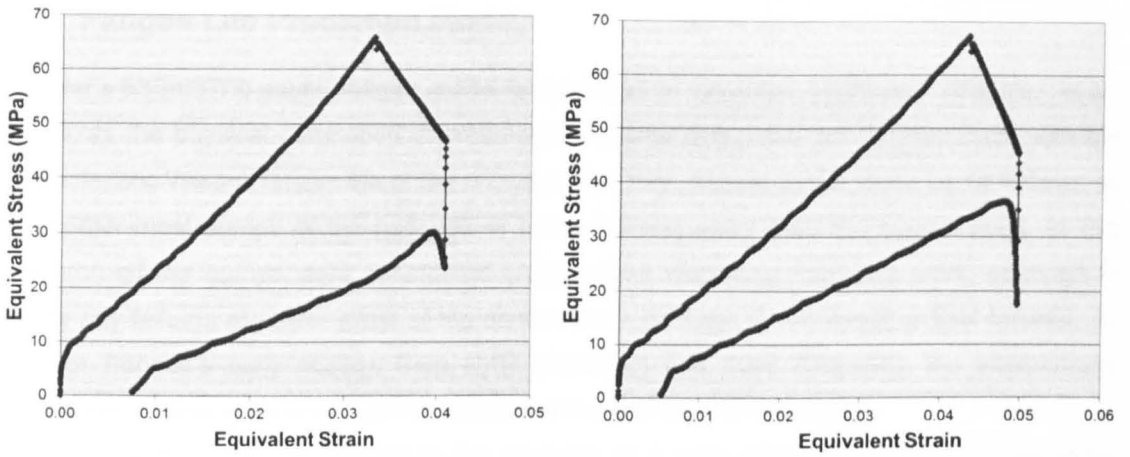
$$\varepsilon_{cr} = \left\{(2/3)\left(\varepsilon_x^2 + \varepsilon_y^2 + \varepsilon_z^2 + (1/2)\left(\gamma_{xy}^2 + \gamma_{xz}^2 + \gamma_{yz}^2\right)\right)\right\}^{1/2} \qquad \textit{Equation 4-2}$$

Where ε's and γ's denote normal and shear components of creep strain respectively.

No plasticity component has been included in *Equation 4-1* as it is assumed that the thermal cycles are slow enough to allow sufficient time for creep to occur, although in practice this may not happen.

For each FEM simulation scenario performed, a creep hysteresis curve as described previously in Section 3.3.2 is generated for a single thermal cycle representing the average stress and strain within the damage zone (Z) of Figure 4-2. Popelar (Popelar, 1998) points out that this reduces the dependence of the results on the mesh density of the finite element model. The thermal cycle profile in this instance being derived from the thermal profiling experiments performed in Section 3.5.1.1.

Through analysing level one and level two interconnect failures of area array parts, it has been determined that creep fatigue solder joint failure occurs predominantly at the solder to silicon interface, within a 12.7microns (0.5mil) region termed the damage zone as shown in Figure 4-2.



a) 0.8mm Substrate **b) 1.6mm Substrate**

Figure 4-3: Flip chip hysteresis curves calculated for organic substrates. (single thermal cycle) (Popelar – Braden personal communications)

Since the area within the hysteresis curve defines the average cumulative creep energy dissipation per thermal cycle in the damage zone (Z) of figure 4-2. Then the creep damage per thermal cycle (W_{cr}) can be found through integration:-

$$W_{cr} = \frac{1}{V_Z}\int_Z \int_t^{t+T} \sigma_{eq} d\dot{\varepsilon}_{cr} dt dV \qquad \textit{Equation 4-3}$$

Where:-

W_{cr} Creep damage per thermal cycle in mJ/mm^3 (1mJ/mm^3 = 1MPa).

σ_{eq} in this context is von Mises stress.

$\dot{\varepsilon}_{cr}$ Creep strain energy.

dV is an elementary volume within the damage zone, depicted in figure 4-2 by the green square.

T denotes time period for accumulation of creep energy.

V_z is volume of the damage zone.

The resulting creep damage per thermal cycle (W_{CR}) value can then be input into Popelar's solder fatigue equation defined in *Equation 4-4* and used to predict fatigue life. It should be noted that the hysteresis curves of figure 4-3 in conjunction with the results from physical testing suggest that the experimental work provided a significant over stress condition. This resulted in the number of cycles to failure being extremely small (<100 cycles) which is not consistent with packages deployed in the field that typically show the number of cycles to failure to be >1500.

4.3 Fatigue Life Prediction Model

Popelar's 63Sn/37Pb solder fatigue model is described in (Popelar, 1998) and (Popelar, et al., 2000), as the physical correlation of creep strain energy dissipated per thermal cycle with the characteristic Weibull fatigue life of the critical solder joint. Critical solder joints being defined as the corner-most bumps of the package or those furthest away from the neutral point. In this research all the bumps were considered critical when deploying Popelar's work, although in reality any failures of solder joints at the corner of the package would result in field failures. In both of Popelar's early studies from 1997 (Ceramic) and 1998 (Organic), the interconnect fatigue life models were developed for both ceramic and organic substrates.

The models may also be applied to the analysis of a wide variety of area array packages including flip chip, BGA and CSP since the experimentally measured fatigue life data was recorded for both ceramic and organic substrates. For each substrate type consideration was given to packages that were underfilled and non-underfilled as well as the geometries of the solder joints. Moreover validation of the models over several thermal profile ranges from 0°C to 100°C, using 20 minute cycles to -50°C to 150°C for an 80 minute cycle results in the models being a characteristic of the solder itself and independent of solder joint geometry.

This makes the power law model of *Equation 4-4* for organic substrates particularly flexible and useful in the proposed deployment within this area of research.

An estimate of solder joint fatigue life in terms of the number of thermal cycles to failure was determined for each of the individual solder bumps on the flip-chip components for the specified analysis scenarios. The cycles to failure were calculated through the transposition of the creep fatigue correlation model given for a 63Sn/37Pb solder system subjected to thermal cycling by Popelar (Popelar, 1998).

$$W_{cr} = 3.86N_f^{-0.495} \qquad \textbf{Equation 4-4}$$

Transposing *Equation 4-4* results in the cycles to failure.

$$N_f = 10^{\left[\frac{\log_{10}(W_{cr}/3.86)}{-0.495}\right]} \qquad \textbf{Equation 4-5}$$

Where W_{cr} is the creep energy dissipated per thermal cycle mJ/mm^3 (1mJ/mm^3 = 1MPa) and N_f is the Weibull characteristic life in which 63.2% of the samples have failed in the test population. It should be noted that in the Popelar 1997 paper (Popelar, 1997) *Equation 4-4* is also written as:-

$$W_{cr} = 560N_f^{-0.495} \qquad \textbf{Equation 4-6}$$

This is merely a units issue as *equation 4-6* considers the creep energy dissipated per thermal cycle (W_{cr}) in pounds per square inch (psi) not MPa.

4.4 Boundary and Model Constraints

There are a number of constraints which must be taken into account when considering the accuracy of the fatigue life predictions. FEM result accuracy is dependent upon the precision of the material and, dimensional properties supplied for the studied components and test board configurations. In some of the simulations the data for the material properties were not available and so were based on similar analysis previously performed within Delphi and documented in Appendix B. For the physical descriptions of components and interconnections of the test CBA the nominal or average dimensions were utilised in the simulation.

Materials making up the test board and components are expected to behave linearly in response to temperature, the exception being the solder interconnect. As such the modulus of elasticity, CTE and Poisson's ratio which respond directly with temperature were used as inputs for the FEM. Since the reliability of the solder bump interconnect is dependent on non-linear time dependent creep behaviour of bump geometry and material properties to the applied thermal load profile the uniaxial constitutive equation outlined in Section 4.2 is used in addition to the linear response elements. The analysis presumed the manufacturing quality of the solder joints on the CBA was good, and conforming to appropriate manufacturing standards. Primavera documents that joint quality provides a more critical influence on reliability as joint dimensions reduce (Primavera, 1999). The CBA used in the experimental work was not conformally coated, and area array components were not underfilled.

Furthermore simulations only considered solder joint failure mechanisms resulting from the accumulated creep damage caused through Coefficient of Thermal Expansion (CTE) mismatch between flip chip components and the organic CBA. A simulation thermal cycle describing the maximum temperature for powered devices in the field is described in Figure 4-4. The cycle comprises a 30 minute dwell at -40°C followed by a 30 minute dwell at +132°C. Transition rate between thermal extremes is 69°C/minute (172°C thermal change over a 2.5 minute interval).

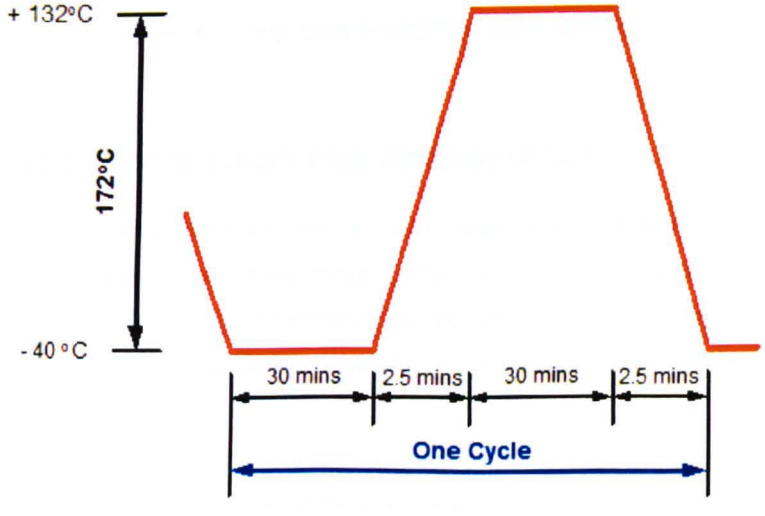


Figure 4-4: Simulation Thermal Profile

4.5 Flip Chip Modelling and Simulation Case Studies

Six modelling and simulation case studies were documented and supplied to the Delphi Mechanical Analysis and Simulation group in Poland for coding, and execution. Each study investigated the individual behaviour of solder joints on the flip chip packages whilst testing the hypothesis that reliability of CBA's is influenced by placement location on the PCB (floor plan layout), PCB thickness, and physical constraints placed on the PCB. Physical constraints considered in this study were due to four mounting screws placed at the corner of the PCB.
The flip chip case studies are documented in Table 4-1.

Modelling Case Study	*Detail of Case Study*
M1	Reliability and fatigue cycles simulated for single side placed 109 bump flip-chip package mounted on 0.8mm and 1.6mm FR-4 substrate.
M2	Reliability and fatigue cycles calculated for individual flip chips mounted either side of FR-4 substrate in a 'Mirrored' configuration. Simulations run for 0.8mm and 1.6mm FR-4 substrate cases.
M3	Global reliability and fatigue cycles simulated for individual flip chips mounted either side of FR-4 substrate in a 'Mirrored' configuration. Substrate thickness, additional components on the floor plan and PCB corner constraint points included in the model and simulation.
M4	0.8mm vs. 1.6mm substrate thickness - Comparison of relative reliability single side simulation for each substrate thickness.
M5	Single vs. Mirrored - Comparison of relative reliability single side simulation case M1 with relative reliability of case M2.
M6	Single and Mirrored vs. Global - Comparison of relative reliability single side simulation case M1 and M2 with relative reliability of case M3.

Table 4-1: Flip chip modelling case studies

4.5.1 Single component, single side placement (M1)

For the case study illustrated in Figure 4-5, a widely used and verified modelling technique is used to establish the base line interconnect performance. No consideration was given to influences provided by surrounding components on the test board floor plan layout or substrate constraints. This is a typical way in which reliability of components and packaging interconnect performance are studied.
Over a single thermal cycle, both the strain energy and subsequent cycles to failure were calculated for all SnPb solder bumps on individual packages placed singly onto either 0.8mm or 1.6mm organic substrate.

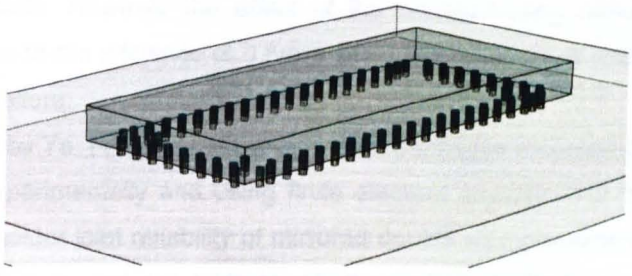


Figure 4-5: Single side, single chip placement model

This provided a means of validating the through life measurement technique whilst testing the hypothesis that substrate thickness can influence package reliability. Earlier work by Primavera (Primavera, 2004) found that when comparing 0.4mm and 1.57mm thick PCB's, solder joint stresses in CSP packages are reduced as board thickness and stiffness decrease. In this work Primavera found that fatigue life performance could be increased by a factor of 2.

4.5.2 Flip chip components mirrored on a substrate (M2)

For this case study the flip chip components are placed on either side of the substrate so bumps are aligned in a 'mirrored' fashion as illustrated in Figure 4-6. This configuration can occur frequently in designs where board real estate is small and microprocessor-based digital circuitry is deployed. An important design requirement in such applications is to interconnect silicon using the shortest path lengths to minimise impedance.

A typical example would be mixed memory storage (RAM and EEPROM) where address and data bus lines are shared. Since the packages are mounted either side of the substrate it is expected that the influence of CTE mismatch will impact significantly on the reliability of the joint performance.

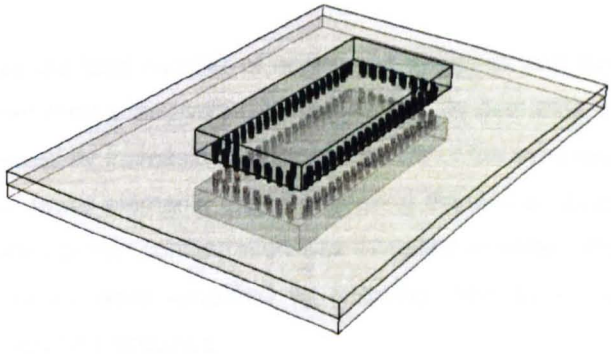


Figure 4-6: Single chips placed either side of substrate

Over a single thermal cycle, both the strain energy and subsequent cycles to failure were calculated for all SnPb solder bumps on individual packages placed singly onto 0.8mm and 1.6mm organic substrate respectively. In the same way as case study M1 no consideration was

given to any influence provided by surrounding components on the test board floor plan layout or substrate constraints. However the effect of the corresponding mirrored component was considered in addition to the influence of 0.8mm and 1.6mm thickness substrates on the overall number of cycles to failure.

In studies performed by Ye (Ye, et al., 2007) on BGA packages mounted on organic substrates it was found both experimentally and using finite element analysis that there was up to 48% reduction in tin lead solder joint reliability of mirrored double side placement compared to single sided assembly. The study did not address whether substrate thickness or rigidity played a significant part in the reliability reduction. The case study (M2) undertaken in this work looked at comparing the modelled and through life measurement data for mirrored packages placed on different substrate thicknesses.

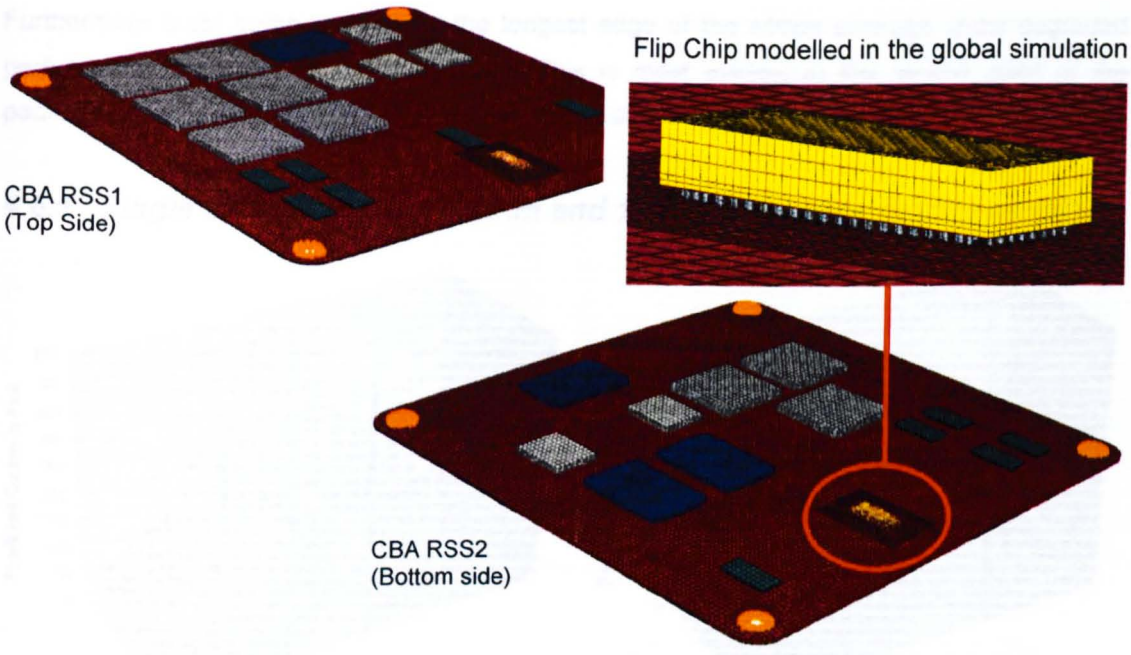
4.5.3 Mirrored packages modelled using a global PCB approach (M3)

Case study M3 was developed to test the notion that component location on a CBA, in combination with other factors such as adjacent components and substrate constraints, influence the overall reliability of solder joints on area array package. Considering that in some automotive applications component counts can be higher than 2000, it is understandable that this type of simulation is not normally performed due to the complexity of the overall FE model, the hardware capability and time required to run the simulation.

The relative simplicity of the test CBA in conjunction with utilising sub-modelling techniques to speed up calculation times, made it possible to perform the simulation analysis on a HP xw4600 workstation comprising of a single processor containing 4 cores and 16GB memory. For this case study the calculation time was typically 48 hours.

Sub-modelling or reduced order modelling describes various techniques applied to an FE model of a complex system in order to reduce its complexity. This can include the use of symmetry or anti-symmetry.

This technique reduces the total number of nodes and elements and therefore the size of the model which in turn can reduce analysis run time as well as demands on computer resource. Often this can be achieved by increasing the mesh density of the symmetrical model for greater accuracy and still have fewer elements than if modelling the whole structure. In this study the mirrored or back to back flip chip configuration was modelled in detail, whilst other components on the printed circuit board were simplified by reducing them to simple cubic shapes with appropriate material properties assigned.



Note: CBA RSS2 illustration is viewed from component side after being flipped through 180degree.

Figure 4-7: Modelling of CBA using global approach.

In addition to modelling the influence of surrounding components on the dynamics of the CBA, the model also included constraints on the PCB introduced by fixing it at the four corner screw holes coloured orange in Figure 4-7.

In this simplified model the fixing of boundary conditions in the simulation could over constrain the PCB. Further physical experimental work is needed to assess the impact of CTE movement of the fixture to which the PCB was screwed and tolerance of screw diameter to hole in the PCB to ensure the model reflects reality.

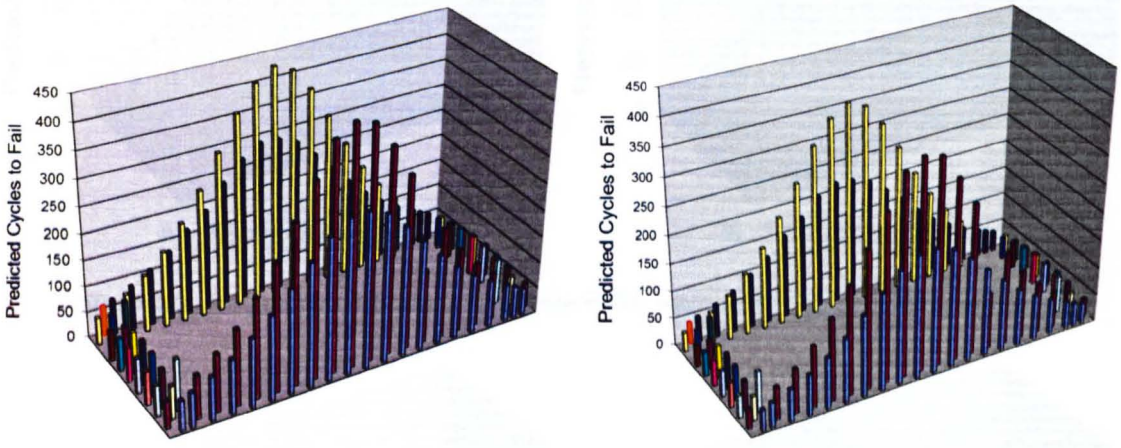
4.6 Simulation Results

In the following series of simulation results for case studies M1 to M6, the predicted fatigue failure cycles for each individual solder bump on the flip chip package were calculated and displayed in a 3D graphical format representative of the silicon package.

For all graphs, bump number one is highlighted in red and located in the upper left or bottom left of the graph in the case of mirrored devices. In all simulation studies the simulation graphs show consistency with the theory that critical solder joints at the corner of the package and furthest from the neutral point of the longest edge of the package are displaying the worst levels of reliability performance and therefore least number of cycles prior to failure.

Furthermore outer bump rows along the longest edge of the silicon package show degraded performance compared to the inner rows. This is most evident at the neutral point of the package which is the centreline of the longest edge of the rectangular package.

4.6.1 Single side placement 0.8mm and 1.6mm substrate thickness (M1)



a) 0.8mm substrate **b) 1.6mm substrate**

Figure 4-8: Graphical results for 0.8mm and 1.6mm PCB, U23 single side placement

Figure 4-8 shows critical solder joints at the package corners (Bumps 1,38,39,54,55,92,93 and 109) furthest from the package neutral point and along the shortest edge of the package fail on average at 52 cycles and 35 cycles in the case of 0.8mm and 1.6mm substrates respectively. This translates to a 33% drop in reliability performance in the case of 1.6mm substrates.
At the neutral point this translates to a 17.5% reduction in reliability cycles for the inner row of bumps and 24.3% for the outer row for 1.6mm substrate case. These values vary as the bumps move from the neutral point out to the critical solder joints at the corners of the package. This simulation case study clearly shows that solder joint reliability is affected by substrate thickness. Consistent with published literature by Ye (Ye, et al., 2007) and Primavera (Primavera, et al., 2004) it can generally be confirmed that reducing board thickness and overall stiffness increase the fatigue life or survivability of solder joints.

4.6.2 'Mirrored' placement 0.8mm and 1.6mm substrate thickness (M2)

The simulations in this study only consider the case of components placed back to back in a mirrored fashion either side of the substrate with no influences from surrounding constraint points or components.

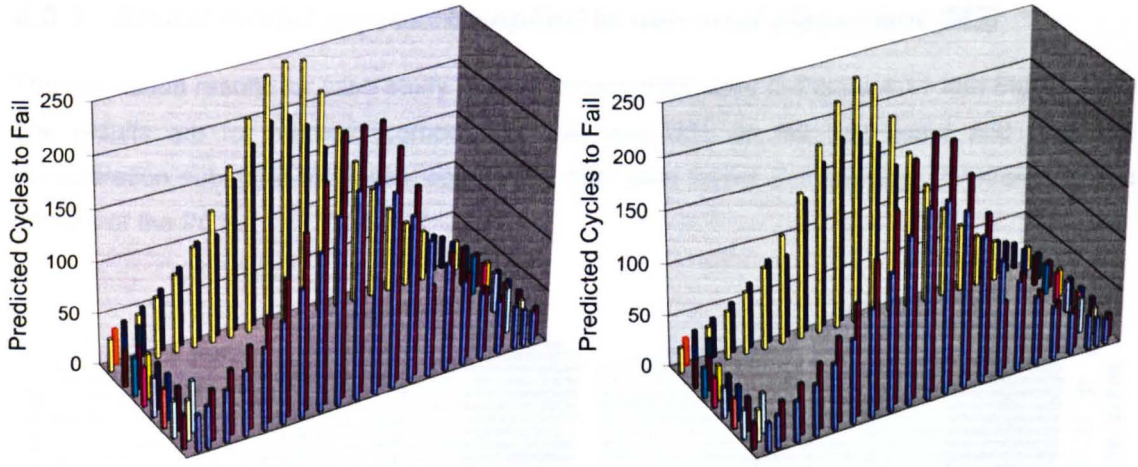


Figure 4-9: Results for 0.8mm and 1.6mm PCB, mirrored, U31 topside placement

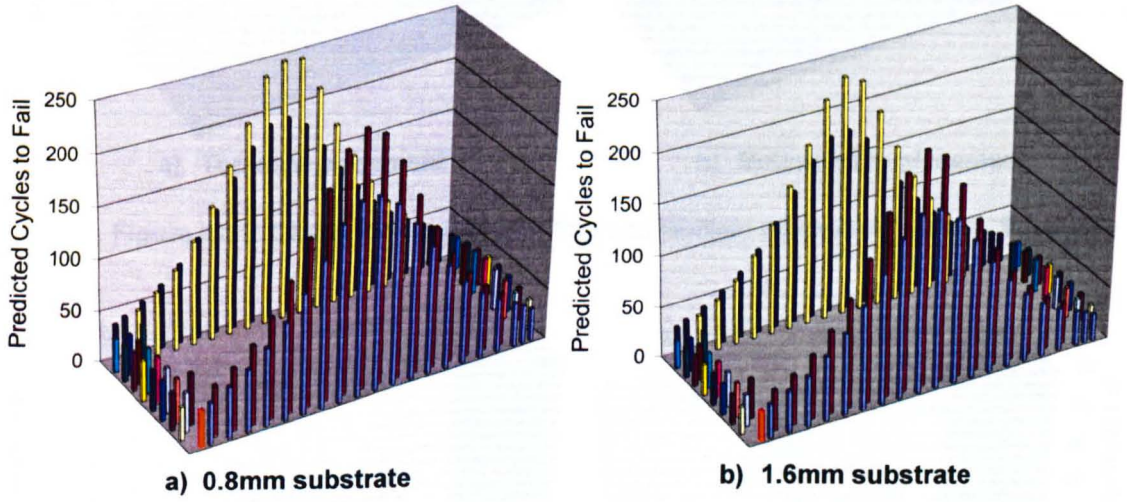


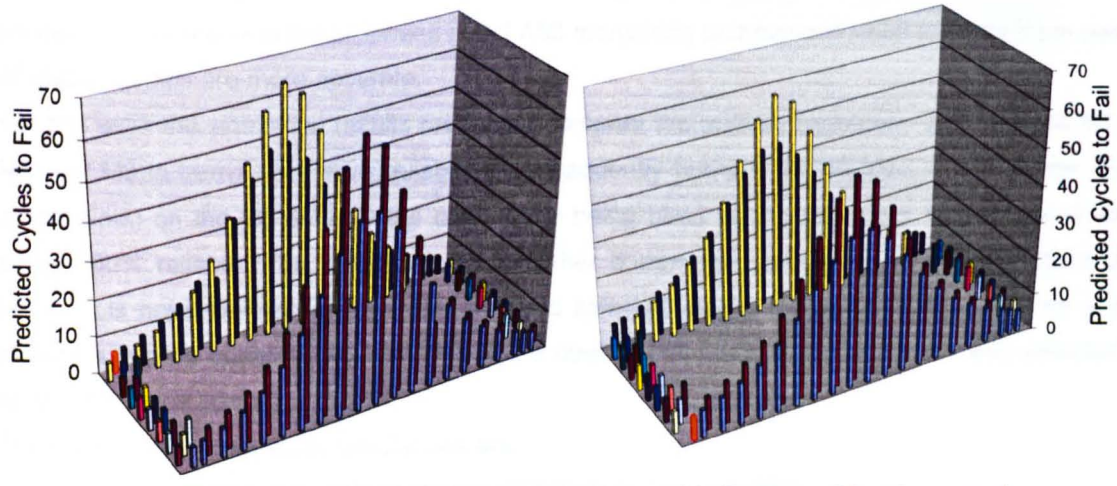
Figure 4-10: Results for 0.8mm and 1.6mm PCB, mirrored, U34 bottom side placement

The simulation results for case study M2 in Figure 4-9 and Figure 4-10 show conclusively that in both cases of substrate thickness, mirrored part placement reduces reliability performance when compared to that of single side placed components. Considering just the inner row neutral point bumps and critical solder joints at the corners for the package this can be as much as 29.4% and 34.7% respectively. In the same way as the M1 case study of section 4.6.1, components on the 1.6mm substrate have reduced reliability performance over the thinner 0.8mm substrate.

Simulation results for this case study also show little difference in reliability performance between top and bottom side located flip chip components. This is consistent across the two substrate thicknesses which suggest that mirrored double-side layout of components has significantly more impact on reliability performance than substrate thickness. This is consistent with published findings of Ye (Ye, et al., 2007) for mirrored BGA devices mounted on organic substrates.

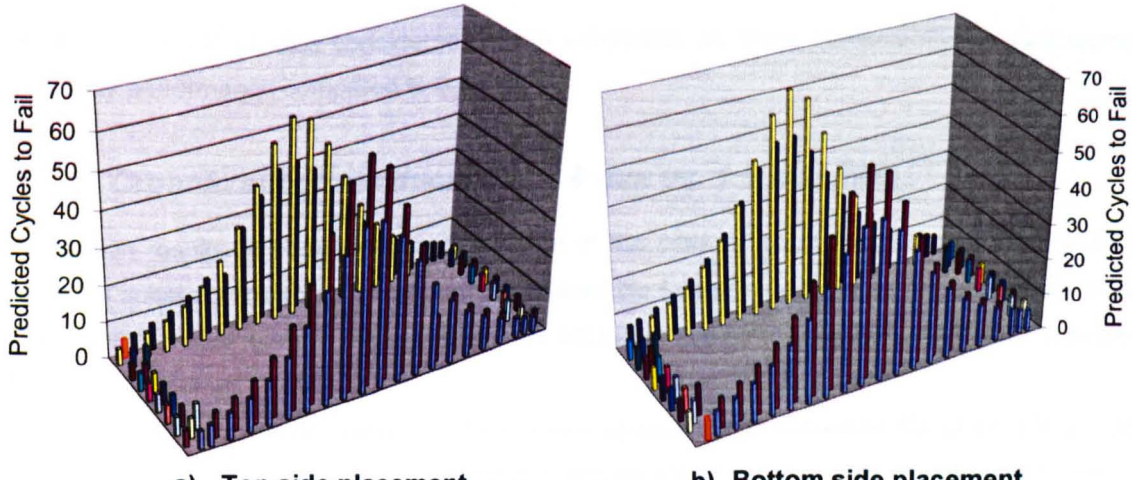
4.6.3 Global model approach applied to mirrored placement (M3)

The simulation results for case study M3 are shown graphically in Figure 4-11 and Figure 4-12. The results are for mirrored components U23 and U31 on the test board and take into consideration substrate thickness, component floor plan layout and physical constraints at the corners of the PCB.



a) Top side placement **b) Bottom side placement**

Figure 4-11: Global Model Results, Top and Bottom placement, 0.8mm Substrate



a) Top side placement **b) Bottom side placement**

Figure 4-12: Global Model Results, Top and Bottom placement, 1.6mm Substrate

On inspection of Figure 4-11 and Figure 4-12 it could be argued there are small differences between top and bottom side placement results around the neutral point axis of the package. This requires further investigation as in reality a 10 fatigue cycle difference is not considered to have a significant impact on overall joint reliability. More importantly for the critical solder joints at the corners of the package there is extremely good correlation between the top and bottom placed components in both the 0.8mm and 1.6mm substrate cases.

4.7 Inter-case Study Comparisons

The simulation results of Section 4.6 allow correlation comparisons to be made with fatigue cycles derived directly from AMI measurements, providing proof of concept for the novel through life monitoring technique proposed.

Inter-case study comparisons seek to provide incremental understanding of the impact on solder joint reliability performance when considering floor plan layouts in the simulation FEA models. In this scenario the proposed novel AMI monitoring technique is used to verify if the use of global models are more accurate.

For this work the simulation results presented compare the primary simulation case studies M1, M2 and M3 in terms of relative reliability. Consequently bump 1 (highlighted in red on the 3D graph plots) on the flip chip for the case study being used as the reference is considered as being 100% reliable. The reliabilities for all other bumps are calculated with respect to that bump. It is not important which solder bump is selected as the reference bump since we are making a relative comparison. However, in the case of this study bump number 1 was selected as the reference bump.

The comparative case study simulations are:

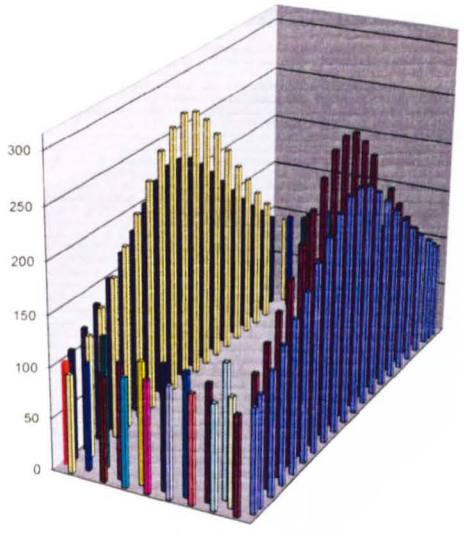
- Organic substrate thickness (0.8 mm vs. 1.6 mm) (M4)
- Single side single component vs. mirrored (back to back) placement (M5)
- Single and Back to back configuration vs. global model approach (M6)

Both M5 and M6 studies considered 1.6mm substrates as these consistently showed worse reliability performance compared to 0.8mm.

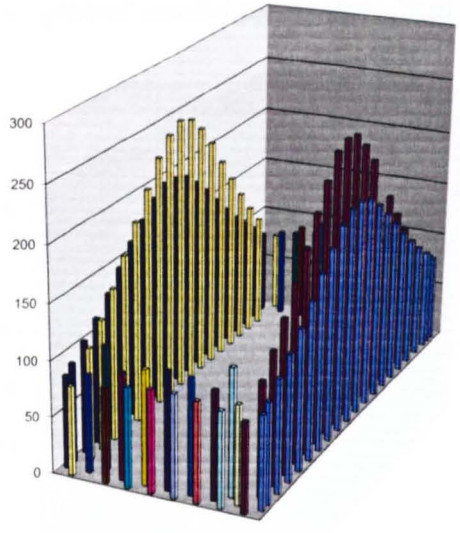
4.7.1 Organic substrate thickness 0.8 mm vs. 1.6 mm (M4)

Simulation results of Figure 4-13 indicate that in the case of circuit board assemblies (CBA) having a substrate thickness of 1.6 mm the relative life expectancy dropped on average by 14% (18% at the critical joints in the corners of the package) compared to CBA's having a substrate thickness of 0.8mm.

This is not an unexpected result as there many references in published literature citing that increased board thickness and overall stiffness reduce solder joint reliability in area array parts.



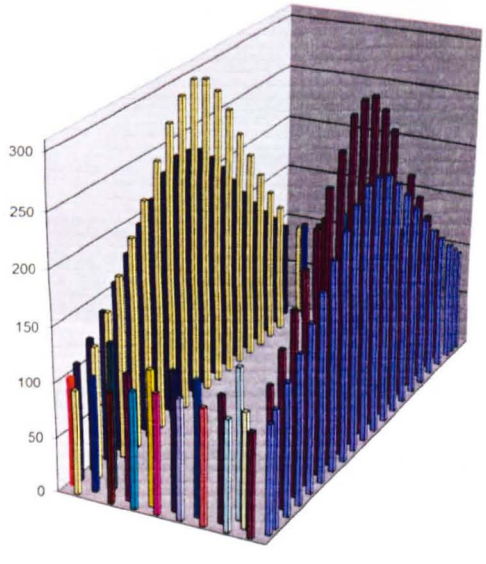
(a) 0.8mm substrate



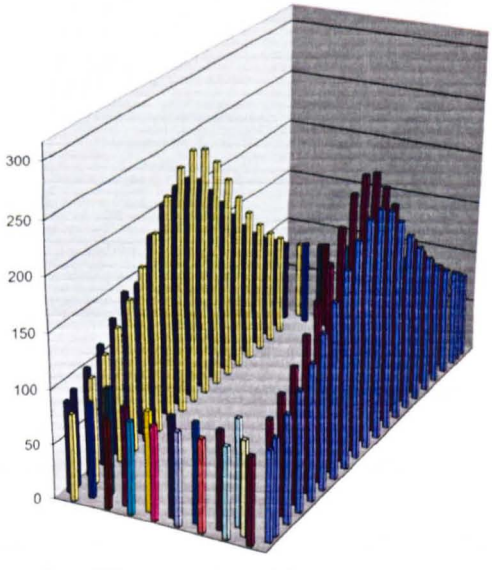
(b) 1.6mm substrate resultant plot

Figure 4-13: Graphical results comparing 0.8mm and 1.6mm PCB, single side placement

4.7.2 Single side component vs. mirrored configuration (M5)



(a) Single topside component placement

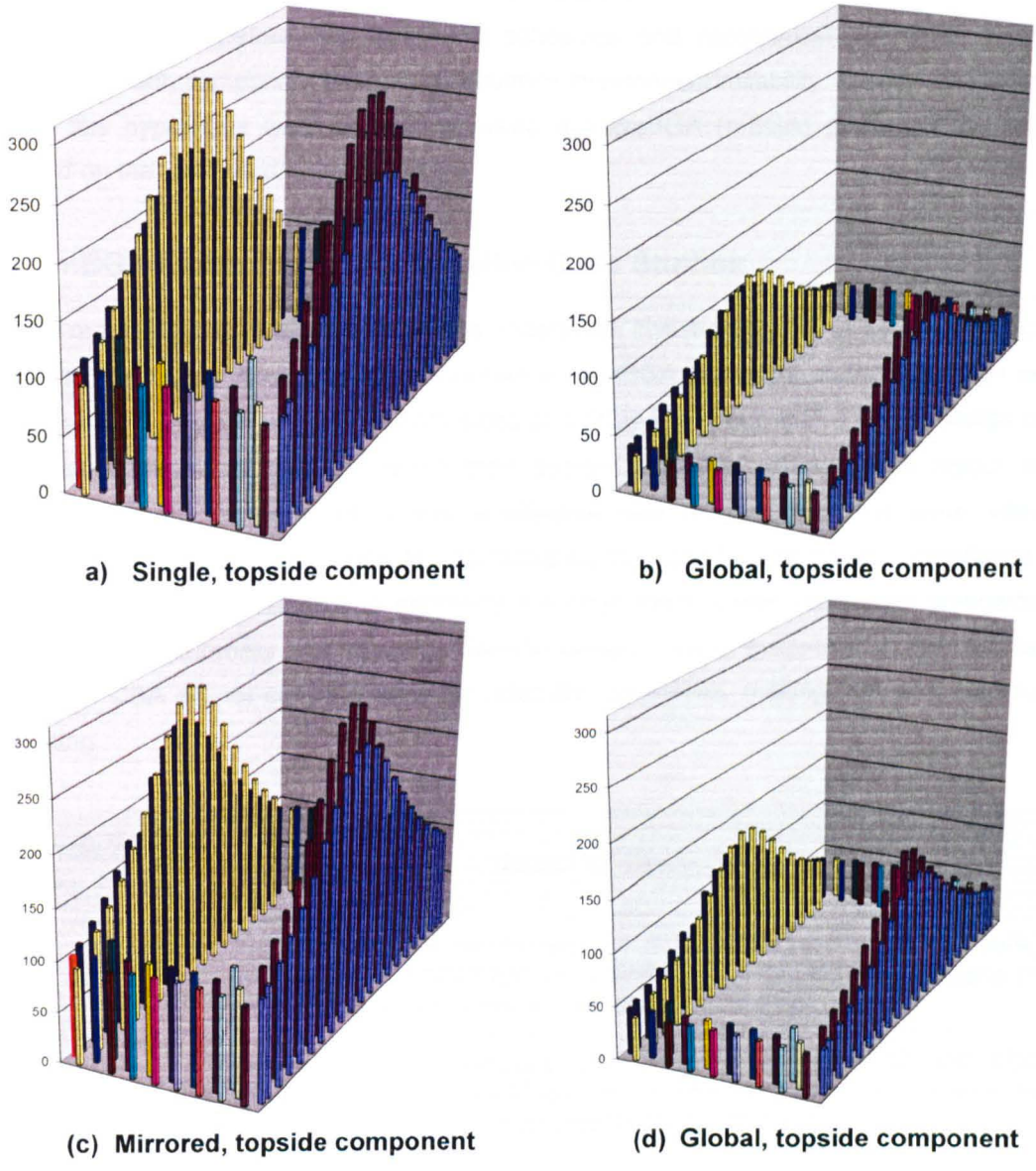


(b) Mirrored, topside component

Figure 4-14: Graphical results comparing 1.6mm substrate single side placement verses mirrored

In this relative reliability scenario, the bump failure distribution is consistent with previous simulation results. However when comparing mirrored or back to back configuration with a single side placed package there is on average a 20% reduction in relative life expectancy of solder joints observed.

4.7.3 Single & mirrored configuration vs. global model approach (M6)



a) Single, topside component

b) Global, topside component

c) Mirrored, topside component

d) Global, topside component

Figure 4-15: Global relative reliability comparisons for 1.6mm substrate

In the 'global model approach' where component interactions are considered in addition to fixing corners of the PCB substrate the simulations show relative life expectancy to drop on average by 64% and 56% when compared to single side flip-chip placement and for packages placed on either side of the substrate in a mirrored fashion respectively.

Undeniably this would suggest that when predicting joint performance for a particular package the entire CBA design and interaction with its case must be considered for the results of modelling to come close to matching the performance of the packages in their field application or when subjected to test during product validation. Interconnect reliability tests conducted within Delphi have shown that when CBA's are subjected to thermal cycling tests at board level,

the observed reliability shows improved performance compared to CBA's enclosed within an aluminium case and subjected to the same thermal profile.

It is suggested therefore that assembly adhesives and mechanical constraint points in combination with component floor plans influence interconnect reliability. Further investigations testing this hypothesis were undertaken using a microBGA (mBGA) packaged device also installed on the test board.

4.8 mBGA Modelling and Simulation Case Studies

Further modelling and simulation work was undertaken investigating the influence of floor plan layout on the interconnect reliability performance of mBGA packaged parts. Floor plan layout determines the location of parts on both sides of a PCB taking into board layout design rules. PCB layout engineers consider within their design standards an optimised layout which considers thermal management to ensure effective heat removal from the parts, vibration response, optimised electrical and EMC performance through short tracks, low impedance and electrical isolation. Pad sizes and geometry are often fixed, based on design standards for meeting manufacturability and reliability. Specific design rules or guidelines at the PCB layout stage of a CBA do not currently exist for reliability robustness, making this work particularly interesting.

Modelling Case Study	***Detail of Case Study***
M7	Relative reliability comparison for single side placed 48 Ball mBGA, 0.75mm pitch, Sn63/Pb37 on 0.8mm FR4 substrate. No influence from surrounding components or constraints on the floor plan.
M8	Relative reliability comparison for single side placed 48 Ball mBGA, 0.75mm pitch, Sn63/Pb37 on 1.6mm FR4 substrate. No influence from surrounding components or constraints on the floor plan.
M9	Relative reliability comparison of 48 Ball mBGA, 0.75mm pitch Sn63/Pb37 single vs. back to back (mirrored) configuration placement on 0.8mm FR4 substrate. No influence from surrounding components or constraints on the floor plan.
M10	Relative reliability comparison of 48 Ball mBGA, 0.75mm pitch Sn63/Pb37 single vs. back to back (mirrored) configuration placement on 1.6mm FR4 substrate. No influence from surrounding components or constraints on the floor plan.
M11	Relative reliability comparison of PCB thickness on 48 Ball mBGA, 0.75mm pitch Sn63/Pb37 single side placement 0.8mm vs. 1.6mm FR4 substrate. No influence from surrounding components or constraints on the floor plan.

Table 4-2: mBGA Modelling case studies

Results were reported at ESTC 2010, Berlin (Braden, et al., 2010). The FEA model stated in *Equation 4-1* of this thesis was used to calculate the creep strain energy for individual solder balls. Boundary and model constraint conditions were changed to reflect the materials and configuration of the mBGA package installed on the test board described in Chapter 3. Five modelling scenarios were simulated, M7 to M11 and are described in Table 4-2, the flip chip thermal cycle profile was used in this investigation.

Because of the symmetry of the solder interconnects on the mBGA package, the package was divided into four quadrants; with a single quadrant being represented by a 4x3 finite element computational mesh. This serves to reduce both the computation power and time required to run the simulation. The overall device joint behaviour was then reconstructed in Microsoft Excel to produce the surface plots of Figure 4-16 to Figure 4-20.

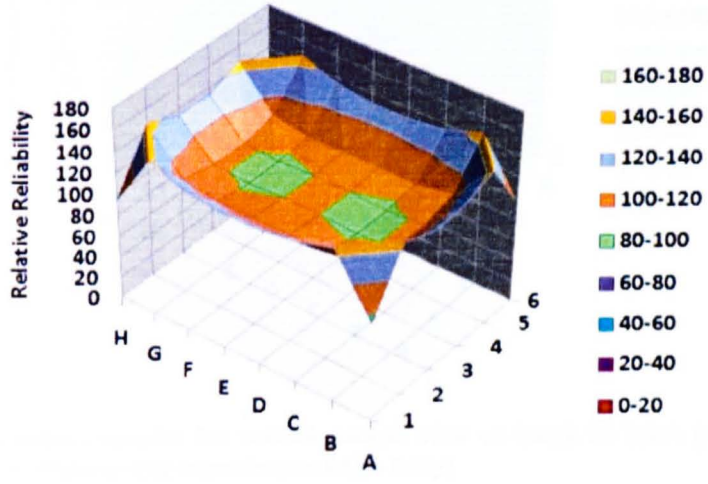


Figure 4-16: Simulation results for mBGA single side placement, board thickness 0.8mm

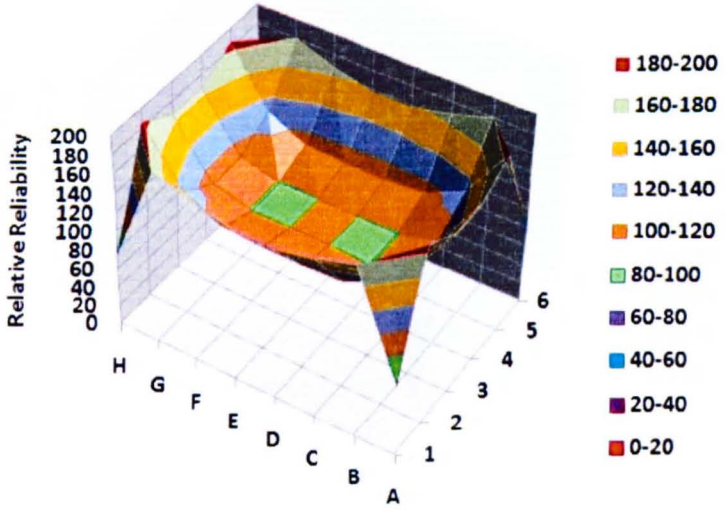


Figure 4-17: Simulation results for mBGA single side placement, board thickness 1.6mm

The modelling scenarios presented show relative reliability in terms of a Weibull characteristic life in which 63.2 % of the parts failed. For solder fatigue failure modes, the Weibull slope is known to be in the range of 6 to 8 (Popelar, 1998).

The relative reliability was calculated for all interconnections in quadrant A1 to D3 with respect to solder ball A1. Using symmetry, the relative reliability of the remaining package interconnects was calculated. The influence of substrate thickness on package reliability is clearly observed in Figure 4-16 and Figure 4-17.

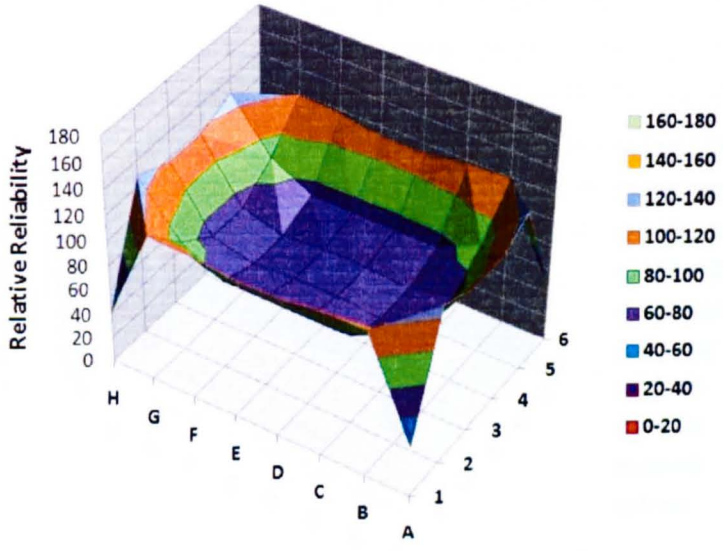


Figure 4-18: Simulation results for mBGA single side vs back to back placement, board thickness 0.8mm (considering topside package only)

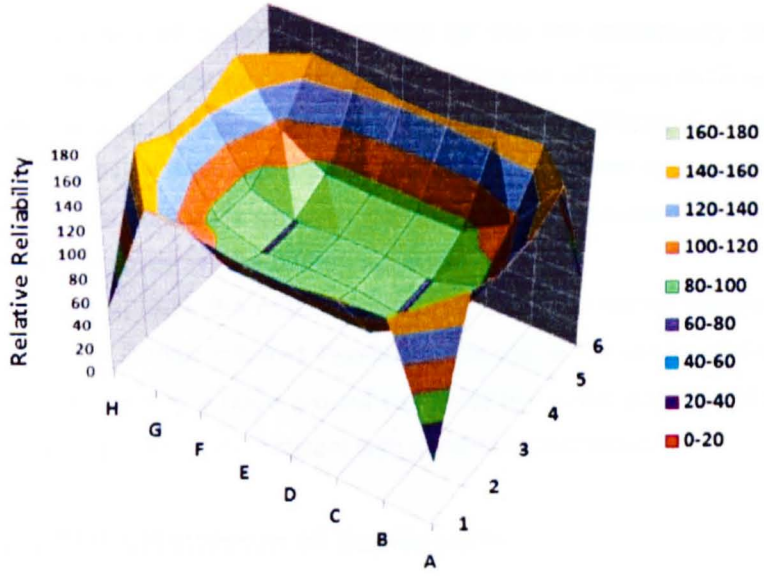


Figure 4-19: Modelling results for mBGA single side vs back to back placement, board thickness 1.6mm (considering topside package only)

In Figure 4-18 and Figure 4-19 a comparison is drawn between single side and back to back placement for 0.8mm and 1.6mm substrates respectively. Solder ball A1 of Figure 4-16 and Figure 4-17 are used as the reference joints representing 100% reliability. Simulation results from each of the A1 to D3 quadrants for the back to back configurations were then used to calculate the percentage reliability change relative to A1 for the respective substrate thickness. The simulation results show an average drop in life expectancy of about 15% in the case of 0.8mm substrates and about 22% in the case of 1.6mm substrates.

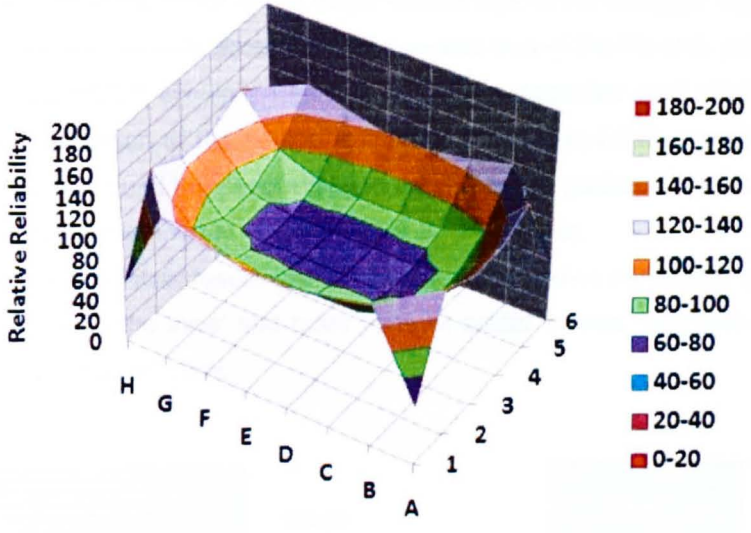


Figure 4-20: Modelling results for mBGA comparing single side placement 0.8mm PCB to 1.6mm PCB thickness.

In Figure 4-20 the effect of substrate thickness on the life expectancy of a single side component is considered. In this comparison solder bump A1 of Figure 4-16 was taken as the reference joint with all other bumps in the quadrant of A1 to D3 of Figure 4-17 used to calculate the relative reliability respectively, as a percentage change against the assumed reliability of 100%. In this simulation the results show an average drop in life expectancy of about 12% for the 1.6mm substrate compared to the 0.8mm substrate.

As in the flip chip case studies, the mBGA simulations show the corner bumps fail first. In the mBGA case studies this is then followed followed by bumps at the centre of the package. The second row of bumps, forming a ridge around the periphery of the package show consistently higher levels of reliability. This is inconsistent with general expectations.

4.9 Summary and Discussion of the Results

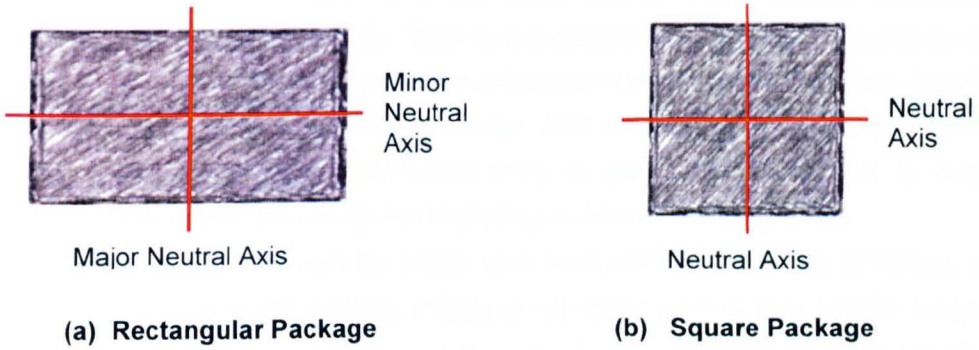
Finite element modelling provides a cost-effective and complementary approach to the study and understanding of solder joint behaviour. There are very few research publications in which consideration is given to component interaction, floor plan layouts or constraint points on

component interconnect reliability. Although Ye (Ye, et al., 2007) has previously performed studies on mirrored components, the modelling did not take into account floor plan influences.

In this chapter a novel approach to modelling was used to examine such research themes resulting in a conference paper publication at ESTC 2010, Berlin (Braden, et al., 2010) discussing the impact of component floor plan layout on the overall reliability of electronics systems in harsh environments.

All case study simulation results in this chapter show a distinct failure distribution pattern. Critical solder joints at the package corners have the lowest levels of cycle survivability or reliability compared to joints closer to the major neutral axis of the package illustrated in Figure 4-21. A similar distribution exists about the minor neutral axis of the flip chip package but this is less obvious. In the mBGA simulation studies, additional degraded joint reliability in a region surrounding the intersection of the neutral axis shown in Figure 4-21(b), producing a ridge of higher reliability joints around the peripheral second row of the package. This is consistent with results published by Chandran et al (Chandran, et al., May 2000).

Furthermore the 3D simulation results graphs for the case studies performed show differences in performance between the inner and outer rows of solder bumps, with less deviation being seen in the globally modelled case.



(a) Rectangular Package **(b) Square Package**

Figure 4-21: Example of package neutral axes

It can be concluded that the rectangular shape of the flip chip used in this study influenced the failure distribution of the solder bumps, the major neutral axis residing on the central axis of the longest side of the die. A similar neutral axis exists on the shortest side of the die but because this length is so small (approximately 2.25 times less) relative to the longest side of the die the distribution appears to be almost non-existent. For square packages such as the mBGA, neutral axes exist in the centre of each package side as illustrated in Figure 4-21(b). It could be argued therefore that optimised area array package design would be one in which the neutral axes are equal as is the case of the square packaging of Figure 4-21(b) and would therefore result in equally distributed shear stress forces.

Solder joints located furthest from the neutral point of the package or die will experience larger shear force deformation under cyclic thermal loading. The intersecting axes in Figure 4-2 being the neutral point of the package. Popelar states that the total shear strain γ is directly proportional to the distance of the bump from the neutral point (axis) of the package (Popelar, 1997). Consequently shear deformation increases when DNP is increased; resulting in lower fatigue life.

$$\gamma \propto \frac{DNP}{h}\Delta T \Delta \alpha \qquad \textbf{Equation 4-7}$$

Where *DNP* is the Distance from Neutral Point of the package to the corner most joint, ΔT is the thermal profile, Δα is the CTE mismatch and h is the net solder joint height (stand-off minus conductor thickness).

Conclusively the simulation results have shown that substrate thickness can affect joint performance, particularly at the critical solder joints furthest from the neutral axis of the package and typically residing in the package corners. Moreover, the predicted reliability from 'global' models incorporating circuit board constraints and component floor plan layout influences show significantly lower levels of reliability; up to 64% in the case of single flip-chip placement and mirrored configuration modelled globally. Since in this study board thickness accounts for a 14% drop in relative reliability in the case of 1.6mm substrates it would appear that floor plan layout and constraints have more influence on solder joint reliability than substrate thickness. Furthermore, global modelling of CBA's are likely to give better correlation to reliability experienced in the field than the non-global modelling performed routinely to-day.

In the next chapter a novel through life solder joint measurement method is presented which uses information available in the acoustic images of the solder joints to give a better insight into joint behaviour. Validation of the proof of concept for the proposed measurement method is undertaken by comparing the simulation results of this chapter with real experimental results.

Chapter 5

Solder Joint Through Life Monitoring

This chapter presents a novel method by which to monitor the through life performance of solder joints using AMI. Popelar (Popelar, 1998) identified that fatigue life could be mathematically predicted with high accuracy based on the diameter or 'cap size' of the UBM within a region encompassing 12.77 microns of the solder bump to silicon interface. In this work the 'cap size' in Popelar's work is extended by considering it as a 2D plane along which a crack has fully propagated through the joint.

In this thesis, the solder joint fatigue life is monitored by ultrasonic NDE. Firstly, the AMI images are collected at regular intervals throughout the environmental testing duration. Secondly, image processing is used to extract crack plane Region of Interest (ROI) information from individual solder joints. This uses an AMI image processing method developed within the Electronic and Ultrasonic Engineering (EUE) research group based within the General Engineering Research Institute (GERI) at Liverpool John Moores University. Finally, from the ROI information the diameter of the crack plane is determined and used to provide an estimate of cycles to failure. In this work complete crack propagation through the joint is considered as a failure.

Results presented in this chapter concentrate on analysing AMI images of topside (RSS1) flip chip devices U23 (single side) and U31 (mirrored) deployed on 0.8mm and 1.6mm organic substrates. This focus is supported by the simulation results of Chapter 4 in which it is observed that there was little difference for mirrored configurations in the failure performance of solder joints in components placed on either the top or bottom side. AMI data is available for all the flip chips placed on the test board and is archived on a DVD at the rear of this thesis. Measurement results were compared directly to the simulation results of Chapter 4 for the equivalent configurations.

5.1 Measurement of Crack Plane Diameters of the Solder Joints

C-Scan acoustic images were obtained as outlined in chapter three at eight cycle intervals starting at zero, through to 96 cycles at which point testing and AMI imaging was terminated. High intensity pixels at the centre of the solder bump, as shown in figure 5-1 and highlighted in red for clarity, represent regions of high acoustic impedance mismatch. These are likely to be cracks at the die to bump interface or grain structure changes as shown in figure 3-30 and figure 3-31. The crack plane diameter measured from the ROI found through post processing the AMI images of solder joints is identified as one key indicator of solder joint performance. The shape and size of the crack plane is directly linked to the cyclic fatigue energy applied to the solder joint. It is logical to suggest that the feature being examined is fundamentally circular in nature and can be simply quantified in terms of diameter. Since a solder ball is spherical in nature, then

any cut across the ball would reveal a circular plane. Propagation of the crack will commence at the peripheral edge of the circular plane described and migrate to the centre of the plane. At this point there is complete separation or failure of the solder joint.

Paradoxically, reflow of the solder balls causes them to distort in shape, having a flattened or oval appearance rather than a spherical. Since the failure region is so close to the UBM cap, which is circular, any bump distortions due to reflow will not affect the measurement method.

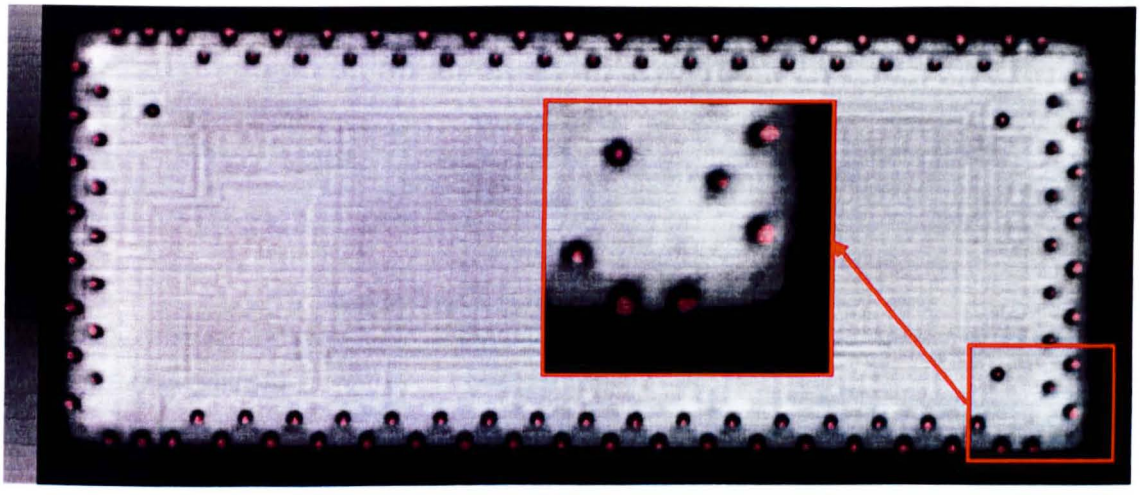


Figure 5-1: CSAM image including radial gradient based region growing segmentation.

A typical ultrasound image obtained is shown in Figure 5-1 where the solder joints are round in shape and have strong greyscale contrast indicating the hypothesis to be true. As a result of the thermal cycling both the intensity and size vary. Therefore any feature detection algorithm used to extract the ROI must be capable of discriminating the solder joint features in both cases.

There are many different methods in which to extract the ROI from the raw image and thereby determine the associated diameter of crack plane. A robust feature extraction algorithm has recently been developed at LJMU and reported in previous research by Yang (Yang, et al., 2010b) (Yang, et al., 2010a). This was deployed in order to obtain the ROI as outlined in the flow diagram of Figure 5-2.

A gradient based circular Hough transform is applied to the C-scan images in order to detect the existence and location of individual solder joints. Prior to the application of the circular Hough transform the gradient of the image is measured. The gradient of the image being a vector point transitioning from dark to light from the centroid of the solder joint. By comparing the measured gradient value to a threshold and excluding gradients lower than the threshold, a reduction in background image information processed by the Hough transform mapping computation is achieved. This reduction in processed information reduces computation time.

The circular Hough transform detects centroid positions and radius for each joint in an image from which seed points for the following Radial Gradient region growing algorithm are determined. This image processing technique makes use of the greyscale information

surrounding the seed point out to an area defined by the pixel intensity values near the inner black ring seen in the images of Figure 5-1 which are selected as the stopping criterion for the growing region.

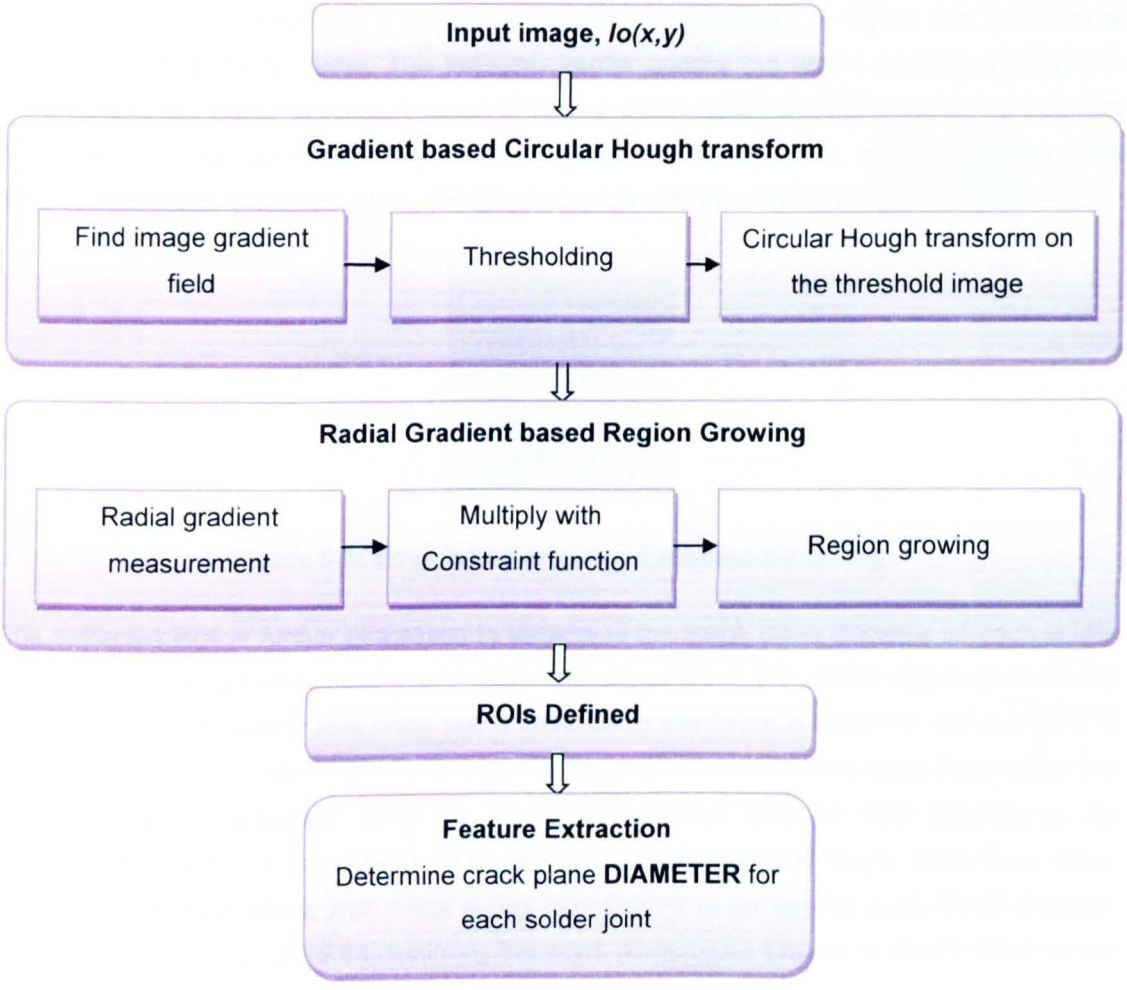


Figure 5-2: Feature extraction flowchart (LJMU EUE research Group)

This image processing technique then makes use of the greyscale information surrounding the seed point to extract the high intensity region found in the middle of each solder joint as shown in Figure 5-1, highlighted in red for clarity which is deemed to represent the crack plane.

Starting from the seed point, neighbouring pixels around the seed point with intensity values higher than a threshold which have similar properties are assigned to the region denoting the crack plane area. The process is continued out to an area defined by the dark pixel values near the inner black ring seen in the images of Figure 5-1 and more clearly in Figure 5-4(a) which determines the boundary of the solder joint. The ring border information is determined by the Radial Gradient Index (RGI) as reported by Yang (Yang, et al., 2010a) and Kupinski (Kupinski,

et al., 1998). The mean intensity of the solder joint boundary pixels is used as the threshold value to decide the similarity and the region growing stopping criteria. Region growing stops when all the intensities of the neighbouring pixels are lower than the threshold.

As discussed in Chapter 3 section 3.6 the influence of edge effects causes joints nearest the package edge to only contain a fraction of a black ring as shown in Figure 5-3. Variation is observed from bump to bump. This indistinct border causes the region growing algorithm to grow beyond the actual solder joint region of interest (ROI) resulting in the extraction of incorrect high intensity pixel perimeter information. To prevent this overgrowth, an isotropic Gaussian constraint function (Kupinski, et al., 1998) is multiplied with the original image.

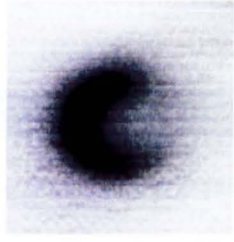
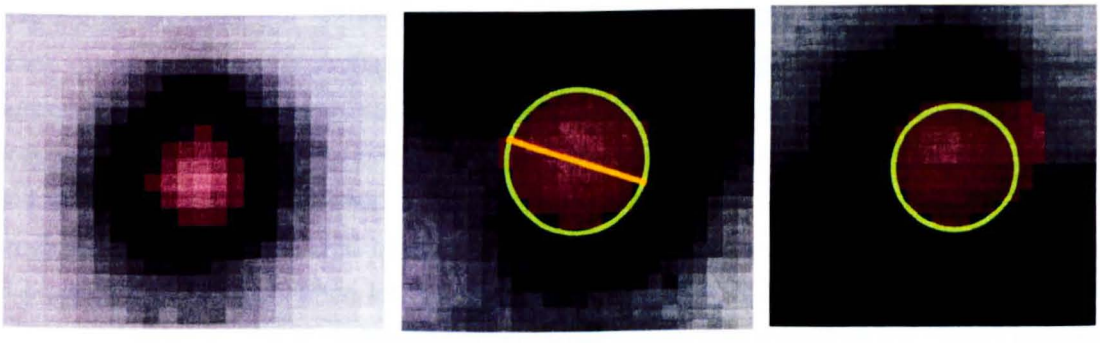


Figure 5-3: Edge bump showing fractional black ring

The extracted ROI is further processed to determine the crack plane diameter of each solder bump in the acquired ultrasound image. High intensity pixels in the central region of the bump image describe the solder joint crack plane area. Since the bump is spherical and the UBM is circular in shape it is reasonable to simplify the crack plane surface to a circle from which the diameter may be calculated using the MATLAB™ software platform from MathWorks. As illustrated in Figure 5-4 (red pixels), ROI's are not perfectly round in shape. Distortions occur due to imaging edge effect, joint reflow during manufacture or the applied cyclic thermal stress. Diameter calculations based on assuming the crack plane being circular in nature which is not the case in Figure 5-4(c) may be inaccurate.



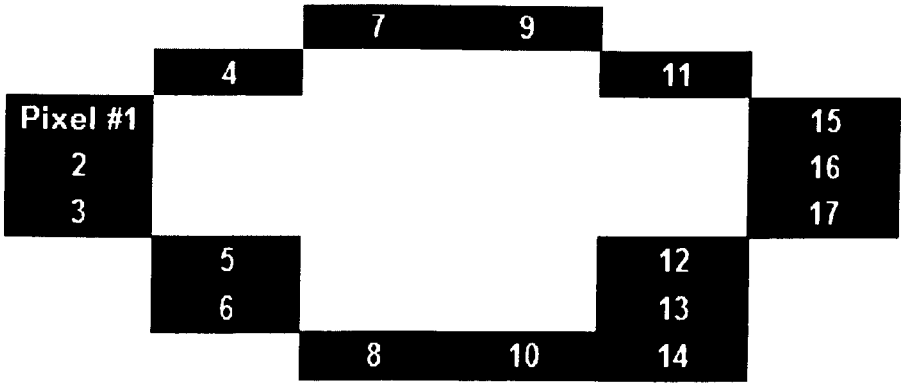
(a) Magnified image of single bump showing crack plane

(b) Diameter measurement of failure region

(c) Image of Solder Bump showing edge effect

Figure 5-4: Magnified images of crack plane measurement of individual bumps

Therefore, an averaging technique is used to determine the diameter of the crack plane. Firstly the perimeter of the pixelated ROI is extracted from the image of Figure 5-4(a) as illustrated in the diagram of Figure 5-5. Secondly the maximum distance in terms of pixels is calculated for all pixel pairs which form part of the extracted perimeter.



Perimeter extraction and Pixel numbering

Figure 5-5: Diagram of a pixelated region of interest (ROI)

For the example shown, the distance between pixel 1 with respect to pixels 2, then 3, 4, 5 etc. up to 17 are measured and the maximum value determined. This is then repeated for pixel 2 with respect to 1, 3, 4, 5, through to 17. Finally the average crack plane diameter is determined from calculating the average of all the maximum pixel pair results. The resulting diameter and circular region described by the orange line and green circle of Figure 5-4(b) is an approximation of the ROI. Bearing in mind that at this stage the unit of measurement is in Pixels, conversion is required to obtain the physical measurand value. The conversion factor used was 1 Pixel = 8.89 μm is detailed in 0. In order to evaluate the work described in this section with the published work of Popelar et al (Popelar, 1997) (Popelar, et al., 2000) the physical measurement is specified in mm. Although this method of describing crack plane area may not be accurate, the circular region described by this diameter covers the majority of the crack plane as illustrated in Figure 5-4(b) and (c). Unsurprisingly, some artefacts remaining outside the extracted circular crack plane may affect the accuracy of the results. This is most noticeable for example on the corner joints that suffer from image distortion due to edge effect and is clearly observed in Figure 5-4(c). The influence of pixels outside the extraction ROI on predicted cycle's accuracy shall be studied in the future.

In practice it is not uncommon for the fatigue life cycle count to be in the thousands as such, variation in terms of 10's of cycles is relatively small having little impact on the overall reliability study. Unfortunately in this study the cycle count is <100 therefore errors in terms of tens of cycles are likely to be more influential on the study. Nevertheless this does not invalidate the novel method proposed or work undertaken. The intent of the aggressive environmental thermo cyclic test regime was to generate failures in the shortest time possible due to availability of

resources. Further work is required to improve resolution and determine accuracy of the methodology proposed. From the experimental work performed, the use of a uniform circular crack plane is the most natural template to use in this instance since the solder ball is generally circular in nature. However this template could not be applied to non-circular interconnects found in say leaded components.

Measuring the diameter of the crack plane may not in itself be the best feature in which to determine the fatigue life (cycles), which is due in part to the resolution accuracy resulting from the pixel size in the image but also due to the variation in the boundary or shape profile of the high intensity region of the bump. Although not investigated in this research it does present opportunities for future research since additional information related to the thermo dynamic behaviour of the solder joint may be contained in the boundary or shape information. A more robust method would be to make use of pixel intensity within the ROI region to map against cycles to fail. Using a 'pixel count' method to calculate the crack plane diameter is inherently reliant on pixel or more accurately, scan resolution in which to measure the diameter of the crack plane. Scan resolution is set manually by the Scanning Acoustic Microscope (SAM) operator. Throughout this work the scan size comprised of 1024 x 768 pixels. For the 230MHz transducer used in this research a 15μm feature resolution can be achieved. Since each pixel represents 8.89μm for a scan resolution of 1024 x 768 pixels then clearly at best a 15μm feature is represented by 2 pixels. Increasing scan resolution to the maximum 2048 x 1920 available, results in the same 15μm feature being represented by 4 pixels, therefore providing a two fold increase in measurement resolution accuracy.

Without further studies it is arguable and difficult to assess whether the imaging used in this research had insufficient resolution. Furthermore, increased scan resolution is also a trade off in the measurement process. Higher resolution results in larger image file size and longer scan times; typically for 1024 x 768 the scan time is 8 minutes per scan rising to 15 minutes for the highest resolution available on the Sonoscan D9000 of 2048 x 1920.

5.2 Ultrasound Imaging and Crack Plane Results

5.2.1 Ultrasound images of bumps

The proposed inspection method is reliant on the hypothesis that firstly the diameter of an assumed circular crack plane occurring at the bump to silicon interface can be recovered from ultrasound images of joints. Secondly, the term crack plane has been defined as the most likely plane of failure. Use of this terminology is warranted through experimental work including micro sectioning. Even though most joints will show no failure at the start of testing, the crack plane observed at the start defines the size of the contact plane between each solder ball and UBM, in terms of a diameter. As testing starts to initiate failure the "crack plane" or diameter will grow from a small initial diameter where no failure is present, to a larger diameter as failure starts to be detectable.

This is illustrated in the raw ultrasound data images of Figure 5-6 to Figure 5-9 obtained for bump 107 of flip chip U23 at 0, 48 and 96 applied thermal cycles. Bump 107 was selected from the flip images taken as it would appear to have been least affected by edge effects.
Two thicknesses of substrate are also considered. For each image the measured crack plane is calculated as described in Section 5.1 and included for completeness in the figures. Diameter values are given in both pixel and engineering units. A full data set and flip chip images undertaken in this research is available on a DVD at the rear of this thesis. The physical measurement is specified in mm so that it can be compared readily with Popelar's work. The images for bump 107 have been extracted directly from the AMI images of flip chip U23 and U31 for the respective PCB thickness and magnified for illustrative purposes.

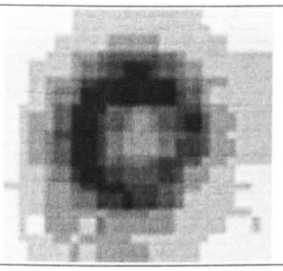
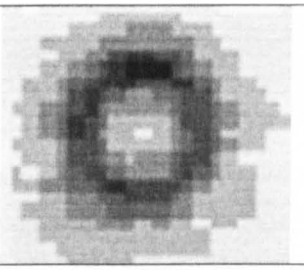
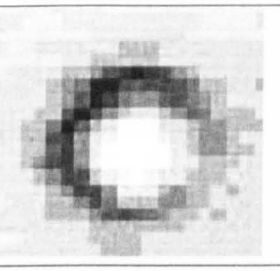
		
Crack Plane = 4.171 Pixels Crack Plane = 0.037 mm	Crack Plane = 5.687 Pixels Crack Plane = 0.051 mm	Crack Plane = 6.886 Pixels Crack Plane = 0.061 mm
(a) 0 Cycles	(b) 48 Cycles	(c) 96 Cycles

Figure 5-6: U23 single side placement, bump 107, 0.8mm organic substrate

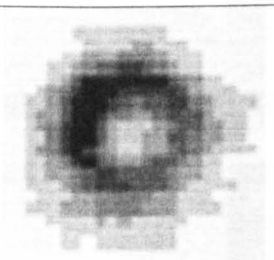
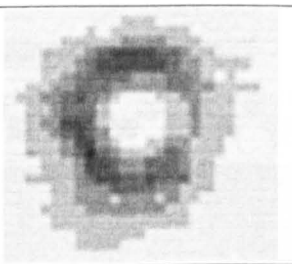
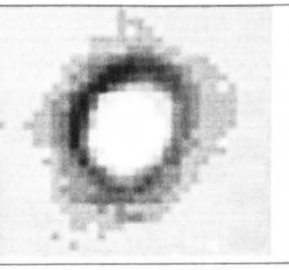
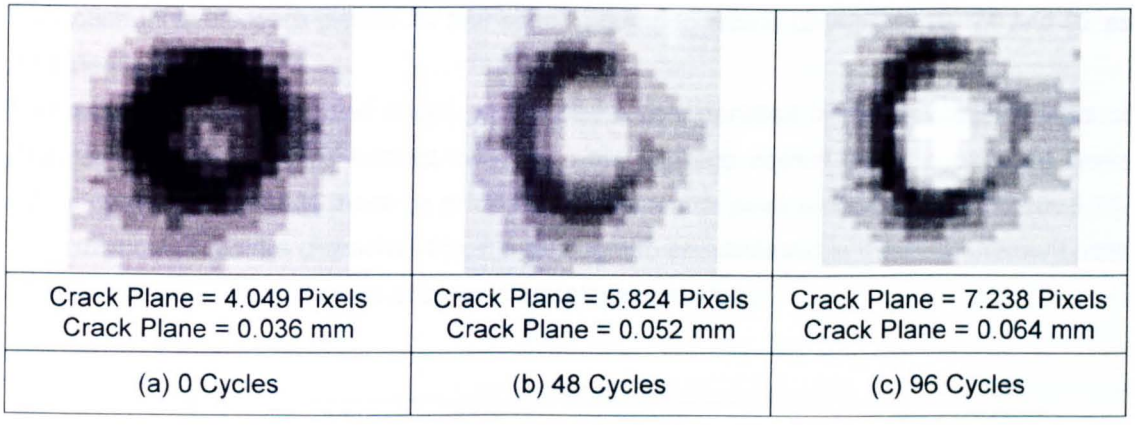
		
Crack Plane = 4.973 Pixels Crack Plane = 0.044 mm	Crack Plane = 5.914 Pixels Crack Plane = 0.053 mm	Crack Plane = 8.761 Pixels Crack Plane = 0.078 mm
(a) 0 Cycles	(b) 48 Cycles	(c) 96 Cycles

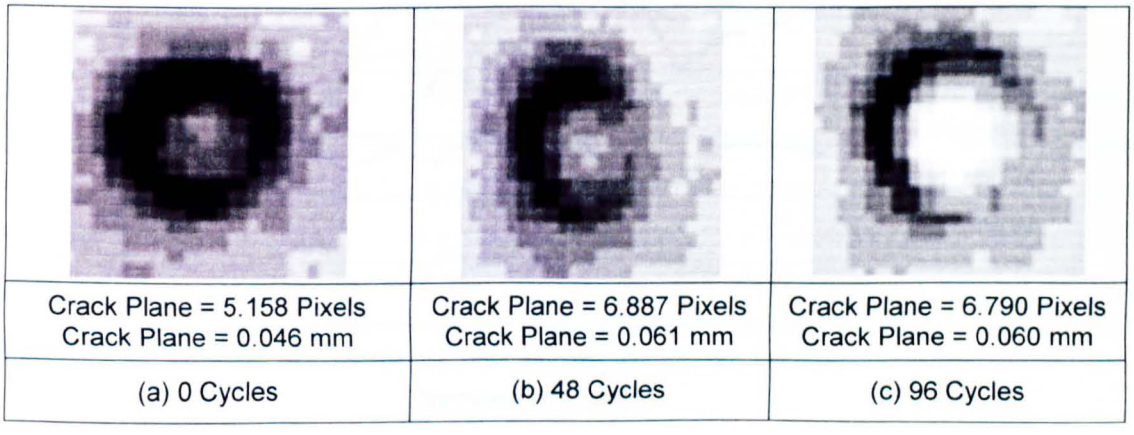
Figure 5-7: U23 single side placement, bump 107, 1.6mm organic substrate

Visual analysis of figure 5-6 to figure 5-9 shows a dark ring outlining the solder joint interconnection resulting from edge effect, the centre of the joint is represented by a light grey region characteristic of the crack plane. Moreover this light grey region expands in size and grey scale intensity as the cycle count increases, supporting the feasibility of this innovative method of non-destructive through life measurement.



Crack Plane = 4.049 Pixels Crack Plane = 0.036 mm	Crack Plane = 5.824 Pixels Crack Plane = 0.052 mm	Crack Plane = 7.238 Pixels Crack Plane = 0.064 mm
(a) 0 Cycles	(b) 48 Cycles	(c) 96 Cycles

Figure 5-8: U31 top side placement, bump 107, 0.8mm organic substrate



Crack Plane = 5.158 Pixels Crack Plane = 0.046 mm	Crack Plane = 6.887 Pixels Crack Plane = 0.061 mm	Crack Plane = 6.790 Pixels Crack Plane = 0.060 mm
(a) 0 Cycles	(b) 48 Cycles	(c) 96 Cycles

Figure 5-9: U31 top side placement, bump 107, 1.6mm organic substrate

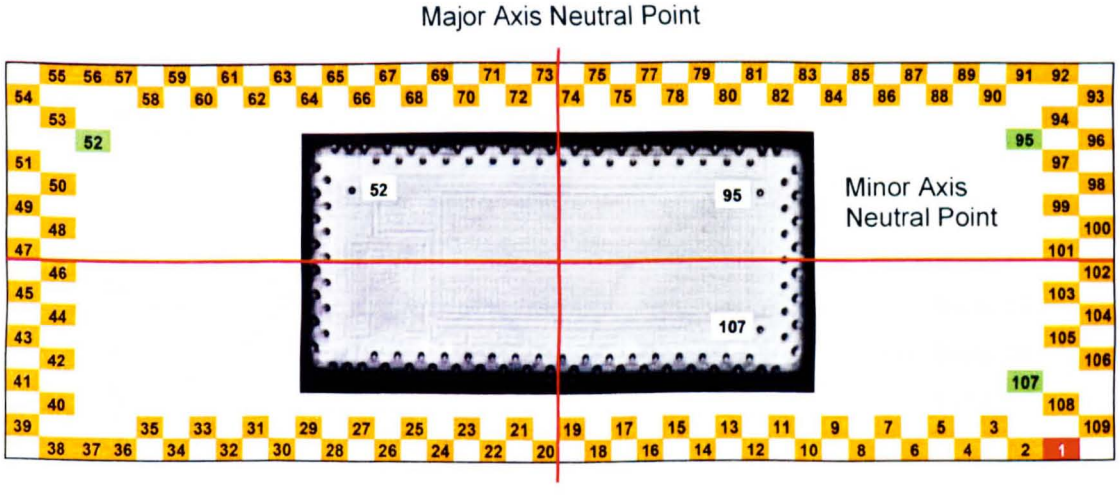


Figure 5-10: Bump labelling and package neutral points

A more qualitative assessment of joint performance was undertaken by extracting the crack plane diameter dimension for every solder joint on each package image examined. The measurement values obtained for 0.8mm and 1.6mm substrate thicknesses at 8 cycle

inspection intervals were plotted for four specific bump locations (Bumps 1, 19, 74 and 92 as indicated in Figure 5-10).

Bump locations were selected based on the distribution identified in the simulation results of Chapter 4 in which bumps furthest away from the package neutral points experience lower failure cycles compared to those on or closest to the neutral point as illustrated in Figure 5-10. Such distributed feature characteristics, if true, ought to be witnessed in the measurement plots of the proposed system in terms of larger crack plane diameters.

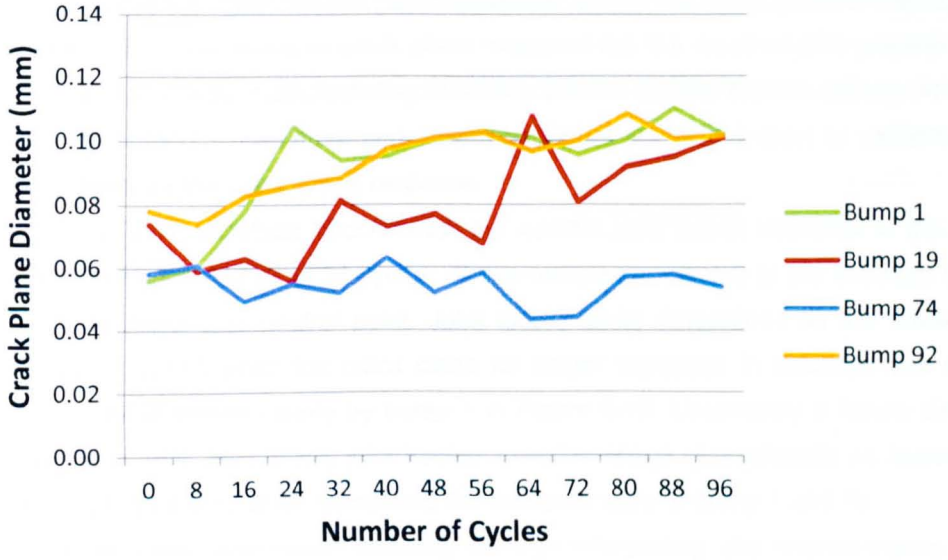


Figure 5-11: Bump characteristics for U23 0.8mm substrate.

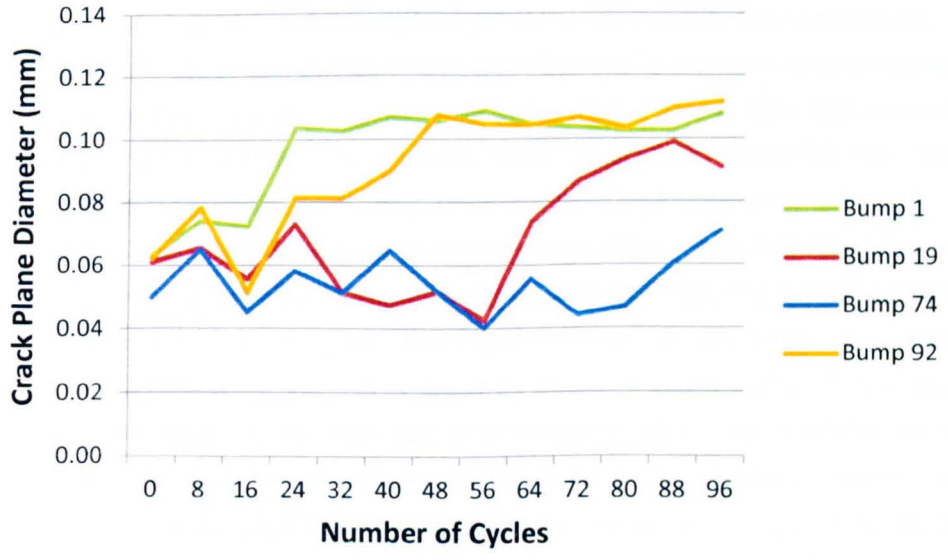


Figure 5-12: Bump characteristics for U23 1.6mm substrate

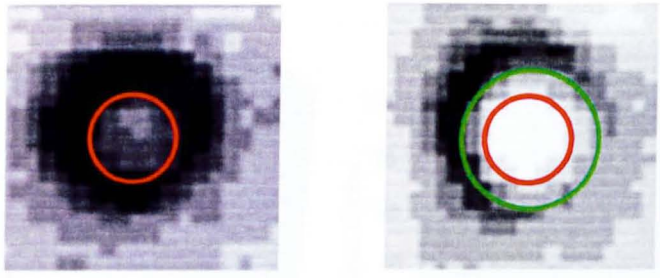
In the presented data Bump 1 and 92 are critical solder joints located at the corners of the package furthest from the major axis neutral point, Bumps 19 and 74 lie on the package neutral point. Figure 5-11 and figure 5-12 conclusively show the diameter of the crack plane increasing with increased fatigue cycle exposures. Moreover, each bump displays a unique crack plane characteristic resulting in different points of failure. In this work the point of failure is indicated by a sharp increase in crack plane diameter value greater than 0.1mm. This value is based on the cap size of the UBM on the silicon which is 0.104mm. Clearly any crack plane diameter cannot be larger than the diameter of the solder bump and UBM cap diameter. Values less than the 0.104mm signify that the crack has not fully propagated across the bump to UBM interface area being examined. Such variations in crack plane response are the result of joint position on the chip, interconnect geometry, manufacturing assembly and the applied thermo-cycling. Additional factors such as substrate thickness and CBA population are also known to influence joint reliability and therefore the crack plane response.

Unsurprisingly for both substrate thicknesses, the earliest joint failure occurred in the critical solder joints of bumps 1 and 92 at 24 cycles. These bumps are located at the package corners furthest from the major axis neutral point. Joint failure being determined as the crack plane diameter value or cycles when the crack plane no longer increases in diameter and its size becomes static as illustrated clearly by bump 1 in Figure 5-12. Undeniably a failure threshold value is specific to each joint. Every joint having a unique failure characteristic as illustrated in Figure 5-11 and Figure 5-12 when comparing the characteristics of bump 1 and 19.

Threshold values were determined manually through interpreting the characteristics of the critical bumps located at the package corners. This value was then applied to all bumps in order to derive the 3D plot data for the graphs in Section 5.2.2. Further research is required in this area to establish a more accurate and repeatable method; including the development of a software algorithm to establish individually from joint characteristics its failure threshold.

The graphical results presented in Figure 5-11 and Figure 5-12 highlight an anomaly requiring further explanation. Assuming good solder joints at the start of testing then logically one would expect the crack plane diameter to be zero, which clearly the measured AMI results as illustrated in Figure 5-13 are not supporting. There are three explanations for this.

The first and most important are ultrasound imaging 'edge effect' errors that result from imaging the solder bump which is spherical in nature and generates the black ring surrounding the bump core in the ultrasound images of Figure 5-6 to Figure 5-9 and from which the crack plane ROI is determined. This occurs since the ROI is found by acquiring pixels surrounding a seed point having a greyscale value greater than that of a threshold value. The threshold value being accurately determined from the strong contrast observed at the boundary between the black and dark grey pixels at the edge location of a plane area as shown in Figure 5-13 (a). The red circle in Figure 5-13(a) shows a region of the solder bump bounded by what has been defined as crack plane area. The greyscale level of the centre pixels in this image at 0 cycles suggesting the existence of a functioning interconnect.



(a) 0 Cycles **(b) 96 Cycles**

Figure 5-13: U31, bump 107, 1.6mm organic substrate

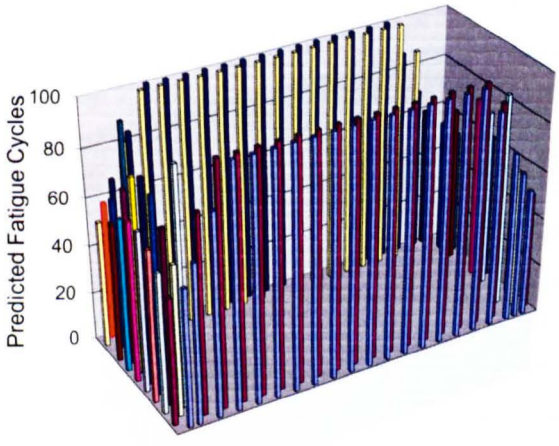
Therefore irrespective of whether a crack exists or not, the proposed ROI image processing methodology results in diameter values which are not absolute and ultimately present incorrect initial crack diameter values. The use of very high resolution acoustic imaging systems encompassing small transducer spot size, ultrasound frequencies greater than 230MHz and increased scan rate would improve the performance of the image processing algorithm. This does not render the technique invalid but does explain the existence of a 'crack plane diameter' when no fatigue cycles have been applied to the test samples.

Secondly the expectation of zero defects at 0 cycles and therefore no crack plane diameter being present may not be correct, making this technique particularly useful in reliability studies. However, the presence of cracked joints were not verified by sectioning of bumps at the start of testing as this is destructive in nature and prevents further AMI scans on the boards being undertaken. Therefore this hypothesis is not proven. Moreover no two boards are considered identical so although the sectioned board may confirm a crack in a specific bump at zero cycles, additional boards subjected to AMI may not show cracks in the same bump or location within the bump.

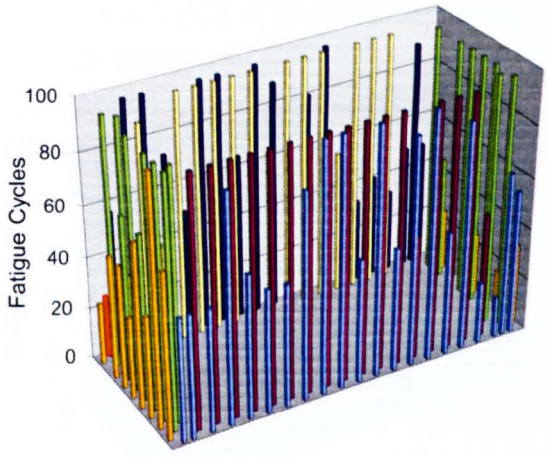
Thirdly, since the crack plane diameter values are not absolute due to the edge effect described, using a single linear measurement technique on its own can contribute to cycle count errors. The ROI represented by the red circle in Figure 5-13(a) has increased in size as represented by the green circle in Figure 5-13(b). Clearly post 96 cycles the bump has a high intensity or bright pixel region at the centre, therefore the fusion of multiple image features, for example crack diameter and ROI greyscale intensity within the image would improve the measurement system further.

5.2.2 Correlation of simulated and measured results

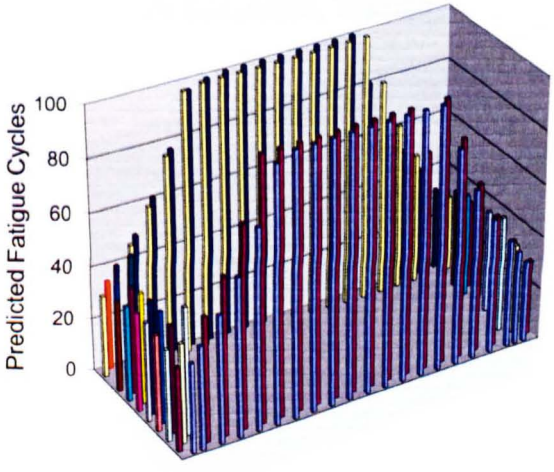
In this section of the study the fatigue life versus crack plane diameter simulation results of Chapter 4 are correlated with AMI measurement results obtained from fully populated test boards. A good level of observed correlation confirming the underlying measurement technique works in addition to demonstrating the viability of the technique as a reliability assessment tool.



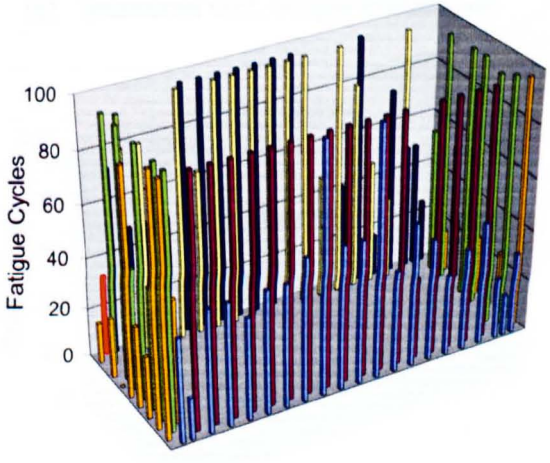
(a) Single Simulation, Topside



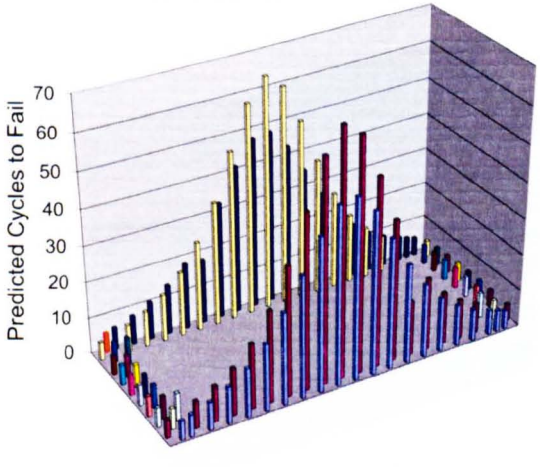
(b) Measured U23, Single Placement



(c) Mirrored Simulation, Topside

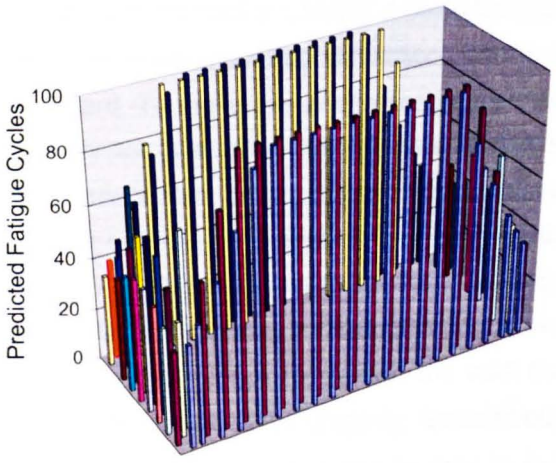


(d) Measured U31, Mirrored Topside Placement

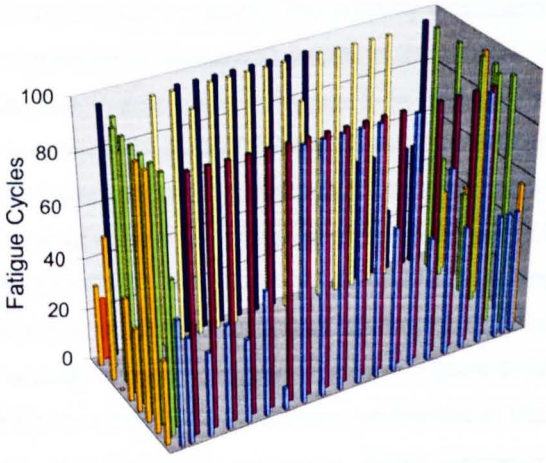


(e) Global Simulation, Mirror Topside

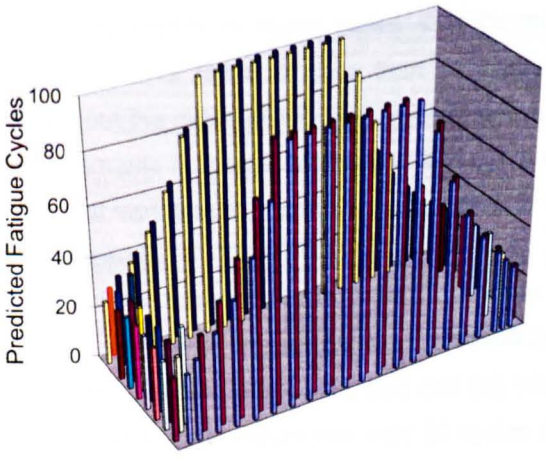
Figure 5-14: Comparison simulation and measured results – 0.8mm substrate



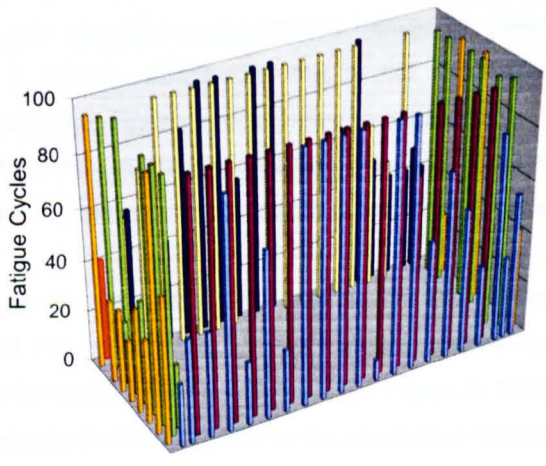
(a) Single Simulation, Topside



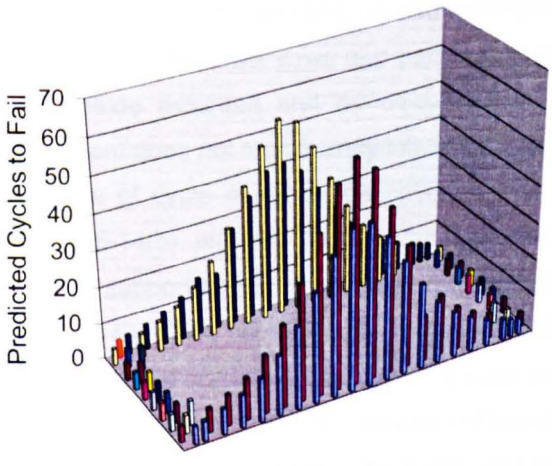
(b) Measured U23, Single Placement



(c) Mirrored Simulation, Topside



(d) Measured U31, Mirrored Topside Placement



(e) Global Simulation, Mirror Topside

Figure 5-15: Comparison simulation and measured Results - 1.6mm substrate

Since the measured results were obtained from unconstrained test boards not all the simulation scenarios performed in Chapter 4 could be used in the correlation study. The primary exclusions were the global modelling simulations due to the inclusion of constraint points in the corner of the board. To make the results comparison easier, the Y axis scale in Figure 5-14 and Figure 5-15 for the simulation results were limited to a maximum of 100 cycles. Bump one being identified in Red on all graphs with subsequent bump numbering following the numbering scheme outlined in Figure 5-10. Although on the face of it, measured results in Figure 5-14 and Figure 5-15 do not appear to correlate well with the simulation results nevertheless this does not signify the technique as a concept is flawed or incorrect. Simulation assumes the best case and is an idealised joint performance. The work has already shown in Figure 5-11 and Figure 5-12 that solder joints behave uniquely. Since through life monitoring has not been performed in this way before, the measured results may in fact be correct in their response. Albeit individual bump cycle values are lower or higher than predicted.

Sectioning results in many cases validate that the diameter measurement results for joints shown to have failed at less than 96 cycles is correct. Admittedly, this is not consistent throughout the entire distribution of joints on the package. Further investigation is required.

Improvements in image processing and cycle calculation methodologies that take into account individual variation in bump metrology results would yield an improvement in the overall cycle fatigue results.

In the 0.8mm case of Figure 5-14(b) which is a single side placed flip chip device the results correlate well with the single side simulation of Figure 5-14(a). Ignoring shape distribution differences between Figure 5-14(a) and (b), then for bump 1 (corner bump) then Figure 5-14(b) shows fatigue cycle failure just over 20 cycles compared with 58 cycles in the simulation results of Figure 5-14(a). It is also evident that for many of the bumps on the inner rows of the package connection footprint that there is some level of correlation with the simulation results.

Moreover Figure 5-14(b) and (d) show similarity in bump response and distribution, particularly for bumps in the inner rows and package corners. This is to be expected since both flip chips are topside mounted and as discussed in Chapter 4 on simulation results, mirrored part placement does not significantly influence interconnect performance.

In terms of cycle count of the critical solder joints and distribution toward package corners, Figure 5-14(b) and (d) have better correlation to the 'mirrored' simulation result of Figure 5-14(c), supporting the hypothesis that modelling, which does not include additional influences found on the CBA, will introduce solder joint reliability estimate errors.

Likewise measured and simulation results show differences between inner and outer bump rows. Unquestionably this is a function of bump distance from the neutral point of the silicon and the CTE differences between the silicon and the substrate. Although the same feature occurs in both measured and simulation results there are marked differences in the fatigue cycles. The inner rows of bumps provide better shape correlation to the simulation results which is an outcome of the measurement being more accurate due to less 'edge effect' influences. Since

edge effect influences the stopping boundary of the region growing algorithm; resulting in bumps in the outer rows of the package having larger than expected crack plane diameters. It is suggested that the pixel resolution of the acquired images is also too low, thereby contributing to further errors in the crack plane diameter values. Similar results are seen in Figure 5-15 for the 1.6mm substrate case study.

In both substrate cases poor correlation is witnessed between the global simulation results and those of Figure 5-14(d) and Figure 5-15(d). This is expected since the test board was not constrained at the PCB corners; consequently U31 and U23 would not experience additional strain influence resulting from the additional constraint.

5.3 Through Life Measurement Summary

In this chapter a novel non-destructive method has been presented that measures crack growth in terms of a gap diameter along a 2D plane from which fatigue cycle exposure estimates prior to failure can be obtained. Qualitative comparisons of simulation results from Chapter 4 with those obtained through AMI measurement show co-relationships exist for bumps 1 to 38 and 3 to 35 for the outer and inner rows respectively along the longest edges of package U26 as illustrated in Figure 5-16 and Figure 5-17.

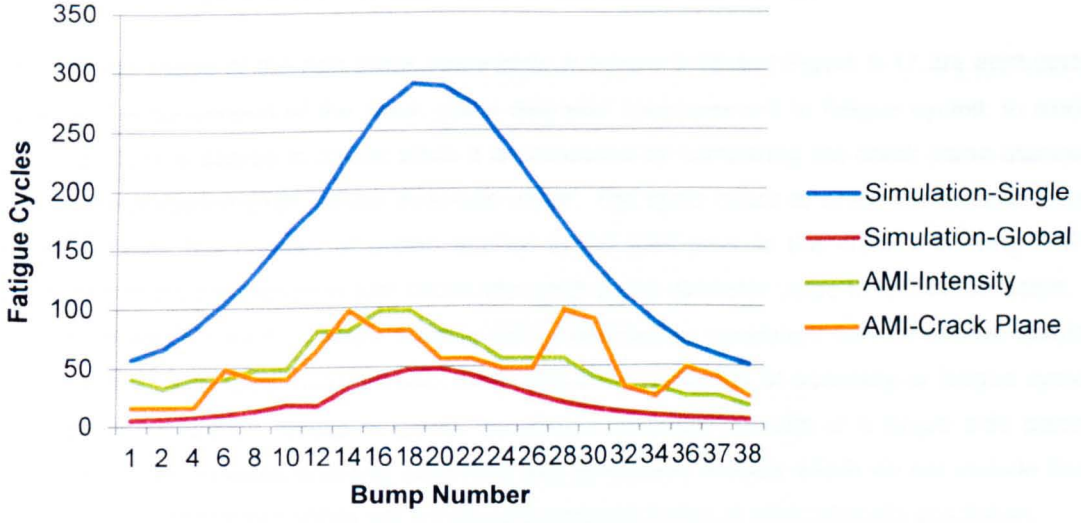


Figure 5-16: U26 outer row, 0.8mm substrate bumps 1 to 38

Fatigue cycle results obtained from Yang's (Yang, et al., 2010c) AMI intensity measurement method are also included in Figure 5-16 and Figure 5-17. Permitting performance comparisons to be made with the proposed crack plane diameter method presented in this thesis.

The shape distribution results from the rectangular shape of the flip-chip, shorter fatigue life being experienced along the shorter edge of the die compared to the longer edge. The aspect ratio of the die is approximately 2.25. The complementary assessment approaches of FEA and

metrology confirm the existence of a failure cycles distribution consistent with the theory that critical joints furthest from the package neutral axes fail first.

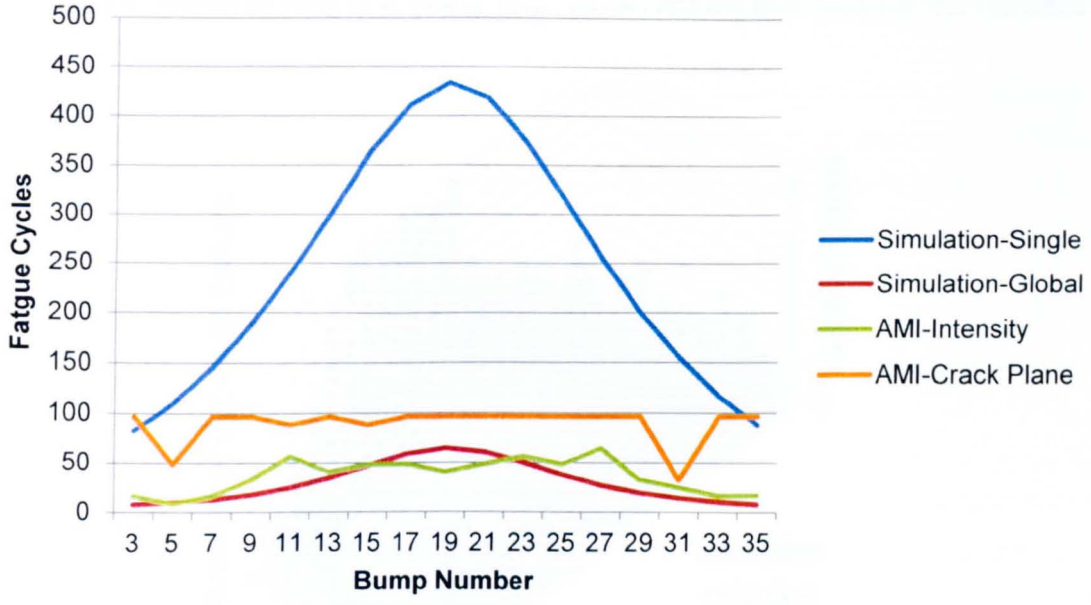


Figure 5-17: U26 inner row, 0.8mm substrate bumps 3 to 35

The complex shape of the AMI crack plane plots in Figure 5-16 and Figure 5-17 are attributable in part to the conversion of the crack plane diameter measurement to fatigue cycles. In reality the cycle count is coarse in nature since it is calculated by comparing the crack plane diameter value to the predetermined 'failure threshold value'. The cycle count at which the threshold was exceeded being the number of cycles applied to the joint prior to the crack achieving 100% penetration of the joint which in turn cause the crack plane diameter value to remain constant.

Figure 5-16 and Figure 5-17 show a bump failure distribution consistent with simulation results. Moreover, the developed measurement method is closer in terms of accuracy or fatigue cycles to the global simulation results obtained, compared simulation results of a single side placed component. This provides a strong argument that simulation models which do not include floor plan layout and constraint points will introduce significant errors in joint reliability prediction.

The graphs presented emphasise the importance of cycle count accuracy, which is dependent upon the accuracy of two variables. Firstly the accuracy of the diameter measurement values, discussed earlier in this chapter and secondly the frequency with which the image measurements were taken. In this research the measurement 'scan' rate was 8 cycles. For test durations with cycle counts in the thousands such high scan rates are not practical in long term reliability testing studies. Extrapolation algorithms which extend the time between acoustic scans are a potential solution. Higher levels of reliability are predicted in the single sided single package simulations. However the AMI measurement techniques concur with the simulation

results for the modelling scenarios which take into account constraint and floor plan layout considerations suggest this modelling approach is closer to real world experience. The crack plane diameter measurement technique compares favourably to fatigue cycle estimates based on intensity published by Yang et al (Yang, et al., 2010c) and the EUE research team at LJMU.

Figure 5-18: 3D AMI intensity plot for flip chip U26 (Yang, et al., 2010c)

Figure 5-19: Rotated 3D fatigue cycles plot for flip chip U26 – crack plane method

This is highlighted in the graph plots of Figure 5-16 and Figure 5-17 and further demonstrated by comparing the critical solder joints in the 3D AMI intensity plot of Figure 5-18 with crack plane measurement method plot of Figure 5-19. The two plots are comparing U26 a single side placed flip chip on a 0.8mm substrate. The plot in Figure 5-19 has been rotate to ensure that bump 1 is aligned with bump 1 of Figure 5-18.

In conclusion the results presented have demonstrated the feasibility of this novel inspection method and shown that it is a valuable tool both in the development and testing of future reliability models as well as through life inspection of area array package solder joints.

Chapter 6

Conclusions

6.1 Summary of Achievements

The work presented in this thesis followed a multidisciplinary approach to developing a non-destructive through life solder joint evaluation methodology for area array packaging. Although several non-destructive testing (NDT) techniques are available having the potential to detect and locate defects in microelectronic devices, the effects of thermal cycling on through life solder joint behaviour has not previously been studied. No single method has been able to satisfy all present non-destructive inspection requirements. The research developed a concept in which a key solder joint feature, nucleating at the bump to silicon interface and propagating across a laminar crack plane could be captured using acoustic microscopy imaging (AMI). Concept feasibility was successfully demonstrated by employing the measurement technique to study the impact of component floor plan layout on the overall reliability of electronics systems in harsh environments. As joint geometries and packaging dimensions reduce it is suggested that floor plan layout, PCB constraint points and substrate thickness will significantly influence solder joint reliability. The proposed new metrology method is crucial in the study of this emerging area of interest, ultimately leading to better physics of failure models and development of model based prognostics in electronics systems.

A wide body of knowledge has been acquired in the research undertaken. Firstly, a comprehensive review of current and emerging packaging and interconnect technologies has shown increasingly a move from conventional 2D to 3D packaging. In the case of SiP, whole systems comprising of stacked silicon and passive surface mount components are integrated inside a single package. This presents not only reliability and thermal management challenges but severe challenges to existing metrology and inspection systems. The realisation of these systems is highly reliant on interconnections between dies in the package. As miniaturisation continues, joint sizes correspondingly reduce and wire bonding no longer becomes viable. Ball or solder column, along with TSV, are becoming the principle interconnection solutions. The proposed metrology system addresses these evolving requirements. A review of reliability terminology, testing and physics of failure models enabled the requisite understanding to subsequently develop the test board, component configurations for physical testing and required FEA simulation studies.

Secondly, in analysing many non-destructive inspection methods two methods were found offering the ability to image difficult to access solder joints, X-ray and AMI. The work showed these to be complementary approaches capable of inspecting solder joint shape, size and

integrity. X-ray is not good at inspection of gap type defects such as small cracks, but can identify the presence of a solder joint though not necessarily the quality of connection. In contrast AMI is an effective method for imaging laminar fatigue cracks and voids in solder joints. Preliminary experimental work confirmed the complementary nature of X-ray and AMI, showing that C-SAM is a feasible approach in which to pursue through life monitoring and inspection of area array solder joints. One limitation identified being that we cannot inspect solder joints by imaging through the lattice weave found in the construction of organic substrates with current ultrasound technologies.

Imaging results from the experimental studies clearly show variation in shape and greyscale of a region residing at the centre of the AMI image of the solder joint. This region of interest (ROI) is an important indicator of solder joint integrity and quality; and measurable throughout accelerated testing. Undeniably the ROI and intensity grow in response to reduced connection quality between bump and silicon in response to applied thermal cycles. A key outcome of this research was establishing this feature within the image of an ageing solder joint. Through simplifying it to a circular plane, from which a diameter value could be extracted, an estimate of thermal cycle exposures experienced by the joint prior to failure could be determined. Since the diameter increases as the crack progresses across the 'crack plane', this demonstrates the feasibility of the method. A crack can be tracked and joint integrity gauged using the proposed non-destructive through life measurement method.

Thirdly, FEA simulations were undertaken for flip-chip and micro-BGA (mBGA) packages placed on FR4 PCB's. Case studies presented in this work investigated the impact of component floor plan layout and constraint points on the reliability of solder joints. Conclusively the simulation results show substrate thickness can affect joint performance, particularly at the critical solder joints furthest from the neutral axis of the package and typically residing at the package corners. This is true in both mBGA and Flip Chip studies. In the case of mBGA, the reliability of the central interconnect region was also reduced, producing a ridge of higher reliability joints around the peripheral second row of the package. This is consistent with the findings of Chandran et al (Chandran, et al., May 2000). Moreover, the predicted reliability from 'global' models incorporating circuit board constraints and component floor plan layout influences show significantly lower levels of reliability; up to 64% reduction in the case of single flip-chip placement and mirrored configuration modelled globally. In this study board thickness accounts for only a 14% drop in relative reliability, in the case of 1.6mm substrates it would appear that floor plan layout and constraints provide more influence on solder joint reliability than substrate thickness. Furthermore, global modelling of CBA's are likely to give better correlation to reliability experienced in the field than the non-global modelling performed routinely to-day. This work provides an explanation for differences in reliability performance seen between circuit board assemblies tested as boards on their own compared to when they assembled into the housing of the final products using glues, thermal paste and screws. This combination of component floor plan layout and CBA constraint conditions are extremely important to

simulation of future products as well as the development of more realistic physics of failure models. Presently in acceleration test models we only consider test and field parameter conditions, no coefficient is applied for the nature or complexity of the final assembly in the product. This provides an explanation as to the reason that so many models exist, each providing correlation to specific test conditions and test sample configurations.

Fourthly, in the investigation work performed, qualitative comparisons were completed using simulation results from Chapter 4 with results obtained through AMI measurement. AMI images were taken at regular intervals. Image processing techniques extracted from the acquired images a diameter measurement for a laminar crack plane, within a solder joint damage region occurring at the bump to silicon interface. The complementary assessment approaches of FEA and metrology confirm the existence of a failure distribution consistent with theory, which states that critical joints furthest from the package neutral axes fail first. Variance in reliability performance is observed between inner and outer bump rows along the longest edge of the package, inner rows consistently having higher levels of reliability than outer. This in part may be explained by the definition of 'distance from neutral point' DNP provided by Ahmed and Brillhart (Mudasir, et al., 2008) who define DNP as "the effective distance along the diagonal of the package, from the centre to its outermost corner". This definition of DNP explains more accurately why the inner solder bump rows are more reliable than outer, including the critical solder joints at package corners. Furthermore, it provides reasonable explanation for the bumps either side of the package major and minor axes having increased levels of reliability.

Higher levels of reliability are predicted in the single sided single package simulations. However the AMI measurement techniques concur with the simulation results for modelling scenarios which take into account constraint and floor plan layout considerations. This modelling approach is closer to real world experience.

In terms of critical solder joints and outer bump rows, the crack plane diameter measurement technique compares favourably to the fatigue cycle estimates based on intensity measurement published by Yang et al (Yang, et al., 2010c) and the EUE research team at LJMU. For inner rows, the crack plane diameter method is showing higher levels of joint reliability than both the AMI intensity measurement method and modelling results. Sectioning results corroborate the diameter measurement results for joints shown to have failed at less than 96 cycles, indicating the methodology as being correct. It is too early to state which technique is more correct, as further work is required on feature extraction and calibration.

Moreover, the developed measurement has provided strong evidence that simulation models which do not include influences due to the placement of other components on the floor plan layout and constraint points will introduce significant errors in joint reliability prediction.

Finally the research undertaken in this study has contributed to the development of a novel metrology concept required to evaluate the interconnect reliability of future packaging. The feasibility of the concept was demonstrated and shown that the through life behaviour of solder joints in flip-chip packaging can be non-destructively monitored. For the FEA simulation case

studies undertaken, preliminary results compare favourably to double sided mirror placed flip chip components. This indisputably demonstrates that floor plan layout influences solder joint reliability. Consequently when performing reliability studies on packaging solder joints using FEA, accuracy is dependent upon modelling the whole board if results are to compare favourably to real life.

6.2 Suggestions for Further Work

The feasibility of a non-destructive through life measurement technique to evaluate solder joint reliability has been demonstrated, and new avenues of research have been identified and further work is suggested to mature the developed technology. Key areas for future work are discussed below:-

1. Calibration of ROI Greyscale

Further work is required to calibrate greyscale levels in the ROI to the characteristics of the gaps generated along the crack plane. A specific greyscale being associated with crack initiation and crack progression tracked within the crack plane region thereby improving accuracy. Access to an AMI machine capable of collecting 3D acoustic measurement data which was not available in this research is required. It is also the case that it would be necessary to accurately calibrate the greyscale intensity information to understand if the chosen intensity is actually representing a crack plane in the joint. This concept of utilising image intensity correlation to estimate cycles to failure is already being pursued by the research team at LJMU.

2. Image Resolution

The scan resolution and transducer frequency used throughout this investigation found that current AMI systems are adequate for imaging the bump, although higher scan resolutions are required in order to improve crack plane dimensional resolution and features. The complementary nature of X-ray inspection and AMI has informed us of further opportunities for improvement of the through life inspection of solder joints. Although not pursued in this research, the fusion of two or more imaging data sets may result in a combined image which has substantially higher defect resolution than is currently available.

3. AMI Tomography

AMI Tomography or 3D inspection of solder bonds would be extremely useful in investigating crack nucleation and propagation. Although the technology currently exists, e.g. Virtual Rescanning Module from SONOSCAN to capture the required

data, limitations in AMI resolution mean that only a few image slices are available. As a result, useful 3D solder bond profiles are difficult to obtain. By stacking the image slices from different impedance interfaces, a pseudo 3D image of solder bonds might be reconstructed.

4. *Feature Extraction*

Further work is required to expand the developed measurement technique from measuring just one solder joint feature, in this case crack plane diameter to multiple joint features. Suggested features within the ROI include:-

a. Shape of the crack plane area – This would provide indication on shear plane direction, joint movement and defect classification.
b. Pixel intensity data.
c. Crack plane, Z (Gap) dimensional profile information. This can only be obtained with 3D AMI inspection systems. Knowing the gap dimension would yield information on true existence of a crack, the magnitude of Z providing data on cyclic fatigue severity.

5. *Edge Effects*

Distortions occurring in the acoustic echo returns due to 'edge effects' arising from the silicon edge boundaries or more importantly the spherical nature of the solder bumps reduces the effectiveness of the metrology method proposed. Further work is required assessing the impact on the presented results. Overcoming some of these issues requires the development of new transducers and post processing algorithms as discussed in this thesis.

6. *Floor Plan Layout*

Additional work is required to understand and characterise the interactions between component characteristics and floor plan layout on reliability.

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Appendix A Test Board Configurations

Printed Circuit Board Configurations								
Surface Finish	ENIG		HASL Pb free		HASL Pb			
PCB Thickness (mm)	0.8	1.6	0.8	1.6	0.8	1.6		
Device Type	Package Type	Supplier part number	PCB identifier	Connection materials available				
				Pb	PB free			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U1	X				
ISSI - 1MB SRAM - Daisy Chain	TSOP 44L	Daisy chain test part	U2	X	X			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U3	X				
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U4	X	X			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U5	X				
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U6	X				
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U7	X	X			
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U8	X	X			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U9	X				
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U10	X				
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U11	X	X			
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U12	X	X			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U13	X				
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U14	X				
ISSI Test part 48B 8x10mm (Ball pitch 0.75mm)	FBGA	Daisy chain test part	U15	X	X			
Delphi - VSEP - electrical rejects	BGA	Mechanical Part	U17	X				
Delphi PSVI 8	Flip Chip	Functional Part	U19	X				
Delphi PSVI 8	Flip Chip	Functional Part	U20	X				
Delphi PSVI 8	Flip Chip	Functional Part	U23	X				
Delphi PSVI 8	Flip Chip	Functional Part	U26	X				
Delphi PSVI 8	Flip Chip	Functional Part	U27	X				
Delphi PSVI 8	Flip Chip	Functional Part	U28	X				
Delphi PSVI 8	Flip Chip	Functional Part	U31	X				
Delphi PSVI 8	Flip Chip	Functional Part	U34	X				
Delphi PSVI 8	Flip Chip	Functional Part	U35	X				
Delphi PSVI 8	Flip Chip	Functional Part	U36	X				
Delphi PSVI 8	Flip Chip	Functional Part	U39	X				
Delphi PSVI 8	Flip Chip	Functional Part	U40	X				
Delphi PSVI 8	Flip Chip	Functional Part	U43	X				
Delphi PSVI 8	Flip Chip	Functional Part	U46	X				
ISSI - 1MB SRAM	TSOP 44L	Daisy chain test part	U47	X	X			
ISSI - 1MB SRAM	TSOP 44L	Daisy chain test part	U48	X	X			
ISSI - 1MB SRAM	TSOP 44L	Daisy chain test part	U49	X	X			

Table A-1: Configuration of test boards

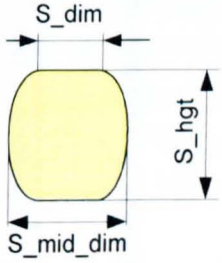
Appendix B Modelling Parameter Details

Printed Circuit Board	Young's Modulus [MPa]	24 500
	Poisson's ratio	0.15
	CTE [ppm/C]	12
Flip Chip	Young's Modulus [MPa]	260 000
	Poisson's ratio	0.23
	CTE [ppm/C]	7.8
Solder	Non-linear Properties	Sn52/Pb45

Table B-1: Summary of principle materials properties of test CBA

Level 1 Interconnect (Die to Die or BT attachment
Dimensions in [micrometers unless specified]

Ball	Yes
Column	N/A
wirebond	N/A
DieX	3948 micrometers
DieY	8898 micrometers
DieZ	725 micrometers
Ball size	Approx 7mils (177.8 micrometers)
S_dim	102 micrometers
S_mid_dim	140 micrometers diameter
S_hgt	125 micrometers
Bump Solder material (eg SAC	Sn=52.9%, Pb=45.9%, Cu= 1.2%
DiePitchX	Staggered see document dpPSVI8_Cap4_Stagger.doc
DiePitchY	Staggered see document dpPSVI8_Cap4_Stagger.doc
UBM dims	Bump Diameter (cap size) is 102um
UBM material	UBM stack is Al 4k, NiV 3.25k, Cu 8k , with Cu being on the top of stack.
Modulus E (GPa)	Range of values specified - 129.5, 168.0, 186.5
Poisson's ratio (n)	0.22 to 0.28
CTE (ppm/K)	2.6
Underfill	
material type	N/A
Modulus E (Mpa)	N/A
Poisson's ratio (n)	N/A
CTE (ppm/K)	N/A
Underfill_x	N/A
Underfill_y	N/A
Underfill_z (Die_att_z)	N/A



Note:
Flip Chip is a bare die device. No overmold material or underfill applied in finished test board.

PCB Cu Pad (**plen**)	0.3429	Staggered see document dpPSVI8_Cap4_Stagger.doc
PCB Cu Pad (**pwdth**)	0.1016	Staggered see document dpPSVI8_Cap4_Stagger.doc
PCB surface finish	Dependant on DKtestbd configuration ENIG, Pb or Pbfree	
PCBz	Dependant on DKtestbd configuration 1.6mm or 0.8mm	

Table B-2: Flip chip simulation data form

PCB Substrate Material Properties						
	Substrate z dimension (PCBz) = 0.8mm			Substrate z dimension (PCBz) = 1.6mm		
	PCB surface finish			PCB surface finish		
	ENIG	Pb HASL	PbFree HASL	ENIG	Pb HASL	PbFree HASL
Pre- Preg Material manufacturer/manufacturers material name	Ventec VT47			Ventec VT47		
Pre-preg weave	7628M x 4			7628M x 8		
Tg (degC)	180			180		
PCB - modulus of elasticity (e_en) N/mm2 or MPa	24500N/mm2			24500N/mm2		
PCB - Poisson's ratio (n)	0.15			0.15		
Pad - Poisson's ratio (n)	0.326			0.326		
CTE - PCB (ppm/K)	z=35x10-6, x=11x10-6, y=13x10-6, (in/in/c)			z=35x10-6, x=11x10-6, y=13x10-6, (in/in/c)		
CTE - Pad (ppm/K)	17 ppm/c			17 ppm/c		
Pad thickness	35 - 42 microns			35 - 42 microns		
Pad material	Cu with surface finish as above			Cu with surface finish as above		
Substrate x dimension	100mm, 5mm radius to corners			100mm, 5mm radius to corners		
Substrate y dimension	100mm, 5mm radius to corners			100mm, 5mm radius to corners		

Table B-3: Printed Circuit Board material characteristics

Appendix C Advanced Acoustic Imaging Techniques

Presented in this appendix is an accumulated body of work undertaken by the Electronic and Ultrasonic research team at LJMU under the leadership of Dr Guang-Ming Zhang and to which the author of this thesis was a contributor.

C.1 Introduction

Conventional acoustic micro imaging is a time domain imaging technique (TAMI). For thin/small packages, however, detection of the internal features and defects in the packages are approaching the resolution limits of AMI. As a result, the reflected echoes from internal features are superimposed, resulting in degraded ultrasonic images. One way to increase AMI resolution is to use high acoustic frequencies. However, higher frequencies provide less penetration through materials. A better alternative is to utilize digital signal processing methods to improve the resolution. Recently, acoustic frequency domain imaging (FAMI) has been introduced by Semmens and Kessler (Semmens, et al., 2002) where Fast Fourier Transform (FFT) algorithms were used to separate the reflected echoes into individual frequencies. Many anomalies can be imaged more meaningfully by FFT images, but frequency domain imaging will degrade or even fail if the reflected echoes are overlapped in the frequency domain. Several novel methods have been developed by Zhang, et al (Zhang, et al., 2004a) (Zhang, et al., 2005) (Zhang, et al., 2006a) (Zhang, et al., 2006b) to improve the resolution and robustness of AMI without increasing ultrasonic frequencies and are briefly described here.

C.2 Sparse signal representation based AMI

An ultrasonic A-scan signal can be modelled as a sum of the reflected ultrasonic echoes and gives the following when ignoring the noise

$$y = \sum_{i=1}^{M} c_i x_i \qquad \textit{Equation C-1}$$

Our goal is to infer both the reflection coefficients ci and the incident pulses xi according to the observed signal y, and then produce C-scan images. A four stage process for a sparse signal representation based AMI (SSRAMI) is proposed.

First, a-priori selection of a possibly overcomplete signal dictionary in which the ultrasonic pulses are assumed to be sparsely representable.

Second, separate the incident pulses by exploiting their sparse representation and thirdly selection of an appropriate echo. According to the frequency of transducer chosen and the interface to be investigated in the microelectronic package, we determine a time-frequency window. In the given window, we search for the time-frequency atom which has the biggest

decomposed coefficient. A resulting C-scan output is finally produced. We reconstruct the echo using the found time-frequency atom and its decomposed coefficient. The peak intensity of the reconstructed echo is displayed at its x-y position of C-scan image. Details of the techniques and experimental results were submitted to IEEE Trans on Advanced Packaging (Zhang, et al., 2006a).

In general, the ultrasonic A-scan y can be assumed to have a very sparse representation in a proper signal dictionary though not in the time domain. The problem of separating the ultrasonic pulses is therefore formulated as follows:

(P_0) Given the observed A-scan y and the overcomplete dictionary Φ, find the vector of coefficients in $c=\{c_i\}$ such that $y=\Phi c$ and c is as sparse as possible. In an overcomplete basis, the number of basis vectors is greater than the dimensionality of the input, the representation of an input is not a unique combination of basis vectors. Overcomplete representations have greater robustness in the presence of noise, can be more sparse, and can have greater flexibility in matching structure in the data. Several methods have been proposed to decompose signals in overcomplete dictionaries, including Basis Pursuit (BP) (Chen), Matching Pursuit (MP) (Mallat, et al., 1993), and Best Orthogonal Basis (BOB) (Coifman, et al., 1992), thus resulting in different implementation methods of SSRAMI.

C.3 Learning overcomplete representation based AMI

The construction/selection of dictionary Φ in the above SSRAMI is crucial in order that the atoms in Φ will be well matched to the ultrasonic incident pulse x_i in equation C-1. Many overcomplete dictionaries have been proposed, including wavelet packets (WP) and cosine packets dictionaries, Gabor frames, wavelet frames. In SSRAMI, we build Φ for the special application from these existing dictionaries by incorporating some prior information. However, we hope the atoms themselves to be adapted to x_i. Lewicki and Sejnowski (Lewicki, et al., 2000) proposed an algorithm for learning a dictionary by viewing it as probabilistic model of the observed signal. On the basis of the learning algorithm, learning overcomplete representation based AMI are proposed. Several overcomplete dictionaries for AMI signals are learned.

C.4 Acoustic time-frequency domain imaging

The basic concept of acoustic time-frequency domain imaging was described in (Zhang, et al., 2004b), and an implementation method based on continuous wavelet transform (CWT) was proposed. First, the received acoustic A-scans are decomposed into the time-frequency domain by CWT. The local maxima of the transform are then identified, resulting multi-scale edge representations of the A-scan. Threshold de-noising is further applied to the maxima to remove noise. Similar with SSRAMI, a time-frequency window is then determined in terms of the frequency of transducer and the interface to be investigated in the microelectronic packages.

Within the given window we search for the coefficients from the multi-scale edge representations, which are lying in the window and among them pick up the one with biggest coefficient value. Finally, the selected coefficient value is displayed at each x-y position to produce the C-scan image.

C.5 Example results

An example of synthesized ultrasonic A-scans, its amplitude spectrum, and time-frequency energy distribution are illustrated in figure C-1. For this A-scan the amplitude of either echo is affected each other due to overlap in time and frequency, so that TAMI likely produces a contaminated C-scan image when gating either echo. Similarly FAMI produces incorrect C-scans in these overlapped frequencies. However, two echoes are clearly separated in the time-frequency plane so that more accurate C-scans can be produced.

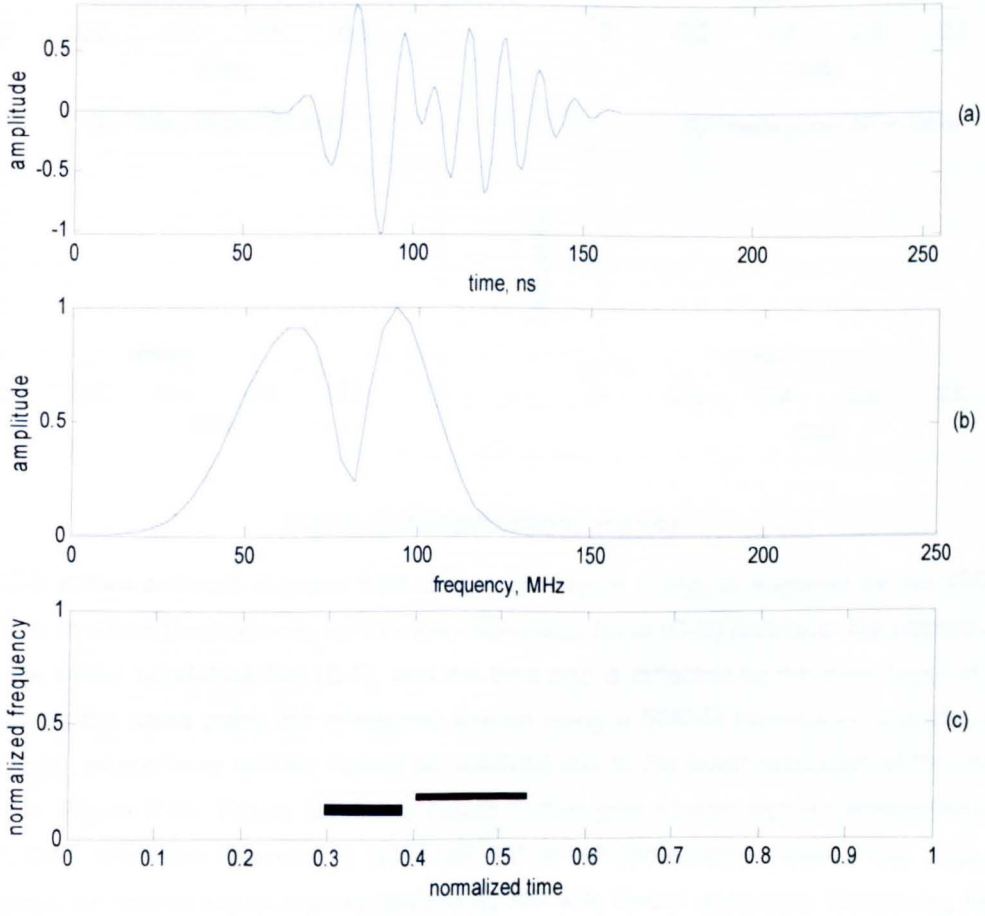


Figure C-1 Simulation result

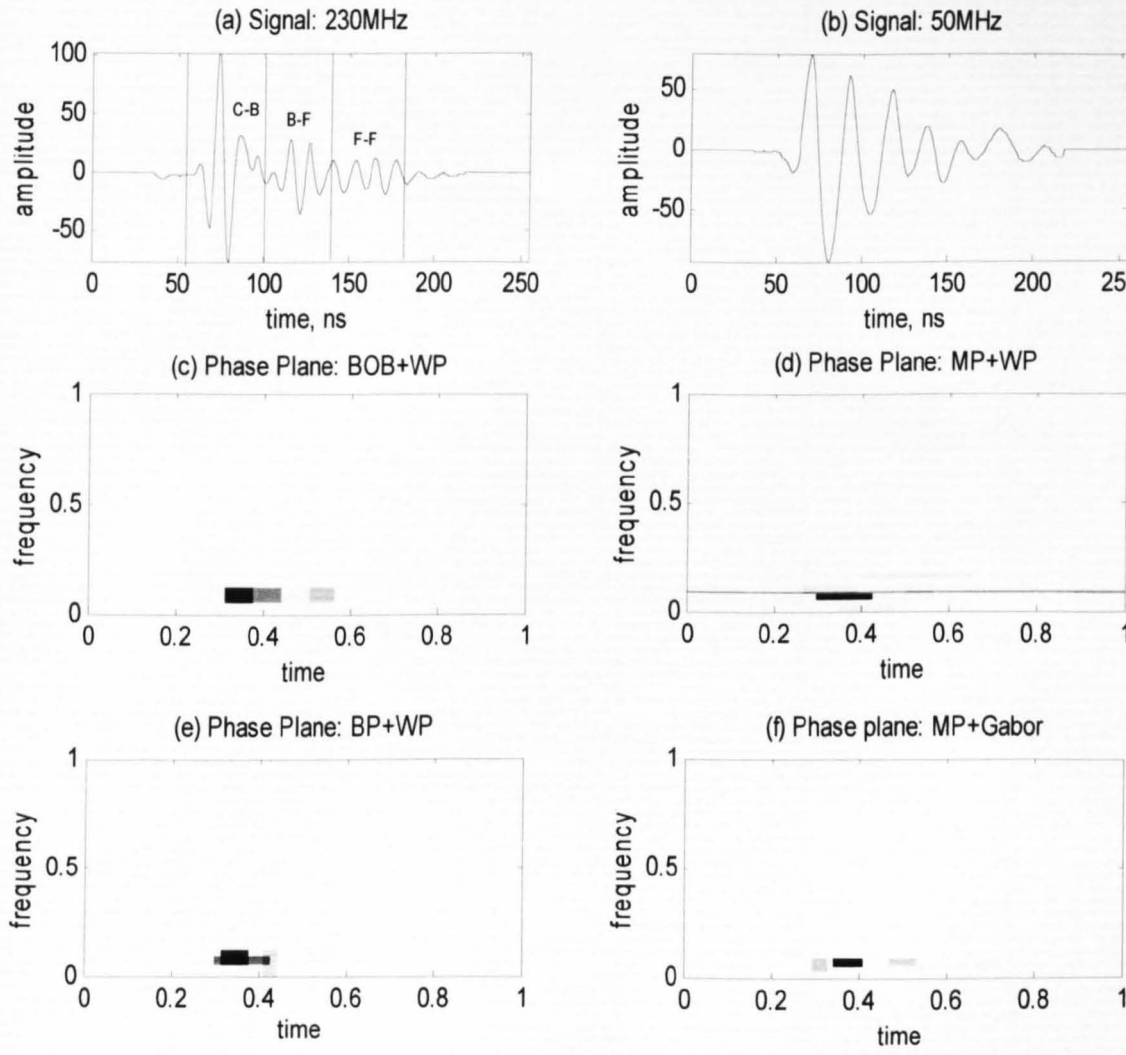


Figure C-2 Experimental results

Figure C-2 shows example A-scans from a flip-chip. Figure C-2(a) is acquired by the 230MHz transducer, in which the first echo is from the chip-solder bond (C-B) interface, the second echo is from the solder bond-thick film (B-F), and the third one is reflected by the other layer of thick film (F-F). At the same point, the measured A-scan using a 50MHz transducer is displayed in figure C-2(b), where three echoes cannot be resolved due to the lower resolution of the 50MHz transducer. Figure C-2c, Figure C-2d and Figure C-2(e) give sparse signal representations of Figure C-2(b), which are obtained by BOB, MP, BP in WP dictionaries, respectively. Figure C-2(f) displays the sparse signal representations by MP with Gabor dictionary. Comparing Figure C-2(a) with the resulting SSRAMI results in Figure C-2(c) to Figure C-2(f), it is observed that SSRAMI resolves these echoes in the low resolution 50MHz A-scan. Thus, SSRAMI can image the individual interfaces, improving the AMI resolution.

Parameters				A_{error}(%)		
A1/A2	*v2-v1*	*u2-u1*	*s2-s1*	SSRAMI	TAMI	FAMI
1.00	-0.08	48	0	4.42	0.00	47.41
1.00	0.10	48	0	4.39	0.00	55.04
1.00	0.15	36	0	1.83	0.42	11.63
1/0.8*	0.2	32	0	0.83	0.44	4.58
1/0.8	-0.3	28	5	1.92	13.38	0.00
1/1.5	-0.3	28	10	1.16	42.85	0.00
1/1.5	-0.3	20	15	3.32	60.60	0.00

Table C-1: The AMI results of simulated A-scans by different AMI techniques.

Table C-1 lists the evaluation results of imaging performance of TAMI, FAMI, and SSRAMI by amplitude error A_{error}, which is defined as $A_{error} = |A_{rec} - A_{theo}|/|A_{theo}| \times 100\%$, where A_{rec} is the peak intensity value of recovered echo by AMI techniques from gated A-scans, and A_{theo} is its theoretical value. Where parameters *A1* and *A2* are the amplitudes of two echoes separately, *v2-v1* determines the frequency separation of two echoes, and *u2-u1* determines the time separation (in sample number) of two echoes. The interface for C-scan imaging was set to the first echo by choosing gates as follows: for TAMI, the gate was chosen to centre at *u1*, with width equal to 32 samples. The time-frequency window was set to the Heisenberg box of the first echo. For FAMI, the centre frequency of the first echo is used as the imaging frequency, so A_{theo} and A_{rec} is the spectrum amplitude at this frequency. From Table C-1 it can be seen that SSRAMI is more stable, and gives more accurate results in most cases when compared to TAMI and FAMI. Some results have been published in (Zhang, et al., 2004a).

In summary, advanced AMI techniques have been proposed in previous research by Zhang, et al. including acoustic time-frequency domain imaging (TFAMI) (Zhang, et al., 2005), sparse signal representation based AMI (SSRAMI) techniques (Zhang, et al., 2006a), and learning overcomplete representation based AMI (LORAMI) techniques (Zhang, et al., 2005). These techniques improve the axial resolution and robustness of traditional AMI systems by employing acoustical time-frequency domain imaging with sparse representations of ultrasonic signals.

Appendix D Determination of Pixel Dimensions

Fully Imaged Die

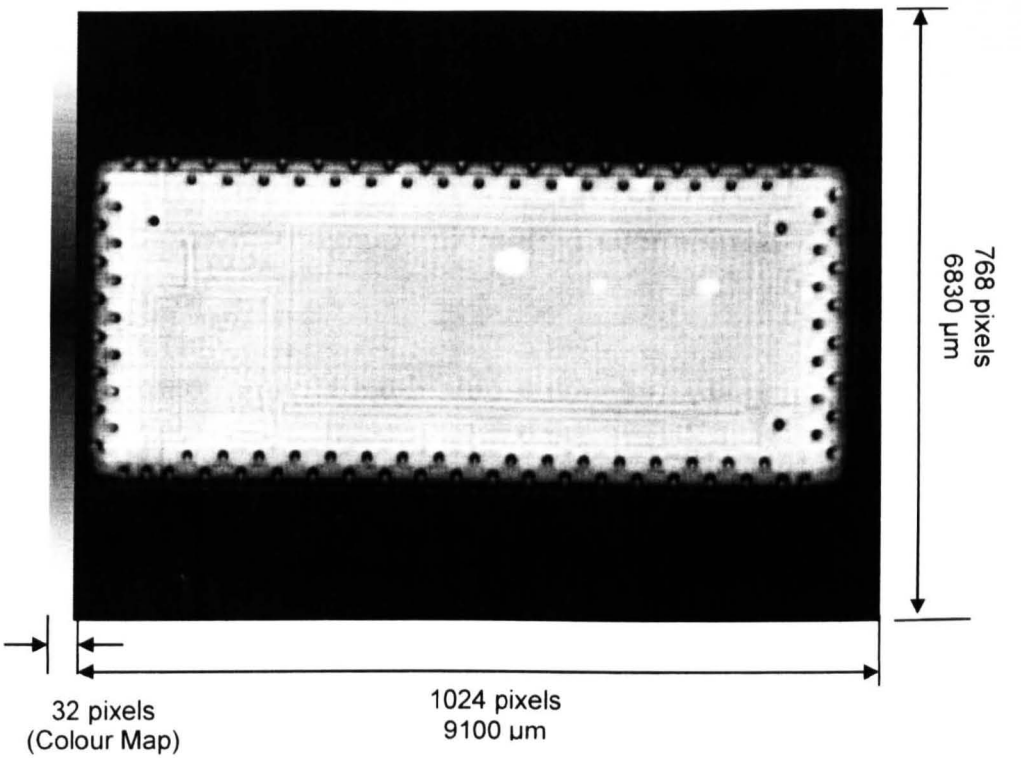


Image size = 1056 x 768

Actual image size without colour map = 1024 x 768

X-direction:-

1024 pixels = 9100 µm

1 pixel = 9100/1024 = 8.8867 µm

Y-direction :-

768 pixels = 6830 µm

1 pixel = 6830/768 = 8.8932 µm

Area per pixel = 8.8867 x 8.8932 = 79.03 μm^2

Appendix E Common Transducer Specifications

Transducer			Spot Size (mm)	Resolution (mm)	Depth of Focus
Frequency (MHz)	Focal Length (inches)	Diameter (inches)			
10	2.000	0.500	0.732	0.518	17.04
10	0.750	0.375	0.366	0.259	4.26
15	0.750	0.500	0.183	0.129	1.60
20	1.250	0.250	0.458	0.323	13.31
20	0.500	0.250	0.183	0.129	2.13
30	1.250	0.250	0.305	0.216	8.88
30	0.750	0.250	0.183	0.129	3.20
30	0.500	0.250	0.122	0.086	1.42
50	1.000	0.250	0.146	0.104	3.41
50	0.500	0.250	0.073	0.052	0.85
75	0.500	0.250	0.049	0.035	0.57
100	0.500	0.250	0.0366	0.0259	0.43
100	0.200	0.250	0.0146	0.0104	0.068
230	0.375	0.187	0.0160	0.0113	0.186
30	0.150	0.187	0.0064	0.0045	0.030

Table E-1: Resolution Data for Common Transducers (Courtesy of Sonoscan Inc.)

Appendix F DVD Data Archive

A companion DVD is submitted with this thesis, the DVD comprises of six folders, the contents of which is described below:

Electronic copy of thesis:

An electronic copy of the thesis in pdf format is stored in this folder.

Microsection results:

Archive for the SEM images of the sectioned components used in this research.

Miscellaneous:

Contains additional information on thermocouple location data for thermal profiling work undertaken and data labelling scheme for the Ultrasound and X-ray images.

Publications

Copies of listed publications

Simulation data and results:

Archive of all required modelling data and simulation results.

Ultrasound imaging results:

Archive of all ultrasound images acquired in this research.

X-ray imaging results:

Archive of all X-ray ultrasound images acquired in this research.