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Reliable time exponents for long term prediction of negative bias temperature instability by extrapolation

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***Abstract*— To predict the negative bias temperature instability (NBTI) towards the end of pMOSFETs' 10 years lifetime, power-law based extrapolation is the industrial standard method. The prediction accuracy crucially depends on the accuracy of time exponents, n. The n reported by early work spreads in a wide range and varies with measurement conditions, which can lead to unacceptable errors when extrapolated to 10 years. The objective of this work is to find how to make the n extraction independent of measurement conditions. After removing the contribution from as-grown hole traps (AHT), a new method is proposed to capture the generated defects (GD) in their entirety. The n extracted by this method is around 0.2 and insensitive to measurement conditions for the four fabrication processes we tested. The model based on this method is verified by comparing its prediction with measurements. Under AC operation, the model predicts that GD can contribute to ~90% of NBTI at 10 years.**

Index Terms—Negative bias temperature Instability (NBTI), BTI, aging, oxide traps, interface states, positive charges, lifetime.

I. INTRODUCTION

Designing reliable circuits has become more difficult in recent years and one of the constraints is the Negative Bias Temperature Instability (NBTI) in pMOSFETs. The initial investigation of NBTI can be traced back to 1960s [1]. The thick oxides (>50 nm) and low field (<3MV/cm) used in early works [1-2] prevent hole current flowing through the oxide. This 'intrinsic' NBTI follows a power law well, allowing its long term prediction by extrapolation, as recommended by JEDEC [3].

For thin oxides used in modern CMOS nodes, however, oxide field under typical NBTI stresses is high enough for hole current to flow through and charge the as-grown hole traps (AHT), in addition to interface state generation [4-12]. AHT causes NBTI kinetics deviating from power law [9-12], making prediction by extrapolation problematic. To restore the power law, a common practice is to introduce a delay between the stress and measurement [13, 14], during which NBTI partially recovers [6, 14-19]. Even if the test data can be fitted well with a power law after such a delay, the time exponent, n, depends on measurement speed [14, 20]. **Fig.1a** shows that the reported time exponent, n, has a wide spread [8, 17, 21-27], questioning the prediction accuracy when extrapolating based on these n values.

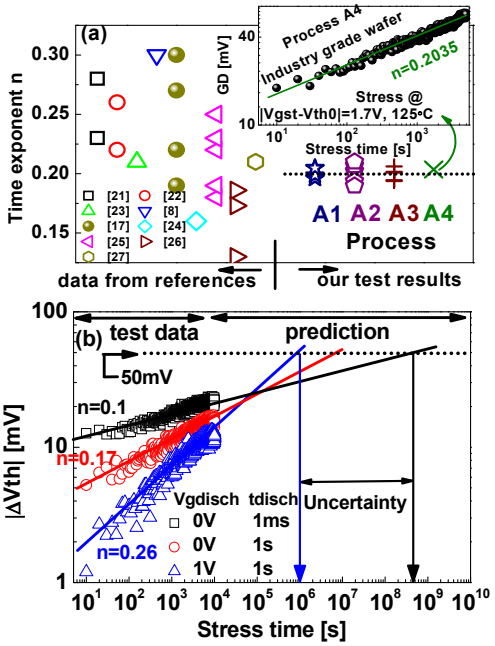

Fig. 1 (a) A summary of time exponents reported by early works and extracted using the method proposed in this work. Multiple points for each process (A1 to A4 in Table 1) represent the values from different stress voltage and temperature. The inset shows the kinetics for the industrial grade sample A4. **(b)** GD component measured by conventional method under different discharge voltage (Vgdisch) and time (tdisch). Different time exponents lead to substantial uncertainty in lifetime extraction when extrapolating to 50mV. The stress was under |Vgst-Vth|= 1.2V.

To extract the correct NBTI kinetics, the as-grown-generation (A-G) model has been proposed [12, 28]. This model divides defects into two groups: AHTs and generated defects (GD). AHTs are active in a fresh device, do not need an activation process, and remain the same after stress [9, 12, 28]. In contrast, the precursors responsible for GD are inactive in fresh devices, need stress-activation, and lead to an increase of defects after stress [9, 12, 28]. It has been proposed that these precursors can be hydrogen-related [2, 7, 29, 30].

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AHTs and GDs can be well separated based on their different energy locations: AHTs are below the top edge of Si valance band, Ev, whilst GDs are above Ev [12]. It is shown that filling AHT saturates typically within seconds [9, 12, 28] and, as a result, they should be removed from the aging kinetics. After removing the contamination by AHTs, **Fig.1b** shows that the GD can be fitted well with a power law. After the same stress, however, n varies with the GD measurement conditions, resulting in unacceptable errors in prediction through extrapolation.

For the first time, this work proposes a new test procedure that ensures capturing the total generated defects and demonstrates that it allows the reliable extraction of the time exponent and makes the extraction insensitive to the measurement conditions. We observed that the n is around 0.2 for all four fabrication processes used in this work, as summarized in **Fig.1a** for the processes A1-A4. We experimentally verify the prediction of the model based on this method and estimate that GD can contribute to ~90% of NBTI at 10 years under real use conditions.

II. DEVICES AND TEST PROCEDURE

To investigate the process dependence of n, pMOSFETs fabricated by four different processes from two suppliers are used and summarized in **Table 1**. They cover a wide range of samples: from processes under development to commercial processes, HKMG, and poly/SiON. Typical devices have a channel length and width of 1×1 μm. A1 was used unless otherwise specified.

Table 1 Test Samples

	A1	A2	A3	A4
Gate	Metal	Metal	Poly-Si	Metal
Dielectric	HK stack	HK stack	SiON	HK stack
EoT(nm)	1.45	1	2.5	1.2
Nodes(nm)	45	22	45	28

The test procedure is shown in **Fig.2**. After stressing under Vgst, an opposite polarity of gate bias (Vgdisch) was applied to accelerate the discharge of as-grown traps, as used in early works [31, 32]. The low use-bias under real operation Vgch (|Vgch|< |Vgst|) was then applied to refill all the traps that contribute under use condition. The pulse Id~Vg curves are recorded during each step with a measurement time of 3 μs. The threshold voltage degradation is monitored by sensing at a constant Id of 500nA*W/L around threshold voltage. Unless specified, the temperature is 125 ºC.

III. RESULTS AND DISCUSSION

A. GD component extraction

A typical result with the procedure in **Fig.2** is shown in **Fig. 3a**: the device was stressed under Vgst=-2.5V ('□') and then discharged under Vgdisch = +1.6V for 100 s. Vgdisch is properly selected to make sure there is no extrinsic degradation ('x'). The following Vgch= -1.2 V recharged the defects that are chargeable under use condition ('Δ'). To measure the AHTs, the same Vgch was also applied on a fresh device ('▽') in **Fig. 3b**. **Fig. 3b** clearly shows that more traps were filled after stress. These extra traps can only come from the new traps generated by the preceding stress. In **Fig. 3c**, subtracting the charging of fresh device from the stressed one shows that filling these generated traps saturates within 10s under Vgch=-1.2V.

Fig. 4a shows the energy distribution of defects in a fresh and then stressed device by using the profiling technique developed in [33]. Subtracting the fresh from the stressed one gives the distribution of GD component, as shown in **Fig.4b**. Clearly, GDs are located both within the Si bandgap and beyond Si conduction band. As observed in **Fig.3a**, charging-discharging can be cycled by alternating Vg polarity for the defects within the bandgap, so that they are referred to as cyclic positive charges (CPC) [7]. On the other hand, the defects above Si Ec are more difficult to neutralize and they are called as Anti-Neutralization positive charges (ANPC). What is worth noting is that the distribution in Fig. 4 originates from the oxide charge, rather than interface states. During the measurement, interface states remain constant since ΔVth was always taken from the Vg shift corresponding to a constant Id where the contribution of interface states to the charges change little during the measurement.

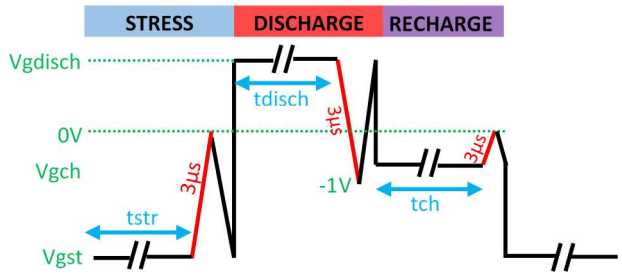

Fig. 2 The test follows a stress-discharge-recharge sequence. At the end of each step, ΔVth was monitored from a corresponding Id~Vg, which was taken from the 3μs pulse edge with Vd = -0.1V applied. ΔVth was extracted at a constant current of 500nA*W/L.

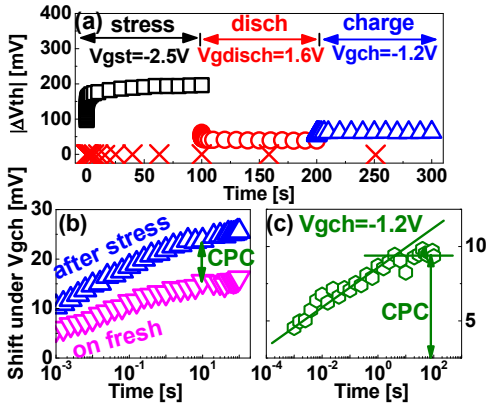

Fig. 3 (a) A typical result using a stress-discharge-recharge sequence. The symbol '×' are the result when Vgdisch=+1.6 V was applied directly on a fresh device, showing that Vgdisch itself causes little aging. **(b)** A comparison of charging kinetics under Vgch = -1.2 V before and after stress on the same device. The reference for the shift is the Vth of fresh device for the 'on fresh' data and the Vth at the end of Vgdisch period for the 'after stress' data. The difference in these two sets of data is caused by the stress-generated CPC as shown in **(c).** The saturation in (c) represents the completion of filling CPC. The EOT is 1.45 nm and the temperature is 125 ºC.

Early works often [8, 13, 14] extracted n after a delay during which NBTI partially recovered. If we measure ΔVth at the end of Vgdisch period, we obtain the ANPC. **Fig.5a** shows that ANPC reduces linearly against logarithmic discharge time [34]. This non-saturated discharge makes the measured ANPC discharge-time dependent and is the main challenge to the accuracy of n [8], as shown in **Fig.1b**. As a result, n should not be extracted from the ΔVth measured after an arbitrary delay and recovery.

To simplify the CPC and ANPC extraction, **Fig. 2** can be used: By using the Vth at the end of tdisch as reference, the Vth shift during tch was measured with and without inserting a stress period. Without the stress phase, this shift only contains AHT. When the stress phase is inserted, it contains AHT+CPC. To minimize device-to-device variation, the test with stress can be performed after the test without stress. CPC can be extracted from their differences. By definition, ANPC are the Anti-Neutralization Positive Charges, i.e. they are not neutralized at the end of discharge period, so that they equal to Vth(end of discharge)-Vth (Fresh).

When discharging time becomes longer, those traps with longer emission time leads to the linear increase of CPC against logarithmic time in **Fig. 5b**. This is because, by definition, CPC are the Cyclic Positive Charges, i.e. they can be refilled in the recharged period, so that they equal to Vth(end of recharge) – Vth(end of discharge). The total GD component, i.e. GD=CPC+ANPC in **Fig.5c**, is independent of discharging time. In addition, it is also independent of discharging voltage, Vgdisch, as shown in **Fig.5d**. **Figs.3b&c** clearly show that CPC are the generated defects, since they are taken from the increased ΔVth during recharge after stress when compared with that of fresh device. We cannot use this method to show that ANPC also are GD, as ANPC are not neutralized at the end of recovery period by definition and one cannot refill an already charged defect. To support that ANPC are generated by the same process as CPC, **Fig. 6** shows that they have the same thermal activation. Based on the common thermal activation of CPC and ANPC, on one hand, one may speculate that they have the same chemical structure and a variation of properties, such as bond length/angle, in amorphous oxides results in a distribution of energy levels. On the other hand, one may also speculate that they are different products of a common controlling aging process. Based on the past work, it is speculated that AHT is most likely originating from oxygen vacancies [35] and it has been reported that they can react with hydrogen species [36]. For instance, H_2 can be cracked by a trapped hole. Hydrogenous species are likely involved in the generation of both CPC and ANPC. For example, an increase of hydrogen exposure of the sample will significantly enhance the efficiency of CPC generation [37].

An apparent activation energy, Ea', can be extracted from **Fig. 6**. The Ea' for both CPC and ANPC is 0.14eV, much larger than the Ea' of ~0.04eV reported for AHT [39], supporting the defect generation is a different process from filling as-grown traps. The extracted Ea' of 0.14eV agrees well with the value reported by early works [38, 40]. What is worth noting is that since activation energy varies with different individual defect, the effective activation energy do not have intuitive physical meaning.

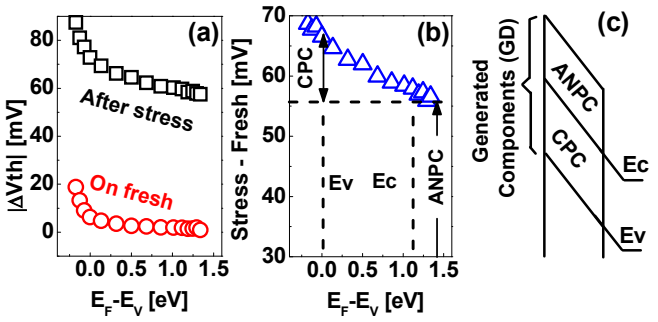

Fig. 4 (a) A comparison of the energy profiles before and after stress. **(b)** By subtracting the fresh profile from the stressed one, the profile for the GD was extracted. **(c)** Illustration of the energy range for the cyclic positive charges (CPC) and the anti-neutralization positive charges (ANPC).

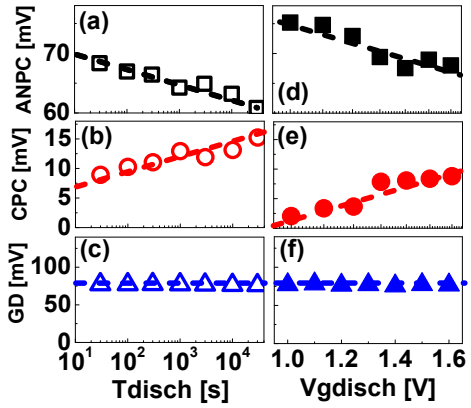

Fig. 5 Dependence on discharge conditions for **(a&d)** ANPC, **(b&e)** CPC and **(c&f)** GD=ANPC+CPC. The discharging voltage is +1.6V. Wherein, ANPC equals to Vth(end of discharge) – Vth(Fresh), CPC equals to Vth(end of recharge) – Vth(end of discharge) and GD is the sum of ANPC and CPC.

B. Intrinsic time exponent for the GD component

Once both CPC and ANPC are included in the GD, GD become independent of the measurement conditions, i.e. the discharge time and voltage. This lays a solid foundation for investigating its generation kinetics. As shown in **Fig. 7a**, the GD=(CPC+ANPC) follows power law relationship against time with n ~0.2. The impact of stress time range used for the extraction is further analyzed. Starting from 10s, the end-time varies between 100s to 20ks. **Fig. 7b** shows that, once the end-time exceeds 1ks, n becomes independent of the range used. The total stress time is kept within 3ks hereafter, therefore. What is worth noting is that if the test is performed under constant Vg, the widely-observed time-exponent decrease can be observed.

To study the dependence on stress conditions, GD are measured under different stress voltages and temperatures in **Figs.8a&b**. It is clear that n ~0.2 is independent of stress conditions. Next, the time exponent, n, are extracted from four different processes given in **Table 1**. The samples include both poly-Si/SiON and HKMG gate stacks, fabricated by different manufacturers, either during process development or used

commercially. The result is summarized in **Fig.1a,** along with the n reported by some early works [8, 17. 21-27]. The large spread of n between 0.13 and 0.3 reported by early works results from the dependence of ΔVth on measurement conditions, as illustrated in **Fig. 1b**. Once GD is independent of the measurement conditions, the spread of n is significantly reduced. For the four processes tested, n is around 0.2.

Early works [5, 41, 42] reported a reduction of n for longer stress under high temperature (up to 200 ºC [5] and 400 ºC [41, 42]). This could be caused by running out defect-precursors. The simultaneous annealing effect at the high temperature [43, 44] may also contribute to the reduction. Under the work temperature of 125 ºC and within the typical lifetime criterion (e.g. ⩽ 50 mV), **Fig. 8a** shows that there are sufficient number of precursors that aging follows the power law well.

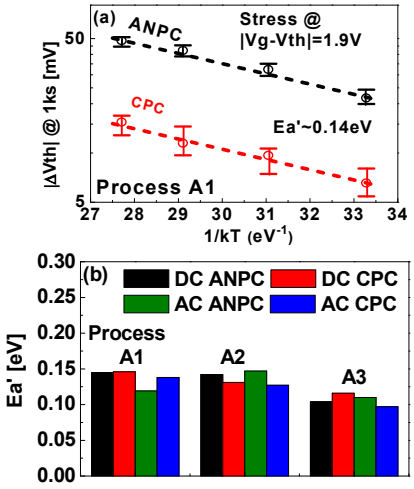

Fig. 6 (a) The effective activation energy extraction for CPC and ANPC for process A1 after stressed under DC |Vg-Vth0|=1.9V for 1ks. Wherein, CPC is taken from its saturated region in the recharge phased as illustrated in Fig.3c. 5 devices are used for each temperature and the error bar is given. The corresponding activation energy, Ea, can be obtained by Ea'/n = 0.7eV, where n is the time exponent obtained in Fig.7b. **(b)** The extracted Ea' from another two process: A2 & A3, under both DC and AC condition. Wherein, AC is with frequency of 10kHz and duty factor of 0.5.

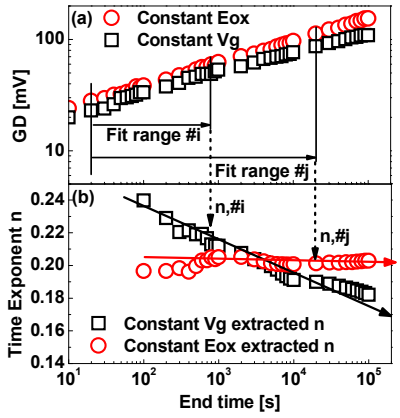

Fig. 7 (a) Kinetics for GD. **(b)** The extracted time exponent using data between 10s and variable end-time. The time exponent varies little after 10^3s for constant Eox stress, in which the overdrive Vg – Vth is kept constant during the test. If the test is carried out under constant Vg stress, a gradual reduction can be observed.

C. *Verify the prediction capability of the new method*

Although GD can be significant under high stress bias, it is typically too small for establishing reliable NBTI kinetics under low use-bias (e.g. Vg=-0.9V). The long term NBTI under low use-bias must be predicted by using the model established based on accelerated stresses, therefore. We now verify that the model extracted from the GD measured by the new method under high stresses can be used to predict the GD under low stresses.

The NBTI kinetics given by JEDEC [3] is,

$$GD = g0 * \exp(Ea'/kBT)(Vg - Vth)^m t^n \qquad (1)$$

Fig. 8 and **Fig.6** already confirm GD following power law against time and Arrhenius relationship. **Fig.9** shows that GD also follows a power law against overdrive voltage.

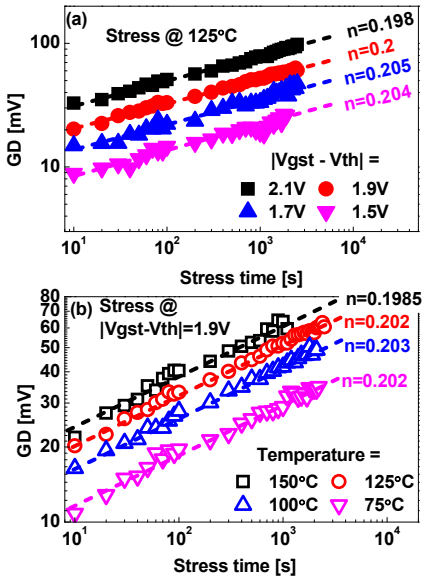

Fig. 8 Kinetics of GD component under different **(a)** stress voltages and **(b)** temperatures. The time exponent varies little around 0.2.

The GD measured by the new method under accelerated tests were used to extract g0, Ea', m, and n. **Eq. (1)** was then used to predict GD under low stress conditions and **Fig. 10** shows that the prediction agrees well with the directly measured GD. It should be pointed out the measured data in **Fig. 10** themselves were not used for extracting the parameters in **Eq. (1)**.

Finally, we point out that, in addition to GD, as-grown hole traps (AHT) also contribute to NBTI. The as-grown-generation (AG) model of NBTI is [12, 28],

$$\Delta Vth = AHT + GD \qquad (2)$$

It is of interests to assess the relative importance of these two components under real use-conditions. From a practical perspective, CMOS circuits operate mostly under AC conditions with frequencies between several GHz for processor core, 100's of kHz for L1 and scratchpad caches, and down to the kHz range for L2 and L3 caches [45, 46].

The similar Ea' and m from DC and AC stress condition shown in **Fig.6b** and the inset of **Fig.9** indicate that the GD degradation is mainly driven by the effective stress time [28] (i.e. stress time * duty factor). In **Fig.11a**, we measured the NBTI under AC (100 kHz) overdrive of -0.9V with a duty

factor of 0.5. The GD component under AC stress is predicted using **Eq. (1)**, as shown by the line in **Fig. 11a**. The predicted GD is lower than the measured ΔVth and their difference comes from the contribution of pre-existing traps. There are two supports for this claim. First, we measured the GD at the end of AC stress by using the new method and **Fig. 11b** conforms that they agree well with the prediction. Moreover, in **Fig. 11c**, the GD were measured after one week and they remain the same, so that no defect losses [41] were observed under current test conditions. Second, subtracting the predicted GD from the measured ΔVth gives a flat line in **Fig.11d**, indicating most of the pre-existing traps has been filled in seconds [9, 12, 28].

Although the rapid filling of pre-existing traps makes them larger than GD initially in **Fig. 11d**, at 10 years, **Fig. 11d** shows that GD reaches 27mV, while pre-existing traps at ~4 mV. As a result, GD can contribute to almost 90% of the total NBTI towards the end of device lifetime under practical AC use-conditions.

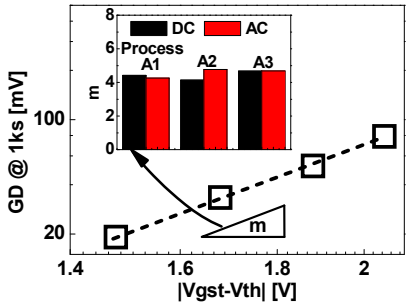

Fig. 9 GD follows a power law against Vg-Vth0. The data is taken from **Fig. 8a**. The inset shows the extracted m value for DC and AC stress conditions for the process A1, A2 and A3.

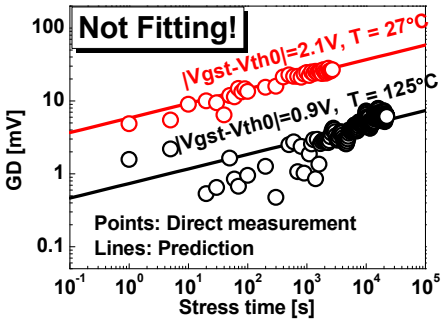

Fig. 10 Verification of the GD model. Prediction is by **Eq. (1)** and the measured data were not used for fitting the parameters in **Eq. (1)**.

IV. CONCLUSIONS

The time exponent, n, extracted by the conventional method varies with measurement conditions, leading to uncertainties in the long term prediction of NBTI through extrapolation. This work proposes a new method for measuring the total generated defects, including both cyclic positive charges (CPC) in Si bandgap and anti-neutralization positive charges (ANPC) above the Si conduction band edge. By adding CPC and ANPC together, it is shown that the total generated defects (GD) are independent of measurement conditions. It is found that GD can be well modelled with emperical power law relationshp against time and voltage. The time exponent extracted from the GD measured by this new method is found to be around 0.2 for four processes from different suppliers. Under practical AC use-conditions, it is shown that GD can contribute to nearly 90% of NBTI at 10 years, although it is lower than as-grown hole traps initially.

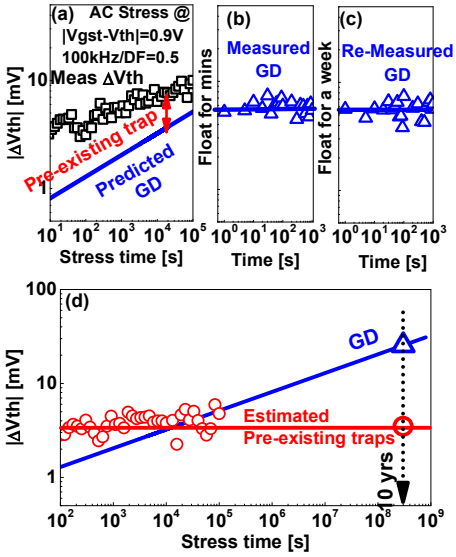

Fig. 11 (a) AC NBTI under low operation bias of (Vg-Vth)= -0.9 V with 100kHz and a duty factor of 0.5. The predicted GD agrees well with the measurement after AC stress **(b)** and after floating under 125°C for one week **(c)**. **(d)** A comparison of AHT and GD at different time.

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