Investigation of pre-existing and generated defects in non-filamentary a-Si/TiO_2 RRAM and their impacts on RTN amplitude distribution

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***Abstract* — An extensive investigation of the pre-existing and generated defects in amorphous-Si/TiO_2 based non-filamentary (a-VMCO) RRAM device has been carried out in this work to identify the switching and degradation mechanisms, through a combination of random-telegraph-noise (RTN) and constant-voltage-stress (CVS) analysis. The amplitude of RTN, which leads to read instability, is also evaluated statistically at different stages of cell degradation and correlated with different defects, for the first time. It is found that the switching between low and high resistance states (LRS and HRS) are correlated with the profile modulation of pre-existing defects in the 'defect-less' region near the a-Si/TiO_2 interface. The RTN amplitude observed at this stage is small and has a tight distribution. At longer stress times, a percolation path is formed due to defects generation, which introduces larger RTN amplitude and a significant tail in its distribution.**

***Index Terms*— a-VMCO, non-filamentary, RRAM, RTN, CVS, Pre-existing, Generated Defects, Mechanism, Read instability.**

I. INTRODUCTION

Resistive switching memory devices have attracted numerous attentions in the past decade and are considered as a strong candidate for next generations emerging memory technology [1-10]. There are mainly two types of transition-metal-oxide (TMO) based resistive switching devices (RRAM), the filamentary ones that can be made from a number of different materials, for example, HfO_2 [5], TaO_x [8], TiO_2 [9], etc.; and the non-filamentary ones such as PMCO [10], a-VMCO [2], or TiO_2/TaO_x [11]. Both types have been widely reported.

Resistance switching in filamentary RRAM has been attributed to the modulation of a conductive filament (CF) by external bias, especially in a localized CF constriction region [12]. This critical filament region has been identified by both modeling [12] and experiments such as the RTN based defect tracking technique [3]. It was found that defects moving into and out of the critical CF region lead to the switching in HfO_2 based devices [3, 13], and also lead to different modes of endurance failure [3, 14, 15]. It has been suggested that the endurance can be improved in Ta_2O_5 RRAM by tuning the oxygen chemical-potential profile along the filament [16], which is strongly correlated to the oxygen interaction with the bottom electrode. The large tail in read current distribution before and after the retention in filamentary devices, especially at high resistance state (HRS), however, is still a major concern, as it deteriorates the resistive switching window [17,18] and causes endurance and retention problems [19, 20]. This has been attributed to defects moving into/out of the constriction, where the least number of defects exist. The movement of individual defect to/from the constriction has significant impact on the overall resistance, and the stochastic nature of individual defect movement causes large resistance variability and large read instability [21, 22].

To overcome the above limitations in filamentary RRAM, novel non-filamentary RRAM devices have been proposed recently, in which the resistance switching is controlled through the uniform modulation of the defect profile at the interface either with the electrode [10] and/or between two dielectric layers [2]. Significant improvement in variability has been observed and attributed to the non-filamentary switching mechanism [11]. Vacancy Modulated Conductive Oxide (VMCO) RRAM is one such promising candidate, thanks to its advantages of low current operation down to low μA range, forming-free, and self-rectifying [2,7]. The a-VMCO RRAM device consists of two layers, with TiO_2 as the switching layer and amorphous-Si as the barrier layer. It shows the non-filamentary switching behavior as its resistance is inversely proportional to the area [24]. The resistance distributions at both HRS and LRS in a-VMCO RRAM show little tail-bits shifting, both before and after retention [2].

Compared to its filamentary counterpart, however, the switching and degradation mechanisms in non-filamentary a-VMCO cells are considerably less clear and little experimental evidence is available for the defects and their profile modulation, and for their correlation with the switching operation and reliability. In this work, the defects in non-filamentary a-VMCO RRAM have been investigated, with the focus on their impact on resistance switching (LRS/HRS) and stress-induced RTN distribution. Defects profiles are extracted during different stages of constant voltage stress (CVS), based on the RTN technique. Statistical analysis is carried out to characterize the RTN amplitude distribution. Significant differences have been identified between the pre-existing and generated defects and their impacts on device performance. This will provide insights into the operation and degradation of a-VMCO devices, assisting further improvements.

II. DEVICES AND EXPERIMENTS

The cross-bar a-VMCO device structure, as shown in **Fig. 1a&b**, was fabricated with CMOS-compatible process. The active stack is formed by an 8-nm PVD amorphous silicon (a-Si) barrier layer and, on top of which, an 8-nm ALD TiO_2 switching layer crystallized in anatase phase [2]. The a-Si barrier layer controls the current through the stack, and it also acts as a scavenger to introduce an oxygen vacancy (Vo) profile in the TiO_2 switching layer. The stack is sandwiched by a TiN bottom electrode (BE) and a TiN top electrode (TE).

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The typical DC I-V characteristics is shown in **Fig. 2a**, with the external bias applied on TE, and BE grounded. A ~10× window can be achieved, showing a gradual RESET/SET process without a current compliance. It has been suggested that the resistance is controlled by a uniform change of the overall defect profile, which modulates the bulk resistance, as illustrated in **Fig. 2b** [2]. This uniform modulation reduces the impact of individual defect and has improved the resistance variability significantly [2, 24].

In order to investigate the defects and their impact on resisitve switching operation, RTN measurements are carried out at incremental biases for both LRS and HRS. The typical RTN measurement procedure and results are given in **Fig. 3&4** [3]. Defect's location is extracted from the dependence of RTN's mean time constants on bias V_{TE}, based on the method adopted from refs [3, 4, 25-27]. Defects can be found in both TiO_2 and a-Si. RTN measurements are also inserted during the CVS stress to extract the defects induced by the stress, as shown in **Fig. 4**. RTN amplitude distribution is analyzed and evaluated statistically in both fresh and degraded devices.

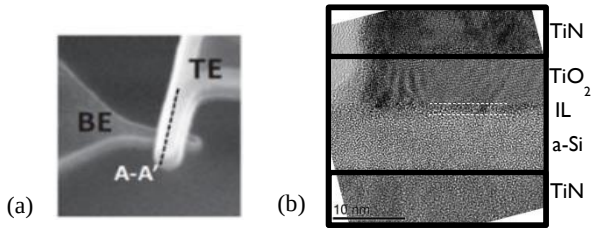


Fig. 1 (a) Top-view SEM image of a-VMCO RRAM cross-bar cell. (b) TEM cross-section of a smallest size (40nm) device. 1-nm SiOx interfacial layer (IL) is naturally formed between amorphous Si and anatase-phase TiO_2 by the end of the process.

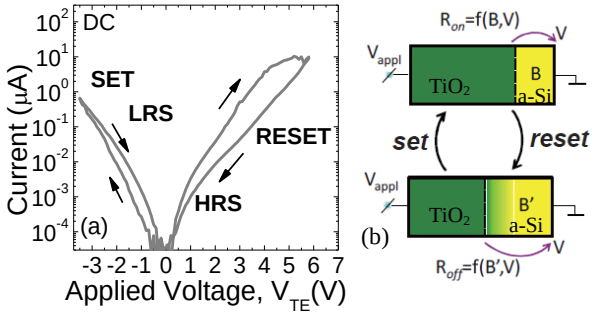
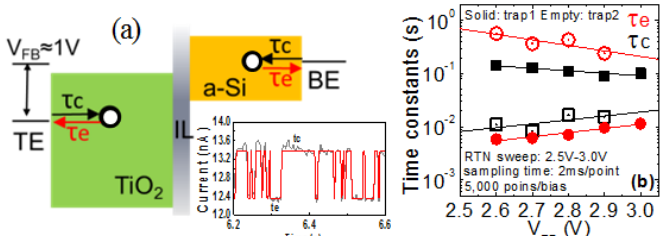


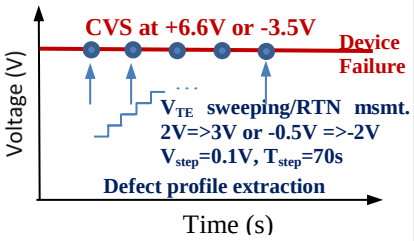
Fig. 2 (a) Typical I-V characteristics during the DC RESET and SET resistive switching. (b) Illustration of the switching mechanism proposed in [2].



$$X_T = \left[1 - \frac{k_B T}{q}\frac{d\ln(\tau_c/\tau_e)}{dV}\left(1+\frac{\varepsilon_{oxS}}{\varepsilon_{oxB}}\frac{T_{oxB}}{T_{oxS}}\right)\right]T_{oxS} + T_{oxB} \quad \text{(Eq.1)}$$

$$X_T = -\frac{k_B T}{q}\frac{d\ln(\tau_c/\tau_e)}{dV}\left(T_{oxB} + \frac{\varepsilon_{oxB}}{\varepsilon_{oxS}}T_{oxS}\right)T_{oxS} \quad \text{(Eq.2)}$$

Fig. 3 Typical RTN measurement procedure and results. (a) Energy band diagram and defect location measured from RTN. (b) Defect locations in TiO_2 (eq.1) and a-Si (Eq.2) are extracted from the dependence of RTN's mean time constants on bias V_{TE} by using the method adopted from refs [3,25-27]. Defects can be found in both TiO_2 and a-Si. RTN measurement bias, negative: -0.5V~-2V; positive: +2.0~3.0V. The mean time constants for high (τ_{high}) and low (τ_{low}) current levels in RTN are the capture (τ_c) and emission times (τ_e), respectively, extracted by using the HMM method [3].



Stress is applied at either 6.6V or -3.5V until device breaks down at a time scale ranging from tens to thousands seconds. Stress is interrupted at certain intervals to measure the RTN signals by incremental biases sweeping from 2V to 3V or -0.5V to -2V at a step of 0.1V. Each step lasts for 70 seconds.

Fig. 4 Test procedure for combined CVS and RTN measurements to extract the defects during the stress. V_{TE} during the RTN sweeping has the same polarity as the CVS stress.

III. RESULTS AND DISCUSSIONS

A. Switching mechanism and RTN in unstressed a-VMCO

Defects profiles are extracted at both HRS and LRS from the RTN signals in an unstressed a-VMCO device, as shown in **Fig.5a**. Defects exist in both TiO_2 and a-Si layers. At HRS, there is defects-'less' region at TiO_2 side of TiO_2/a-Si interfacial layer (IL), which does not exist at LRS, suggesting that defect profile modulation occurs predominantly at TiO_2 side of IL. **Fig. 5b** shows that the resistance states, represented by the read out current at V_{TE}=3V, are correlated well with the 'defects-less' region, as it becomes wider at HRS and narrower at LRS as illustrated in Fig.3c, confirming that the defect profile modulation in TiO_2 near the IL is responsible for the resistive switching,. This result provides direct experimental evidence for the proposed switching mechanism shown in **Fig.2b** [2]. Note that this defect profile modulation is caused by the movement of pre-existing defects, which have uniform spatial distribution in the lateral direction. This is supported by the forming-free and area-dependent non-filamentary switching characteristics as shown in refs [2, 7, 24].

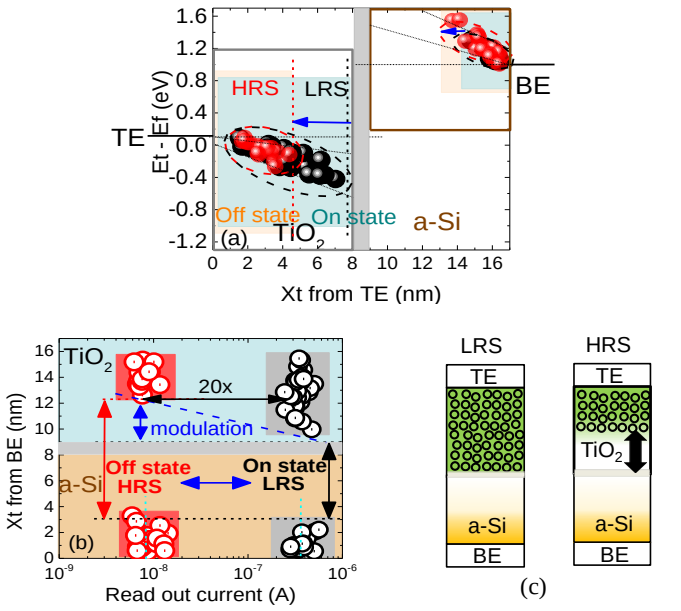


Fig. 5 Extracted defects profile at LRS ('●') and HRS ('●'). (a) the distribution of extracted defects in space (from TE) is plotted vs its energy level, and (b) vs resistance state by plotting X_T (from BE) vs. I_{read} measured at V_{TE}=3.0 V during the RTN measurement sweep. Defect profile modulation predominantly occurs in a defect-'less' region in TiO_2 near IL. (c) 'Defect-less' region becomes wider at HRS, resulting in higher resistance Note that this defect profile does not provide information on the actual defect density, as explained in detail in ref. [3].

To investigate the impact of defect profile modulation on device operation, the statistical distribution of the relative amplitude of RTN signals in unstressed a-VMCO cells is further examined, as large RTN amplitude could lead to large noise during the read operation, and reduce the resistance window. As shown in **Fig. 6a,** RTN amplitude at LRS is relatively small, with a median value of ~4%, and a relatively tight distribution with a maximum value of ~8%. At HRS, the median increases to ~8% and the distribution is shifted almost in parallel except the lower 10% percentiles. In comparison, RTN amplitude distribution in filamentary RRAM, such as in HfO_2 based RRAM devices [3, 5, 28], is significantly different, especially at HRS. Its RTN at LRS is much smaller and tightly distributed, while at HRS the distribution is much wider with a long tail at larger relative RTN amplitudes reaching 50%.

The above differences in RTN amplitude distribution is consistent with their different HRS variability observed in ref. [2, 7], supporting that the conduction and switching mechanisms in filamentary and non-filamentary RRAMs are different. In filamentary RRAM, conduction at LRS is metallic-like, with electrons hopping through a filament formed by oxygen vacancies, leading to very small variability and RTN signals [4]. At HRS, its resistance is controlled by the critical constriction region where the least number of defects exist. Movement and trapping/detrapping of individual defect within and near the constriction has significant impact on the current conduction, hence the much larger variability and larger RTN amplitude and its much wider distribution [28-30]. In contrast, the similarity between RTN distributions at LRS and HRS in non-filamentary RRAM suggests a similar conduction mechanism. The slightly larger RTN amplitude at HRS can be attributed to the slightly larger impact by trapping/detrapping since the defect profile is narrower in TiO_2 at HRS. The resistance variability and RTN amplitude at HRS is much smaller and tightly distributed than in filamentary RRAM, supporting that the impact of individual defect is significantly reduced due to the uniform defect distribution in a-VMCO device.

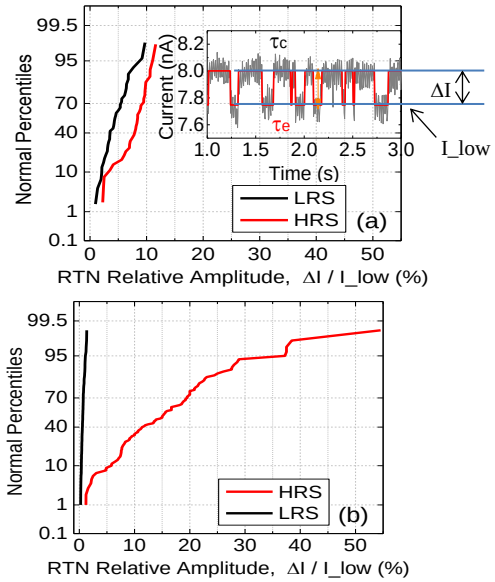


Fig. 6 Statistical distribution of the relative RTN amplitude at LRS and HRS under typical operation conditions in (a) non-filamentary a-VMCO RRAM device (Vread=3V, no compliance current is applied) and (b) HfO_2 based filamentary RRAM device with TiN/Hf(10nm)/HfO_2(5nm)/TiN structure [3]. (Vread= 0.1V, Vbias=0.1V~0.3V, Icc=100μA). Cycle-to-cycle variability is considered in both (a) and (b).

B. Degradation and RTN in stressed a-VMCO device

As shown in **Fig. 7a&b**, the a-VMCO device also features analog switching behavior. A higher RESET voltage, Vreset, can enhance the on/off resistance window by a factor of ×3, which is desirable for both digital and analog applications. The higher program voltage, however, may cause degradation in the memory cell and lead to earlier device failure. To investigate the degradation mechanism, a constant-voltage-stress (CVS) voltage, V_{stress}, is applied to the TE at either negative or positive polarity.

A typical current-time characteristics during the negative CVS is shown in **Fig. 8a**, where V_{stress}=-3.5V is applied on a fresh device, which leads to the memory cell set at LRS. The device exhibits a two-stage cell degradation process. The CVS current is stable in the 1st stage, and there is a large current fluctuation in the 2nd stage, before the device reaches the final failure. As shown in the inset of **Fig. 8a**, the stress induced CVS current fluctuation can be as large as 3~8 times of the initial current, which does not exist in the fresh device. This is a strong indication of stress-induced defect generation in the stack.

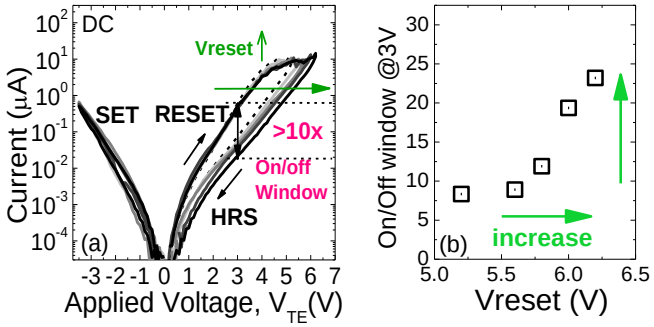


Fig. 7 (a) DC I-Vs of device switching at increased Vreset (b) Larger on/off window can be achieved by increasing the reset voltage.

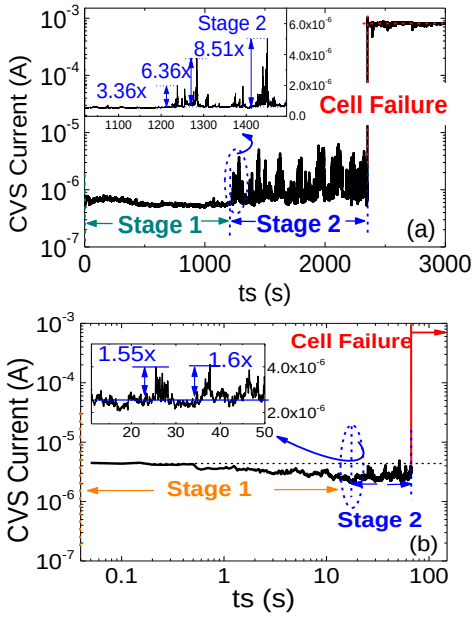


Fig. 8 Typical I-t characteristics in a-VMCO RRAM. (a) Negative CVS (Vstress=-3.5V) is performed on a fresh device at LRS. (b) Positive CVS (Vstress= +6.6V) is performed on an unstressed device at HRS. The inset is the zoom-in of I-t when large fluctuations start to occur. Local current fluctuation of 50% is used as a criterion to define the onset of the 2nd stage.

Fig. 8b shows that under a positive CVS, V_{stress}=+6.6V, which leads to the memory cell reset at HRS, the two-stage cell degradation process can also be observed. The slight CVS current reduction in the 1st stage is caused by the further reset process, and the large CVS current fluctuation in the 2nd stage also indicates defect generation during the cell degradation.

RTN measurements are inserted during the CVS following the test procesure shown in **Fig. 4**, in order to investigate the impact of device degradation on RTN amplitudes. **Fig. 9a-d** show the measured RTN signals during the negative CVS. RTN amplitude in the 1st stage is small at ~4%, as shown in **Fig. 9b**. This is consistent with the results in devices at fresh LRS state, as shown in **Fig. 6a**. In the 2nd stage, however, RTN signals with both small and large amplitudes are observed, at ~4% and ~12%, respectively, as shown in **Fig. 9c&d**. Statistical analysis of the RTN amplitude against the measurement bias during the 1st and 2nd stages of negative CVS are shown in **Fig. 10a&b**, respectively. It confirms that a larger range of relative RTN amplitudes, including both small and large RTNs varying from 2% to 40% are observed in the 2nd stage, while only small RTNs with amplitudes less than 10% are observed in the 1st stage. Similar observations are also found during the positive CVS, as shown in **Fig. 10c&d**.

It has been observed in MOSFETs that defects are generated in gate dielectrics under the NBTI/PBTI stress following an exponential law kinetics. It is likely that in a-VMCO devices the large CVS current fluctuation, as shown in **Fig. 8**, and the large RTN amplitudes, as shown in **Fig. 10b&d**, in the 2nd stage of CVS are correlated and both are caused by progressive defect generation. In the 1st stage, the defect generation is less important and the small noises are mainly originated from the trapping/detrapping of the pre-existing defects. In the 2nd stage, as the number of generated defects increase, local percolation conduction paths are gradually formed, and trapping/detrapping from which leads to large noises, alongside with small noise signals from those defects not located in the percolation paths. This speculation is supported in **Fig. 11a&b**, where the CDF distributions of RTN amplitude exhibit long tails at large RTN amplitude in the 2nd stage, similar to that in the filamentary devices at HRS shown in **Fig. 6b**, indicating formation of filamentary percolation conduction path. There also exist small RTN amplitudes overlapping with that in the 1st stage.

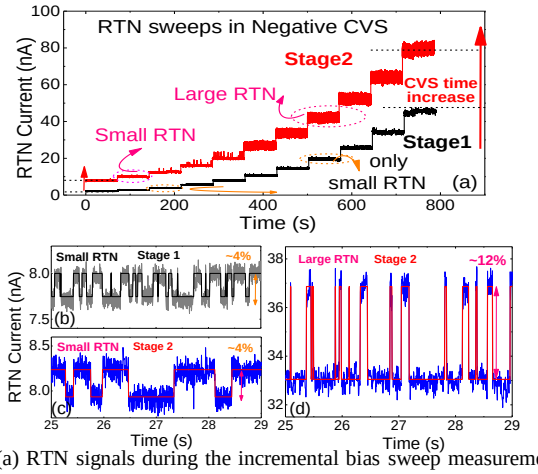


Fig. 9 (a) RTN signals during the incremental bias sweep measurements inserted during the negative CVS. (b) RTN signal during stage 1: only RTNs with small amplitude are observed. Both small (c) and large (d) RTNs are observed in stage 2.

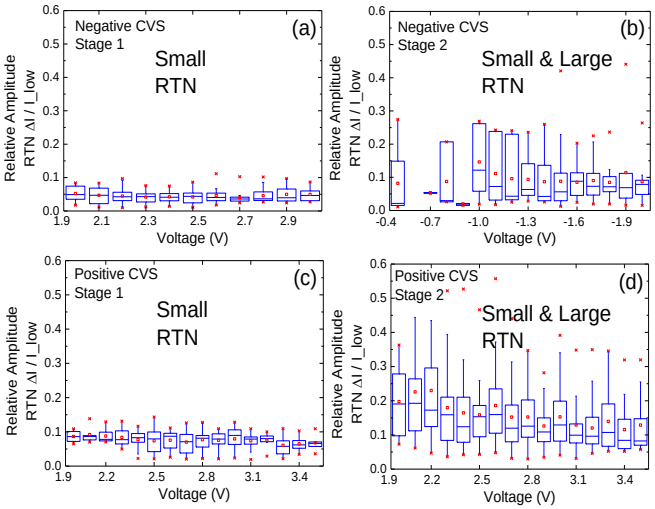


Fig. 10 Statistical analysis of the relative RTN amplitude dependence on the measurement bias during (a) & (b) negative and (c) & (d) positive CVS in a-VMCO during the 1st and 2nd stage.

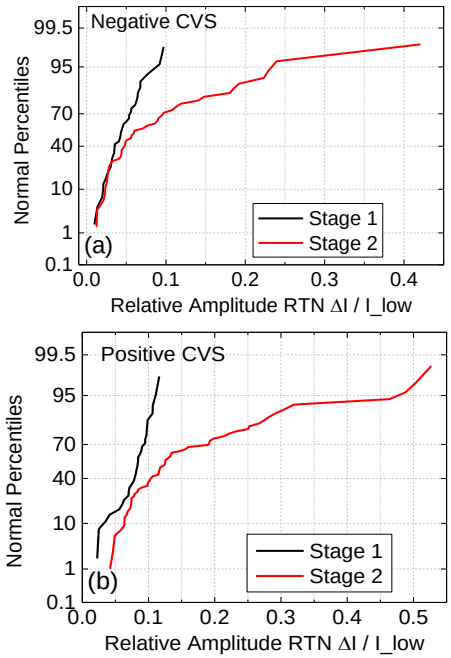


Fig. 11 CDF plot of the relative RTN amplitude distribution during the 1st and 2nd stage of (a) Negative and (b) Positive CVS.

C. Generated defects and percolation path in 2nd CVS stage

In order to provide direct experimental evidence to confirm the percolation current path formation in the 2nd stage during CVS, induced by defect generation as we speculated in Section III-B, defect locations are extracted from the small RTNs in the 1st stage and from the large RTNs in the 2nd stage, respectively, during the positive CVS, as shown in **Fig. 12a**, and the negative CVS, as shown in **Fig. 12b**.

During the positive CVS, the a-VMCO device is reset at HRS, i.e. the off state. The profile of the defects extracted from the small RTNs in the 1st stage is represented by the orange rectangle in the background of **Fig. 12a**. Since there is a wide defect-'less' region near the IL at HRS, there is no percolation current path formed

across the stack in this stage. During the 2nd stage, however, the defects extracted from the large RTNs show a different profile, which not only overlaps with that in the 1st stage, but also approaches the IL region across the TiO_2 layer, as shown in **Fig. 12a**. Before the final failure occurs, the complete percolation path is expected to be formed across the entire stack and leads to the hard breakdown. This suggests that the 'defect-less' region in a-Si is the last stronghold of the dielectric stack before the device's final failure. To note, the cell becomes fragile but still has memory functionality during the 2nd stage before failure. It should also be noted that the conduction currents in the 2nd stage are not increased from the 1st stage despite the large fluctuation and noise amplitude, indicating that the dominating conduction mechanism remain the same in the 2nd stage, i.e., the electron tunneling through defects.

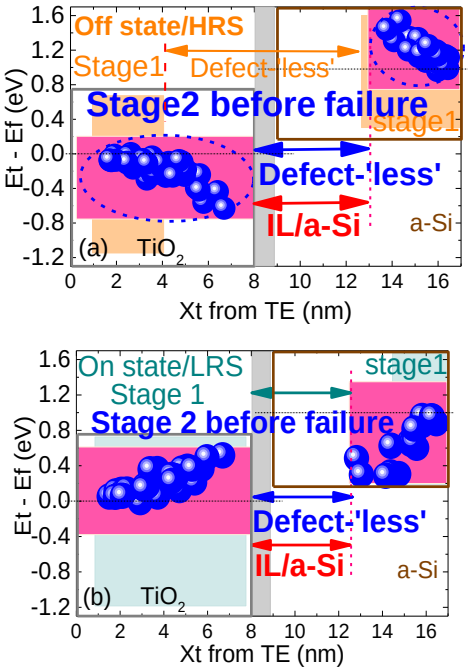


Fig. 12 Percolation path formation by defects generation in the 2nd stage of (a) positive and (b) negative CVS, in addition to the pre-existing defects observed during the 1st stage. The defect-'less' region in a-Si is the most robust region. Large noises observed in the 2nd stage are originated from the trapping/detrapping of defects along the percolation path, especially within and near the defect-'less' region, similar to those within and near the constriction region of the filamentary devices. It should also be noted that the difference in defect energy positions in (a) & (b) is caused by different energy scanning regions during RTN measurements with different polarities (Fig.4).

During the negative CVS, the a-VMCO device is set at LRS, i.e. the on state. The profile of the defects extracted from the small RTNs in the 1st stage is represented by the light blue rectangle in the background of **Fig.12b**. Although there is no defect-'less' region in TiO_2 near the IL at LRS in the 1st stage, the density of pre-existing defects is not high enough to form a percolation current path across the stack, which can only lead to small noises. During the 2nd stage, the defects extracted from the large RTNs show that the defects are generated across the TiO_2 layer, in addition to the pre-existing defects, as shown in **Fig. 12b**, which form a percolation current path and lead to large noises. Defects are generated across the stack, including a-Si and IL at the final stress stage, and a complete percolation path is expected to be formed, leading to the final hard breakdown. In fact, both pre-existing and generated defects should contribute to the percolation path formation in the 2nd stage, as both the small and large RTNs are observed in the 2nd stage, as shown **Fig. 9&11.**

The striking similarity in the CDF distributions of RTN amplitudes between the unstressed filamentary device at HRS (**Fig. 6b**) and the stressed non-filamentary devices in the 2nd CVS stage at both HRS and LRS (**Fig.11a&b**) also provides strong supporting evidence for the percolation formation in a-VMCO. Large noises observed in the 2nd CVS stage in a-VMCO are originated from the trapping/detrapping of defects along the percolation path, especially within and near the defect-'less' region, which is similar to the filament and its constriction region in the filamentary devices. The quality of the defect-'less' regions around the interfacial layer region is, therefore, critical to a-VMCO device performance. A poorer a-Si/TiO_2 interface quality could introduce large read noises and lead to earlier failure. This may explain the smaller current oscillations in the 2nd state at HRS in Fig.8 where the defect-'less' region widens and improves the interface quality. According to the results, improvement of the a-Si/TiO_2 interface quality should lead to better a-VMCO device performance.

It has been demonstrated in this work that the resistive switching in a-VMCO devices is controlled by the profile modulation of pre-existing defects near the IL. The a-Si layer acts as an oxygen scavenging layer to provide a profile of defects in the TiO_2 layer in the form of oxygen vacancies. The defect profile can be modulated by the external bias, as the reset occurs in the bias between +5V and +6V, while the set occurs at around -3 V. The difference in set and reset bias may be partially due to the 1 V flatband voltage as shown in Fig.3 [7] and partially due to the asymmetric dual-layer structures. Detailed mechanism of defect movements in the stack are subject to further investigations. The reduced impact from individual defect of non-filamentary switching leads to much smaller resistance variability and read instability in unstressed a-VMCO device [31]. The large read instability induced by defect generation and percolation path formation in severely stressed devices could be improved by further material and structure optimization, especially around the interfacial layer region [32-36]. This work provides insightful guidance for further process and device structure optimization of a-VMCO device.

IV. Conclusions

The pre-existing and generated defects in amorphous-Si/TiO2 based non-filamentary a-VMCO RRAM devices has been investigated in this work based on the random-telegraph-noise technique. The non-filamentary switching mechanism has been identified. It is found that the switching between the low and high resistance states are correlated with the profile modulation of pre-existing defects in the 'defect-less' region near the a-Si/TiO_2 interface, and the non-filamentary switching leads to much smaller read instability at HRS than that in the filamentary RRAM devices. The degradation mechanism under constant-voltage-stress is also identified. Defect generation induced percolation path formation is experimentally observed and correlated with the larger RTN amplitude and wide distribution in the stressed device. The quality of the IL region is expected to play a critical role in memory cell performance. This work will assist in further development and optimization for the non-filamentary a-VMCO RRAM device.

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