As-grown-Generation (A-G) Model for Positive Bias Temperature Instability (PBTI)

Rui Gao, Zhigang Ji, *Member, IEEE*, Jian Fu Zhang, John Marsland and Wei Dong Zhang

***Abstract*— Positive Bias Temperature Instability (PBTI) is poised to cause significant degradation to nFETs with deep scaling into nanometers. It is commonly modelled by a power law fitted with measured threshold voltage shift. For the first time, this work shows that such models do not warrant PBTI prediction outside the stress conditions used for the fitting. The underlying cause for this failure is the errors in the extracted power exponent. Based on the understanding of different types of defects, we develop a robust As-grown-Generation (A-G) model and demonstrate its capability for accurate prediction of PBTI under both DC and AC conditions. The generation-induced degradation is found to play a key role. Analysis reveals that, although PBTI is usually smaller than NBTI within the typical test time window, it can exceed NBTI by the end of device lifetime.**

Index Terms—PBTI, NBTI, electron traps, HKMG, Reliability

I. INTRODUCTION

Ageing has become a critical concern for CMOS technologies as scaling is reaching nano-scale regime [1-8]. Thorough examination and certification of reliable operation throughout the entire application lifetime is required during design. Emerging applications like the Internet of Things (IoT) or wearables usually require strict resiliency and long lifetimes [9]. For example, some biomedical applications require a lifetime of more than 50 years for medical implants. An accurate long-term lifetime prediction is the ultimate task of ageing evaluation.

Bias Temperature Instability (BTI) has been considered as one of the important ageing mechanisms. Extensive efforts have been made in investigating the Negative Bias Temperature Instability (NBTI) for pFETs. The recent use of the multi-layer gate material, however, has led to considerable Positive Bias Temperature Instability (PBTI) for nFETs [1-8]. From the application perspective, it has been reported that PBTI can be the dominating reliability issue for Field-Programmable Gate Arrays (FPGAs) [10] and Ring Oscillators (RO) [11].

Despite industry-wide characterization of various aspects of PBTI phenomena and general consensus regarding its empirical features [1-11], the detailed mechanism of the degradation is not fully understood. Charging of pre-existing traps and/or generating new traps in the dielectric are considered to be the root of PBTI [12]. Due to the lack of well-accepted PBTI model, the classic power law as described in Eqn (1) is widely used for lifetime prediction [13], where A, m and n represent the pre-factor, voltage and time exponents, respectively.

$$\Delta V_{th} = A \cdot V_{gov}^{m} \cdot t^{n} . \quad (1)$$

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One set of typical PBTI results with different stress gate bias, Vgst, and measurement delays are shown in **Fig.1a**. It is clear that PBTI depends on both Vgst and the delay between stress and measurement. The time exponents are extracted and plotted in **Fig. 1b**. When measured with 1 ms delay, the time exponent declines as voltage increases [1], making it impossible for predicting the long term PBTI under real use conditions [14].

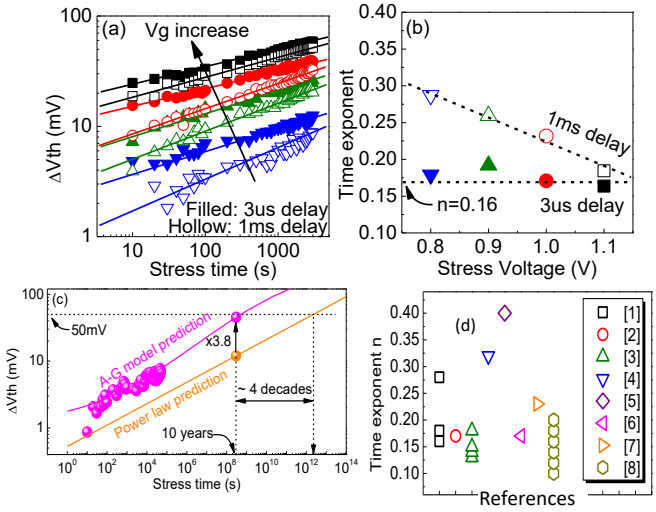

Fig. 1. (a) A comparison of PBTI under accelerated stress with 1 ms and 3 µs measurement delay. ΔVth is monitored at sensing drain current close to Vth. The symbols are test data and the lines are fitted with power law. **(b)** The fitted time exponents. **(c)** A comparison of test data (symbols) with prediction by the model extracted from the filled symbols in (a) (the lower line) and from the A-G model proposed in this work (the upper line). **(d)** A summary of PBTI time exponent reported by early works [1-8].

The apparent time exponent is close to a constant, when measurement delay is minimized to 3 µs. However, the classic power law model extracted from these data failed to predict the PBTI even just 0.1V below the lowest Vgst used for model parameter extraction, as shown in **Fig.1c**. When fitting the measured ΔVth, the uncertainties for the time exponent reported by early works in **Fig.1d** [1-8] do not warrant prediction. There is a need for a test-proven method to characterize and model PBTI induced degradation, enabling reliable prediction.

The central objective of this work is to develop a model for long-term PBTI prediction under both AC and DC operation conditions. By separating different types of defects and understanding their kinetics, the proposed model provides excellent predictive capability. The model is then used to assess the long-term PBTI under real use conditions. It is found that the lifetime for DC PBTI can be overestimated by 4 decades by the model extracted from the filled symbols in **Fig.1a**, as shown in **Fig.1c**. In addition, although PBTI-induced degradation can be smaller than NBTI within typical test time window, we will show that long-term PBTI can overtake NBTI.

The paper is organized as follows: The details of devices and experiments are described in Section II. Section III shows how different types of defects can be experimentally separated. Based on the extracted kinetics for each type of defect, the A-G model for PBTI is proposed and validated under both DC and AC operation conditions in Section IV. Section V discusses the long-term PBTI-induced degradation under real use conditions and Section VI concludes this paper.

II. DEVICES AND EXPERIMENT

nFinFETs fabricated using a Hf-based high-k oxide stack and a metal gate are used to demonstrate the proposed model. An equivalent oxide thickness of 1 nm was obtained by adopting a thin TiN metal gate, inducing Si in-diffusion, and reducing the interfacial oxide thickness [15]. Fast measurement of Id-Vg within 3 μs on Keysight B1530 is used in this work [16]. The threshold voltage degradation is monitored by sensing at a constant Id of 500nA*W/L around threshold voltage. Unless otherwise specified, temperature is 125 °C.

Although PBTI is considered as an electric-field driven phenomenon [17], the tests in literatures were usually performed under constant Vgst against stress time. The underlying assumption is that the total degradation, ΔVth, is much smaller than the applied voltage and thus the change in electric field over the dielectric, Eox, during the stress can be neglected. **Fig.2** compared the PBTI degradation under the constant-Vgst and constant-Eox condition. The constant-Eox is maintained by adding ΔVth measured in the last step to the Vgst(time=0). Although the difference in Fig.2 is small initially, it becomes considerable as the ΔVth increases for longer stress time. In this work, tests were carried out under constant-Eox, unless otherwise specified.

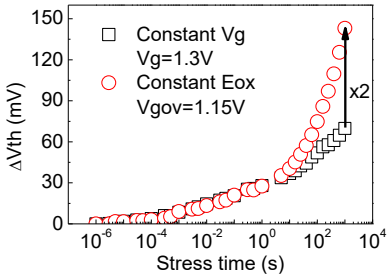

Fig. 2. A comparison between constant Vgst and constant Eox stress for PBTI.

III. DEFECTS UNDER PBTI STRESS

There is no consensus on the defects and mechanisms of PBTI. Some groups ascribe the degradation to filling pre-existing electron traps, such as oxygen vacancies in the high-k layer [18]. Other groups proposed that stress-induced defect generation may also makes considerable contribution [13,19,20]. In order to model PBTI, it is important to separate different types of defects and model the kinetics of each type separately. In the following, we will show that through separating different types of defects experimentally, accurate PBTI model with predictive capability can be extracted.

A. Generated Defects (GD): characterization and modelling

For NBTI, it is reported that GD can depend on measurement conditions (e.g. discharging time, Tdisch, and the discharge voltage, Vgdisch) [21]. This is also the case for the GD induced by PBTI. One example is shown in **Fig.3**: if different Tdisch/Vgdisch is used, the extracted GD kinetics varies. For NBTI, this is because not only as-grown traps, but also some GDs, are discharged [21]. By applying the Stress-Discharging-Recharging (SDR) technique, the discharged GDs are refilled, allowing all GDs being captured. Using all GDs obtained in this way, a reliable power law is obtained, which is independent of measurement conditions [21].

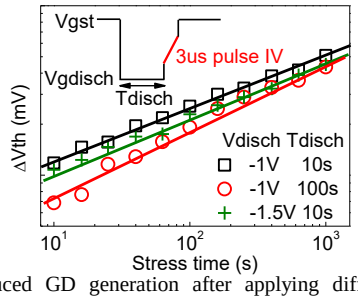

Fig. 3. PBTI-induced GD generation after applying different discharge voltage, Vgdisch, for different discharge time, Tdisch. The waveform for the measurement is shown in the inset.

In this work, the SDR technique is applied for PBTI with the waveform shown in **Fig.4a**. The details about this technique can be found in [21]. As shown in **Fig.4b**, the dependence of GD extraction on Vgdisch and Tdisch are removed with SDR.

To study the dependence on stress conditions, GD were measured under different stress overdrive voltages, Vgov=Vgst-Vth. As in **Fig.4c**, they are well described by,

$$GD = g_1 \cdot V_{gov}^{m1} \cdot t^{n_1}. \quad (2)$$

It is worth of noting that the extracted GD has a Vgov-independent time exponent of 0.32. This is larger than that extracted from the total ΔVth in **Fig.1a** and most of the values reported by early works [1-8] in **Fig.1d**. It is also larger than the ~0.2 reported for NBTI [21]. From a circuit point of view, the large time exponent for PBTI can impact the long-term reliability, as will be further elaborated in Section V.

The atomic structure of GD remains unknown and the electrical measurement used here does not give direct information on it. To test if GD is interface states, we study the sub-threshold swing (SS) against stress time. An increase in SS is considered as an indicator for interface states and/or border traps generation [7,22]. As shown in **Fig.5a**, with a substantial GD, there is little change in the SS. This indicates that the GD is oxide traps, rather than interface states.

To further explore the defects responsible for GD, **Fig.5b** shows that GD and stress-induced-leakage current (SILC) have the same time exponent. This strong correlation supports that they originate from the same generation process. It is reported that the defects responsible for the intrinsic breakdown are the generated electron traps, rather than hole traps [23]. Hydrogenous species has been proposed to cause the generation [24] and one may speculate that the generated defect contains hydrogen. Whether it contains hydrogen before the generation is not known. It is commonly accepted that SILC and intrinsic breakdown are caused by the same types of defects, which are randomly distributed in the oxide [25]. For intrinsic breakdown, one may speculate that foreign elements are not needed in the structure before defect generation.

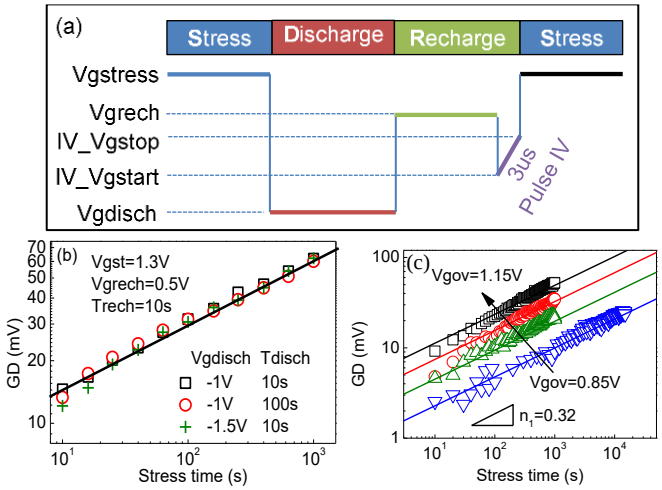

Fig. 4. (a) The Stress-Discharging-Recharging (SDR) test procedure for GD extraction. **(b)** The PBTI-induced GD extracted by SDR under different Vgdisch and Tdisch. **(c)** GD kinetics under different stress Vgov. Time exponents are ~0.32 and independent of Vgov. The symbols are from the SDR measurement and the lines are he fitted power law, i.e. Eqn (2).

B. Pre-existing defects: characterization and modelling

Pre-existing defects originate from the fabrication imperfectness. By definition, their charging and discharging kinetics will not be affected by the device's stress history. Therefore, they can be readily characterized by using heavily stressed devices. Here significant amount of GDs have already been generated, so that there is little further generation in the following pre-existing defect characterization. This suppresses the interference of trap generation on the characterization.

To understand pre-existing traps, their discharge properties are studied. For each set of symbols in **Fig.6a**, traps were first charged under a constant Vgch-Vth and the highest point represents the charged level. The trapped charges were then progressively discharged by stepping Vgdisch-Vth in the negative direction and each more negative Vgdisch-Vth step gives one lower point. After completing one discharge sequence, a higher Vgch-Vth is applied to charge the traps to a higher level, followed by a new discharge sequence to give the next set of symbols in **Fig.6a**.

When Vgch-Vth is low, the discharge profiles are independent of Vgch-Vth, i.e. they overlap well. However, when Vgch-Vth increases further, they deviate from each other and are higher for higher Vgch-Vth. This is because there are two different types of electron traps, as illustrated in **Fig. 6b&c.** One of them captures an electron without changing its energy level (**Fig. 6b**) and is named as As-grown-Traps (ATs). In contrast, after capturing one electron, the energy level of the other type shifts downwards from their ground/neutral state (**Fig. 6c).** This is named as Energy-Alternating-Traps (EADs).

Under low Vgch-Vth, charging is dominated by ATs. Since their energy level does not change after charging, their discharge profiles overlap. Under high Vgch-Vth, however, both ATs and EADs were charged. As the charged EADs have lowered its energy level, they do not discharge immediately when Vgdisch-Vth starts reducing from the Vgch-Vth. This results in the higher discharge profiles for higher Vgch-Vth in **Fig.6a**. EADs can only be neutralized when their lowered charge states are reached under more negative Vgdisch-Vth. In contrast, the additional ATs charged under a higher Vgch-Vth will be discharged as soon as Vgdisch-Vth is lowered.

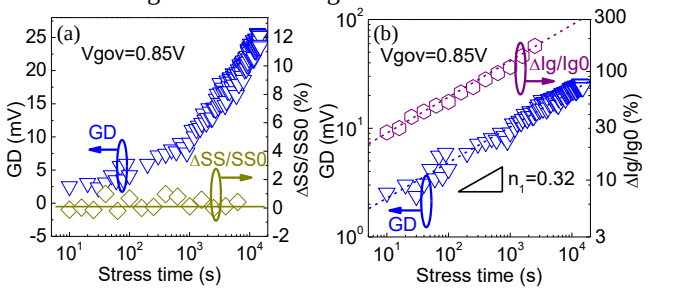

Fig. 5. (a) A ccomparison of GD and SS against stress time. Negligible ΔSS/SS0 indicates little interface states generation in PBTI. **(b)** A comparison of kinetics for GD and SILC. The SILC current is taken at Vgov of 0.85V.

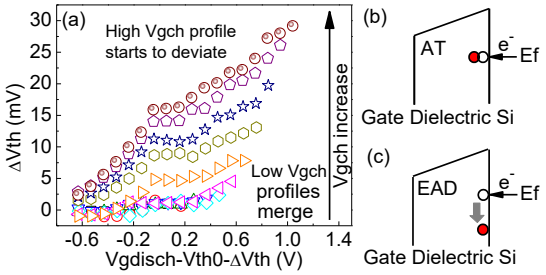

Fig. 6 (a). The discharge profiles of pre-existing traps using the method in ref 26. The traps were first charged under Vgch=Vg-Vth=0.3 V and the subsequent discharging was recorded to give the lowest set of symbols. Vgch was then raised to charge the traps again, following by discharge for the next set of symbols. This charge-discharge sequence was repeated until Vgch reached 1.1V, which corresponds to the highest set of symbols. Charging of AT **(b)** and EAD **(c):** The energy level after charging does not change for AT, but lowers for EAD.

Based on the above, AT can be extracted by adding the additional discharge for two consecutive Vgch-Vth levels to the overlapping discharge profile, as illustrated in Fig. **7a**: starting with the discharge profile at the lowest Vgch-Vth in which only AT traps are involved, the additional discharging trace under the next charging level is shifted down to align these two curves at the last point of the lower curve. By following this procedure up to the highest Vgch-Vth, the distribution of AT is extracted for the whole voltage range. Once AT is known, EAD can then be extracted by subtracting AT, as shown in **Fig. 7b**. AT dominates initially, while EAD follows a power law. Further details can be found from our early works [26, 27].

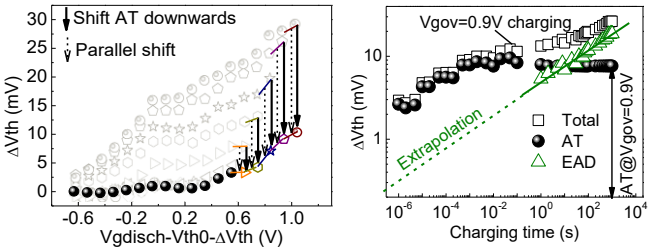

Fig. 7. (a) The extraction of ATs. For each higher set of symbols, they cover an additional voltage range, as represented by the short solid lines. Using the lowest set of symbols as the base, these short lines were shifted downward until they all joined together to give a single profile over the whole voltage range, which are the ATs. The details are given in refs. 26&27. **(b)** An example of separating EADs from ATs. After ATs were extracted, EADs were obtained by subtracting ATs.

The kinetics for EAD and AT under different overdrive voltages are extracted and shown in **Figs.8a&b,** respectively. ATs clearly saturates, confirming their 'As-grown' nature. Empirically, the saturation level, AT_{sat}, can be well modelled with Eqn (3) and its charging kinetics with Eqn (4) [28],

$$AT_{sat} = p_1 \cdot \exp(p_2 \cdot V_{gov}), \quad (3)$$

$$AT = AT_{sat} \cdot \left[1 - \exp\left(-\frac{tch}{\tau}\right)^{\gamma}\right], \quad (4)$$

where p1, p2, τ and γ are constants and extracted from the test data. EADs follow a power law with Eqn (5).

$$EAD = g_2 \cdot V_{gov}^{m_2} \cdot t^{n_2}, \quad (5)$$

where g_2, m_2, and n_2 are fitting parameters. What is worth of noting is that, although both EAD and GD follow power law, their time and voltage exponents are quite different (see Table I) and they must be modeled separately, therefore.

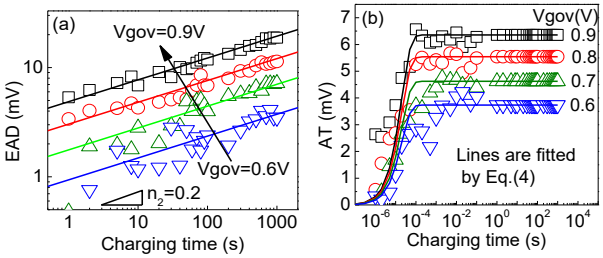

Fig. 8. (a) EAD and **(b)** AT charging kinetics under different Vgov.

As most circuits operate under AC condition, pre-existing traps charge-discharge dynamically. The discharging is directly measured and shown in **Fig. 9**. It can be described by the universal recovery curve in Eqn. (6) [29],

$$\Delta Vth_{tdisch} = \Delta Vth_{tdisch=0} \cdot \left(1 + B \cdot T_{disch}^{\beta}\right)^{-1}, \quad (6)$$

where B and β are fitting parameters.

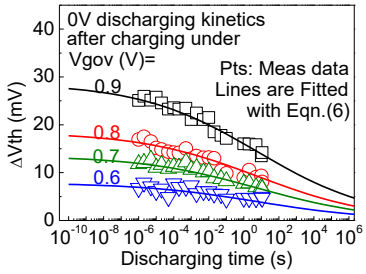

Fig. 9. The measured discharging kinetics of the pre-existing traps (Symbols) and the fitted lines with Eqn (6).

We further explored the apparent activation energy, Ea', of AT and EAD, as shown in **Fig.10**. When compared with AT, EAD has a much larger Ea', suggesting its thermally activated process. One may speculate that the structure of EAD relaxes following trapping: capturing one electron could lead to re-arrangement of microscopic structure in terms of local bond length and angle, which in turn lowered the energy level [29, 30]. In contrast, little change in energy levels of AT after trapping indicates little structure relaxation. This, together with the different trapping kinetics in **Fig.8** and the different temperature dependence in **Fig. 10**, support that ATs and EADs are different types of defects.

AT and EADs are also clearly different from GD: (i) There is no GD in fresh devices; (ii) Majority of GD will not discharge when AT and EAD are neutralized (see **Fig.7a**), indicating that GD has deeper energy levels; (iii) They have different kinetics. These differences should be taken into account for atomistic modelling in future.

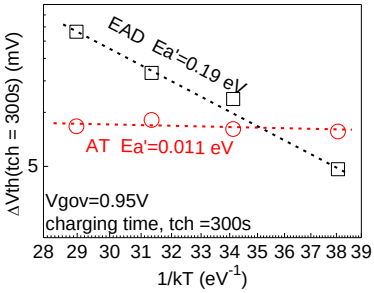

Fig. 10. The Arrhenius plot for AT and EAD. To extract the apparent activation energy, Ea', for each type of defect, both ATs and EADs are measured after charging up for 300s at different temperature.

IV. A-G MODEL AND VALIDATION

A. Model construction

Based on the above knowledge of defects, an A-G model can be built with the architecture in **Fig.11.** The model parameters for each defect are shown in Table I. They were obtained through fitting the data of short Vg-accelerated DC stress, as described in Section III. For a given set of inputs: Vg, frequency, and duty factor, the total ΔVth equals to the sum of all charged defects.

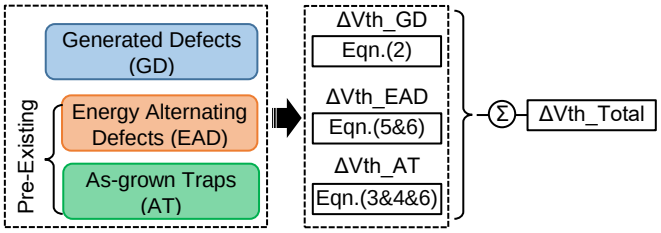

Fig. 11. The AG model framework.

TABLE I A-G model parameters extracted from short Vg-accelerated DC stress described in Section III.

	GD		EAD		AT				Discharge	
Param-eters	g_1	2.75	g_2	7.28	p1	0.29	τ	2e-4	B	0.79
	m_1	5.23	m_2	3.28	p2	3.55	γ	1	β	0.13
	n_1	0.32	n_2	0.2						

B. Model validation for predictive capability

The proposed A-G model is of value only if it can predict the PBTI degradation at the low use bias and longer time, outside the range used for fitting the model parameters. The constant-Eox paradigm is necessary for model parameter extraction, but the circuits operate under constant-Vg condition. To test the predictive capability of A-G model, PBTI degradation under several constant Vgst conditions were measured. Specifically, a relatively long test time is used for the lowest Vgst, which is limited by the minimum-measurable degradation. ΔVth under constant Vg is predicted by the model framework in **Fig.11** with Eqns (2-6). The excellent agreement between measurement and prediction for both DC and AC PBTI validates the predictive capability of the A-G model, as shown in **Fig.12a&b.** The frequency and duty factor dependences can also be predicted well in **Fig.13a&b**.

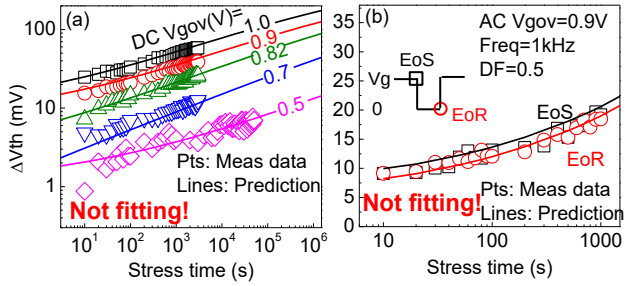

Fig. 12. A comparison of measurement and prediction with the A-G model for: **(a)** DC constant voltage stress, and **(b)** AC stress under Vgov =0.9V, 1kHz DF=0.5. For both DC and AC stresses, Vgov=Vgst-Vth(time=0) and Vgst was a constant for each set of symbols, i.e. Vgst was not adjusted for ΔVth. These test data were not used for fitting the model parameters.

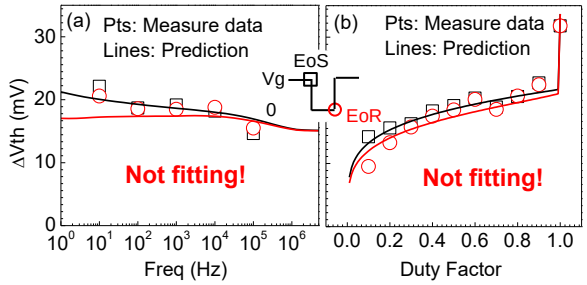

Fig. 13. Validation of prediction capability of AG model under different frequency **(a)** and Duty Factor **(b)**. Vgov of 0.9V is used.

It is worth of pointing out that this good agreement is not from the fitting. This is because the model parameter extraction is based on the data from short-term DC constant-Eox tests, while the test data under constant-Vgst in **Figs.12&13** were not used for the fitting. Indeed, the lowest Vgov=0.5 V in **Fig.12a** is well outside the range of stress biases used to extract the model parameter in **Fig.4c**. Therefore, PBTI cannot be modelled reliably by simply fitting test data with a power law and a defect based A-G model should be used.

V. Implication to Practical Device Operation

Based on the established A-G model, PBTI can be predicted under operation condition (solid lines in **Fig. 1c**). If the prediction is made from the classical power law fitted with the total ΔVth (the filled symbols in **Fig.1a**), there is a clear gap between the measured data and the prediction (the lower line in **Fig.1c**). In the short term, this gap may appear insignificant (~2mV), but it leads to an overestimation of lifetime by over 4 orders of magnitude.

The contribution from each type of defect under DC and AC real use conditions is assessed in **Fig. 14a-d**. **Fig. 14a** shows PBTI kinetics under DC condition. ATs reduce slightly for longer time, because the surface potential varies when GD and EAD increases under a constant Vg. Although AT becomes insignificant by the end of device lifetime, they must be taken into account during the PBTI test, so that an accurate time exponent can be extracted for GDs and EADs. EADs are one major component at both short and long time for DC PBTI.

Due to their larger time exponent, GDs increase faster than EADs and overtake EADs when approaching 10 years. Quantitatively, **Fig. 14c** shows the relative contributions of each defect at 1 day, 2 months and 10 years. By the end of 10 years, the contribution from GD increases to ~60%.

The degradation kinetics under AC PBTI condition is shown in **Fig. 14b**. Compared with DC, PBTI under AC is smaller. This is mainly due to the reduction of EAD, which discharges effectively during Vg=0 phase. On the other hand, GDs are similar for both DC and AC. At 10 years, GDs contribute to over 80% of the total degradation, as shown in **Fig. 14d**.

In recent years, most of test data report that PBTI is smaller than NBTI under the same electric field [31, 32]. The test time, however, is limited typically to less than 10^4 sec. In order to compare the long term NBTI and PBTI, we extracted and validated the A-G model for both of them from the same wafer. The predicted degradations under real-use condition are compared in **Fig. 15.** It is clear that when test time is short (e.g. <10k), NBTI is indeed larger. At 10 years, however, PBTI overtakes NBTI by a factor of 1.5, because of the time exponent of GD is ~0.32 for PBTI and ~0.2 for NBTI.

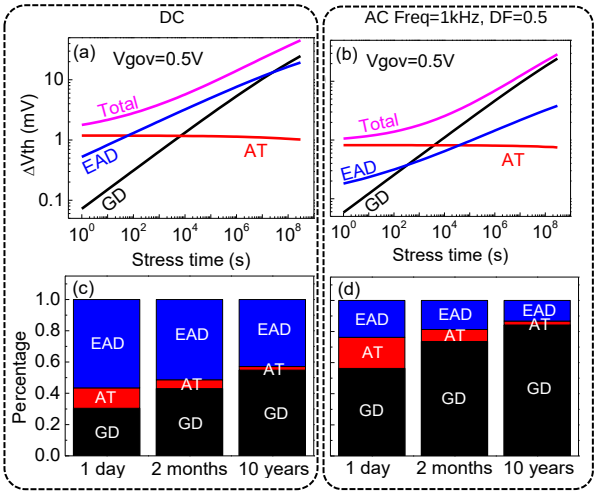

Fig. 14. Kinetics of different components against stress time under DC **(a)** and 1kHz **(b)** PBTI stress. The normalized contribution of different components under different stress time is given in **(c)** DC & **(d)** AC stress.

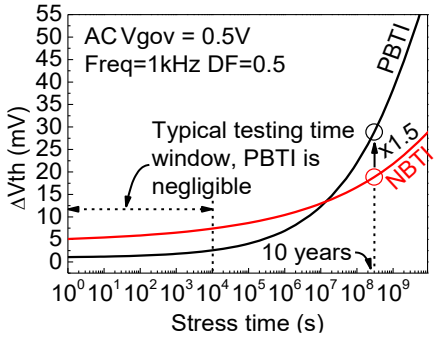

Fig. 15. A comparison of NBTI and PBTI under typical use bias of Vgov=0.5 V. Both are calculated from A-G model with parameters extracted from p- and n- FETs on the same wafer.

VI. Conclusions

In this work, for the first time, we demonstrate that the common power law model extracted from ΔVth do not warrant predicting PBTI outside the test conditions used for fitting model parameters. An A-G model is proposed, which can predict PBTI not only under DC but also under AC conditions with different frequency and duty factor. This excellent predictive capability is validated through comparison between measured data and the prediction from the model. Further

analysis based on the established model reveals that although PBTI can be smaller than NBTI within typical test time window, it becomes larger towards the end of device lifetime due to its larger time exponent. The simplicity of the model and its parameter extraction makes the proposed methodology favorable for future process qualification and circuit level reliability evaluation.

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