A 40-Gb/s Quarter-Rate SerDes Transmitter and Receiver Chipset in 65-nm CMOS

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Abstract— This paper presents a 40-Gb/s transmitter (TX) and receiver (RX) chipset for chip-to-chip communications in a 65-nm CMOS process. The TX implements a quarter-rate multi-multiplexer (MUX)-based four-tap feed-forward equalizer (FFE), where a charge-sharing-effect elimination technique is introduced into the 4:1 MUX to optimize its jitter performance and power efficiency. The RX employs a two-stage continuous-time linear equalizer as the analog front end and integrates a low-cost sign-based zero-forcing engine relying on edge-data correlation to automatically adjust the tap weights of the TX-FFE. By embedding low-pass filters with an adaptively adjusting bandwidth into the data-sampling path and adopting high-linearity compensating phase interpolators, the clock data recovery achieves both high jitter tolerance and low jitter generation. The fabricated TX and RX chipset delivers 40-Gb/s PRBS data at BER $< 10^{-12}$ over a channel with >16-dB loss at half-baud frequency, while consuming a total power of 370 mW.

Index Terms— 4:1 multiplexer (MUX), 40 Gb/s, charge-sharing effect, clock data recovery (CDR), continuous-time linear equalizer (CTLE), edge-data correlation, feed-forward equalizer (FFE), jitter suppression, jitter tolerance (JTOL), low-pass filters (LPFs), sign-based zero-forcing (S-ZF), transmitter (TX) and receiver (RX) chipset.

I. Introduction

THE exponential growth of cloud computing, social networking, and multimedia sharing has led to an explosive bandwidth demand on data communication in both telecommunication equipment and inter/intra data center [1], [2]. To accommodate to this requirement, the data rate of the wireline serializer/deserializer (SerDes) transceiver has been continuously increased [3]–[5]. Currently, 25–28 Gb/s serial links approved by InfiniBand EDR, 32GFC, and CEI-28G have stepped into the period of industrial deployment [1], [3], [6]. The 38–64 Gb/s transceivers, which

will play a key role in the next-generation data rate supported by Ethernet 400GbE, InfiniBand HDR, and CEI-56G, have attracted increasing attentions in the industry and the academia [2], [4], [5], [7]–[11]. The main challenges in designing such high-speed transceivers originate from the ever decreased unit interval (UI) period, which not only poses high bandwidth requests on the blocks located at the critical path, but also makes the link timing budget extremely tight. Moreover, advanced processes cannot completely solve these problems, since the parasitic capacitances/resistances at the high-speed outputs usually do not scale well with the technology due to the bonding and/or electro-static discharge (ESD) protection requirements.

The major difficulty in the transmitter (TX) design is insufficient timing margin for the final-stage serialization. To address this issue, traditional half-rate TXs often apply extra delay matching buffers [10], [12] or phase calibration loops [9], [13], [14] to guarantee an appropriate data selection window. These techniques result in substantial power and area overhead. An alternative solution is to replace the last three 2:1 multiplexers (MUXs) with a single 4:1 MUX [4], [11], [15], [16]. The resulting quarter-rate serialization relaxes the critical path timing margin to 3 UI, halves the maximum clock speed, and saves considerable power. These benefits come with the penalty of a doubled self-loading drain capacitance, which dramatically degrades the bandwidth of the 4:1 MUX, hence limiting its maximum operation speed.

The main challenge in designing high-speed clock data recovery (CDR) is how to satisfy the bandwidth requirement while maintaining excellent jitter performance. In many SerDes protocols, the CDR bandwidth grows linearly with the data rate [2]. In a phase interpolator (PI)-based digital CDR (preferred choice because of its robustness, portability, and compactness), this requirement can be achieved by either raising the update rate of the CDR logic or increasing the data width of the CDR logic. The update rate is constrained by the synthesized logic speed while the increased data width directly increases the update step size and extends the loop latency that are both prone to enlarge the dithering jitter [2]. The CDR performance is also limited by the PI nonlinearity, which not only deteriorates the uniformity of the phase steps but also causes phase-spacing errors among the multi-phase sampling clocks. The short UI makes the CDR design even more challenging, since there is smaller margin left for the sampling deviation, clock dithering, duty cycle distortion, and quadrature phase errors [2], [5], [17].
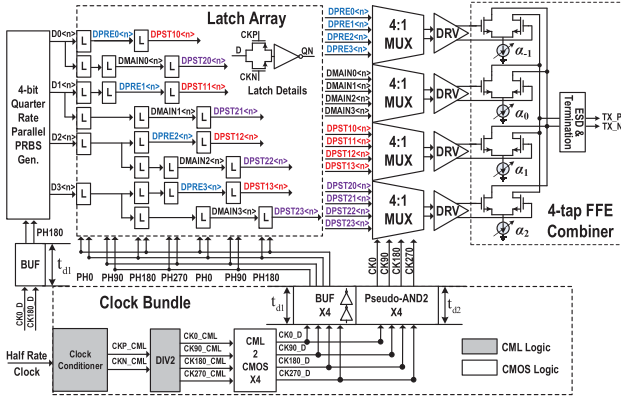
Fig. 1.   Block diagram of the TX chip.

For serial links operating around tens of Gb/s, adaptive equalization has become a dominant option [18]–[20]. One common reason applicable to all data rates is that the practical channel diversity and uncertainty make it difficult and unreliable to manually calibrate the equalization parameters. Another reason is that the channel loss variation becomes particularly severe for data rates beyond 10 Gb/s. This is because the fast rolling-down channel profile makes the channel loss sensitive to manufacturing errors and ambient environment changes. For example, the insertion loss variation of a CAUI-4 compliant channel has been measured to exceed 1.9 dB over a temperature range from -5 to 75 °C at 14 GHz [21].

To alleviate these difficulties and provide potential solutions for ultra-high-speed transceiver design, this paper presents a 40-Gb/s quarter-rate SerDes TX and receiver (RX) chipset. The remainder of this paper is organized as follows. Section II describes the TX chip, mainly focusing on the improved 4:1 MUX. Section III illustrates the RX chip, where the CDR performance is enhanced by introducing jitter-suppression filters and adopting high-linearity compensating PIs. In Section IV, a low-cost sign-based zero-forcing (S-ZF) adaptation algorithm relying on edge-data cross correlation is designed to achieve adaptive tap-weight adjustment for the TX-feedforward equalizer (FFE). Section V gives the experimental results and performance comparison, and Section VI concludes this paper.

II. Transmitter Chip

A. Overall Architecture

Fig. 1 shows the block diagram of the TX chip. It contains a multi-MUX-based four-tap FFE combiner, a latch array, an on-chip PRBS generator, and a clock bundle. The parallel quarter-rate data $D0\langle n\rangle$, $D1\langle n\rangle$, $D2\langle n\rangle$, and $D3\langle n\rangle$ are generated by the on-chip PRBS generator, which are then interleavedly latched by the compact latch array to produce the 16-path quarter-rate data for the following four 4:1 MUXs. The desired timing relationship (see the signal positions in the latch array), which enables each MUX to share the same timing margin, is satisfied by 90°-spaced quarter-rate clock relatching. The full-rate UI-spaced outputs of the 4:1 MUXs are first buffered by the pre-drivers and then sent to the four-tap FFE combiner. In the clock bundle, a clock conditioner is employed
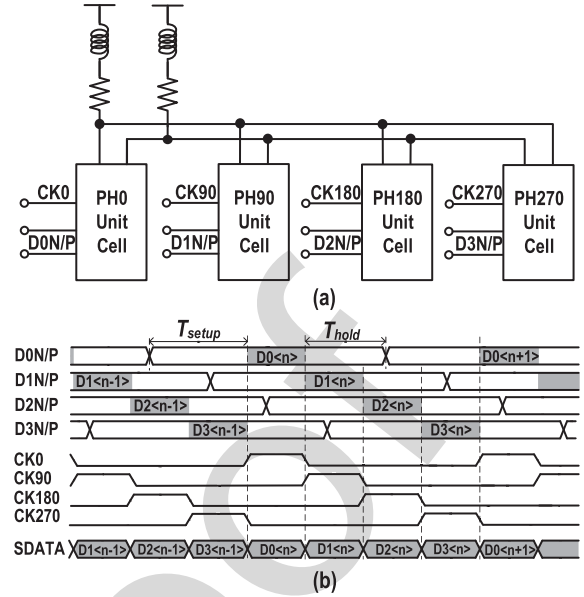

Fig. 2.   Topology of the 4:1 MUX. (a) Conceptual schematic. (b) Timing diagram.

to convert the incoming single-end half-rate clock into differential outputs, which are then fed into a divider (DIV2) to generate the quart-rate I, Q clocks. After being transformed into full swing by the CML2CMOS converters, these clocks are further applied to four driving buffers and four pseudo-AND2s to produce 50% and 25% duty cycle clocks for the latch array and the 4:1 MUXs, respectively.

The main feature of the TX chip is the compact implementation of the multiple 4:1 MUX-based four-tap FFE, which not only relaxes the stringent timing requirement of the final serialization stage, but also provides a robust approach to support a wide operation range. On the other hand, the doubled self-drain capacitance in the 4:1 MUX significantly reduces the bandwidth of the MUX, which is the key factor that constrains the maximum operation speed. Additionally, the output performance highly relies on the quality of the multi-phase gating clocks. The remainder of this section will focus on the enhancement of the 4:1 MUX, including topology consideration, unit cell improvement, and clocking techniques.

B. Topology of the 4:1 MUX

Fig. 2(a) describes the conceptual schematic of the 4:1 MUX, which is composed of a pair of shunt-peaked loads and four identical pull-down unit cells. These unit cells are activated sequentially by the UI-spaced clocks (CK0-90-180-270) to combine the four quarter-rate data streams (D0-1-2-3) into one serial sequence (SDATA) [see Fig. 2(b)]. Unlike the 4:1 MUXs presented in [4] and [11] that combine both the ANDing operation and sampling operation into the pulling-down unit cell, the unit cell in this design only performs the sampling operation while the ANDing operation is carried out by the pseudo-AND2s in the clock bundle (see Fig. 1). This splitting arrangement allows the four 4:1 MUXs in Fig. 1 to share one common ANDing stage, thus exhibiting more potentials on power efficiency.
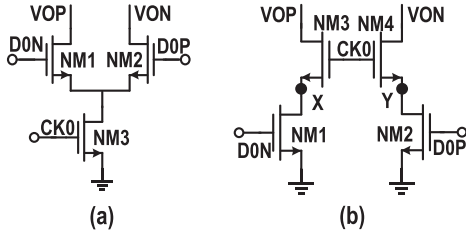
Fig. 3. Traditional unit cell implementations for high-speed 4:1 MUX. (a) Data-up structure. (b) Clock-up structure.
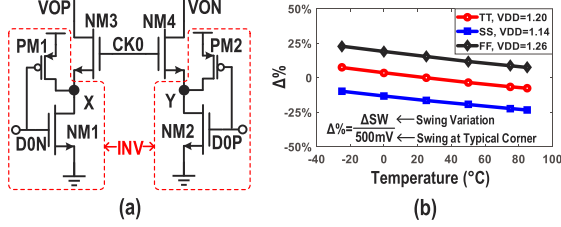

Fig. 4. Improved unit cell implementation. (a) Schematic details. (b) Swing variations for different PVT corners.
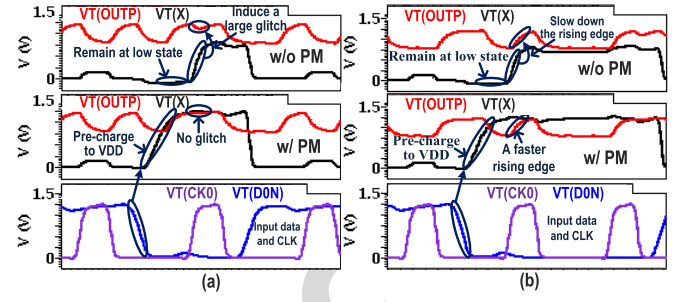

Fig. 5. Effect of the introduced PM on (a) high-level glitches and (b) edge transitions.

Fig. 6. Simulated eye-diagrams of the 4:1 MUX. (a) Without PM. (b) With PM.

C. Enhancement on the Unit Cell of the 4:1 MUX

Fig. 3 shows the two widely used traditional unit cells for high-speed 4:1 MUX, where the current source transistors are eliminated to avoid stacked devices. In the data-up structure [11], [22] [see Fig. 3(a)], the output can be corrupted by the data transitions on other branches through the forward-coupling path from the data input to the output when the MUX is performing data selection on one branch [23]. Fig. 3(b) shows the clock-up structure [1], [12], where the forward-coupling path is eliminated by moving the clocking pairs to the top. However, it suffers from severe charge-sharing effect between the outputs VOP/VON and junction nodes X/Y. Inspired by the voltage mode source-series terminated (SST) driver discussed in [24], we introduce a pair of pre-charging transistors PM1/PM2 into the pulling-down unit cell [see Fig. 4(a)]. The pre-charging PM1/PM2 and the data-gating NM1/NM2 actually constitute two inverters, which make nodes X/Y be always pre-driven to desired states, thus eliminating the charge-sharing effect. Compared to the SST implementation in [24], the improved 4:1 MUX exhibits more potentials on high-speed applications. This is because it can fully exploit the process potentials as its compact NMOS driving topology naturally features fast current switching speed and small parasitic capacitance. Additionally, the speed-constraining output capacitances, including self-drain load, routing wire, and far-end driving load, can be neutralized by adopting on-chip peaking inductors. In the rest of this part, we will discuss the adverse effect of the charge sharing in conventional clock-up structure and the favorable effect of the introduced pre-charging transistors.

1) Charge-Sharing Effect in Conventional Clock-Up Structure: The top row of the simulated waveforms in Fig. 5(a) and (b) demonstrates the two adverse effects of the charge sharing in the conventional clock-up structure [see Fig. 3(b)].
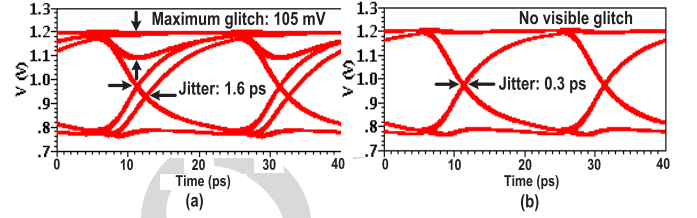
Assuming that the upcoming data D0P/D0N are logic high/low, node Y is pre-discharged to the ground through NM2, which helps to speed up the falling edge. The voltage of node X depends on previous transmitted data. In case that the previous D0N is logic low, node X should have been charged to an allowed maximum value (VDD − V_{THN}) during the selection-enabled period (high pulse duration of CK0), which should maintain to the present instant since NM1 has always been in cutoff state. Therefore, this will not cause prominent charge-extraction effect, as node X has already been charged to the allowed maximum value by the previous transmitted bit. If the previous D0N is logic high, node X should keep the ground voltage that is pulled down during the hold time in previous bit period [i.e., T_{hold} in Fig. 2(b)]. When the high pulse of CK0 arrives, the capacitance at node X will extract charge from the output, thus causing a remarkable glitch for two consecutive output bits at high level or slowing down the rising edge for a low-to-high transition, as shown in the top row of Fig. 5(a) and (b), respectively.

2) Effect of the Introduced Pre-Charging Transistors: To demonstrate the effect of the introduced pre-charging transistors PM1/PM2 shown in Fig. 4(a), we take PH0 branch as an example to illustrate the operation process of the proposed pull-down unit cell. When input data arrive, depending on D0N/D0P, nodes X/Y are either pre-charged to VDD or pre-discharged to VSS by the two inverters consisting of PM1/PM2 and NM1/NM2. This makes nodes X/Y always in desired states, which are coincident with the output signal levels. Then, NM3/NM4 are turned on to send D0N/D0P to the MUX's outputs as the high level of CK0 comes. After a period of 1 UI, the pull-down path is switched off by the falling edge of CK0 and the voltage level of nodes X/Y stays unchanged until the next input data come. The main feature
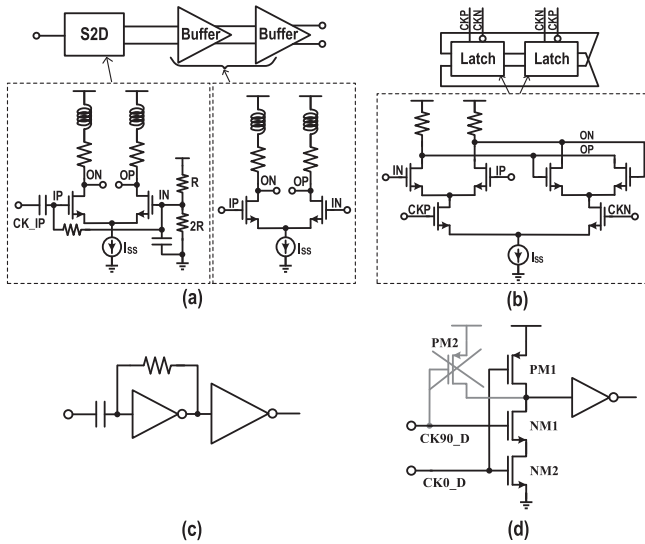
Fig. 7. Circuit details of the clocking blocks. (a) Clock conditioner. (b) DIV2. (c) CML2CMOS. (d) Pseudo-AND2.

Fig. 8. Block diagram of the RX chip.

of this 4:1 MUX is its ability of eliminating the charge-sharing effect caused by parasitic capacitances at nodes X/Y, which brings in several benefits. First, the deterministic jitter and glitches caused by charge extraction can be remarkably mitigated [see the middle row in Fig. 5(a) and (b)]. The simulated eye-diagrams in Fig. 6 indicate that the inter-symbol interference (ISI) induced by charge sharing is reduced from 1.6 to 0.3 ps and the voltage glitches are mostly removed. Moreover, the glitch elimination effectively improves the noise margin that allows a lower output swing to save power. Second, the elimination of the charge-sharing effect makes the capacitances at nodes X/Y less significant. Thus, large-size NM1/NM2 can be used to enhance the discharging capabilities. Note that the output swing is determined by the proportion of resistive load and equivalent resistance of stacked NM1/NM3 (NM2/NM4). For a fixed output swing, the big size of NM1/NM2 implies that NM3/NM4's size can be reduced. The smaller size of NM3/NM4 helps to decrease the self-loading drain capacitances of the unit cells. Consequently, the bandwidth of the overall 4:1 MUX can be expanded. Fig. 4(b) gives the swing variation for different process, voltage, and temperature (PVT) corners, which can be controlled under 25%. By adopting a tunable resistor, it can be further reduced [4]. Third, the added transistors PM1/PM2 provide another path through NM3/NM4 to help to pull up the output, which can accelerate the rising transitions.

D. Clocking Blocks for the 4:1 MUX

As shown in Fig. 1 (bottom), the desired full swing clocks for the latch array and the 4:1 MUXs are produced by a clock bundle, where current mode logic (CML)-style circuits are employed in the clock conditioner and DIV2 to support the most high-speed operation (half-rate) while the CML2CMOS and pseudo-AND2 are implemented in a more power efficient CMOS style. Fig. 7 shows the implementation details of these building 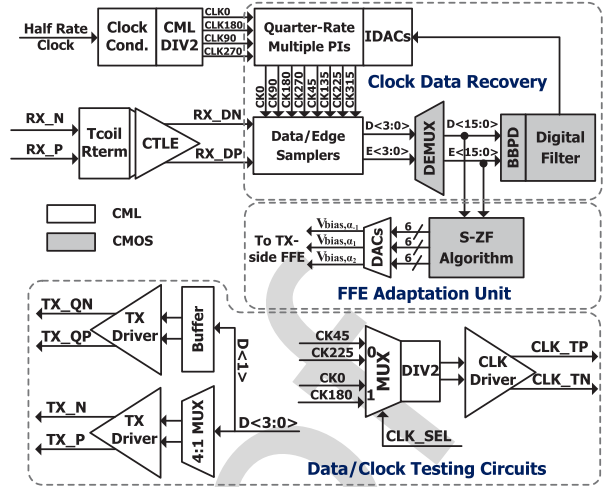blocks. As shown in Fig. 7(a), the clock conditioner is composed of an ac-coupled S2D and two cascaded CML buffers, where the former is used to convert the single-end clock input into differential outputs and the latter is utilized to further rectify the clock waveforms. For the DIV2, a traditional inductorless CML latch shown in Fig. 7(b) is used to balance the operation speed and layout compactness. Fig. 7(c) gives the schematic details of the CML2CMOS, where an ac-coupled inverter with a feedback resistor is utilized to convert the CML voltage level to full swing CMOS logic. For the pseudo-AND2, its function is to AND the two 50% duty cycle half-rate clocks with 90° phase shift to generate the 25% duty cycle clocks for the 4:1 MUXs. In this design, a pseudo-NAND2 associated with a driving inverter [see Fig. 7(d)] is employed to perform the ANDing operation [25]. In contrast to conventional NAND2, this pseudo-NAND2 eliminates the pulling-up transistor PM1, thus reducing the output capacitance. The similar circuit realizations of the pseudo-AND2 and the BUF (consisting of two cascaded inverters) also mitigate the delay mismatch between t_{d1} and t_{d2} (see Fig. 1), which helps to meet the stringent timing constraints against PVT variations.

III. RECEIVER CHIP

A. Overall Architecture

The main task of the RX is to extract the transmitted data from the received signal using appropriate equalization and CDR techniques [26]–[29]. Fig. 8 shows the block diagram of the RX chip. It consists of a two-stage continuous-time linear equalizer (CTLE), a quarter-rate CDR, an FFE adaptation unit, and some testing circuits for the recovered data and clock measurements. The received signal is first equalized by the CTLE and then sliced by eight data/edge samplers, where the sampling clocks are generated by two quarter-rate compensating PIs and the sampling positions are adjusted by a CDR logic using bang–bang phase detectors (BBPDs). In addition, a newly developed S-ZF algorithm along with three 6-bit DACs is adopted to produce the bias voltages for the TX-FFE. The rest of this section focuses on the optimization techniques for the CDR, and the S-ZF algorithm will be elaborated in Section IV.
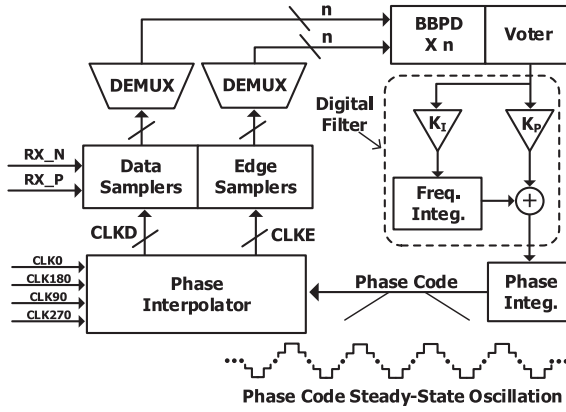
Fig. 9.   Conventional BBPD-based CDR.

B. Challenges in Conventional BBPD-Based CDR

Fig. 9 shows the conventional architecture of the BBPD-based CDR. Due to the nonlinear behavior and inevitable loop delay, the phase code applied to the PI usually exhibits steady-state oscillation, which brings in substantial deterministic jitter through rotating the PI. This effect can become more severe as the data rate increases, because the increased loop gain and the not-well-scaled loop latency are prone to cause a larger limit-cycle oscillation amplitude. To attenuate this amplitude, a split-path CDR/DFE architecture was proposed in [30], which employs a digital averaging technique to filter the phase code for the separate data-sampling clocks. This approach can effectively improve the jitter tolerance (JTOL) amplitude at high frequencies, but the inevitable delay added by the digital averaging block may make the sampling clocks drift away from the optimal positions, thus degrading the maximum tolerable amplitude at low frequencies.

Another factor that limits the performance of the BBPD-based CDR is the nonlinearity of the phase-rotating PI, where both the differential nonlinearity (DNL) and integral nonlinearity (INL) can result in serious adverse effects on the overall CDR performance. Specifically, the DNL introduces a much larger phase jump than the ideal one, which can be directly converted into recovered clock jitter. The INL can make the data-sampling clocks drift away from their optimal decision points in quarter-rate architectures using multiple PIs [2].

C. Improvement on CDR Architecture

Fig. 10 shows the block diagram of the improved CDR. It employs separate PI1 and PI2 to produce the two sets of 45°-spaced clocks for the data sampling and edge sampling, where passive low-pass filters (LPFs) are introduced into the clock branch for the data sampling to provide extra jitter suppression on the data-sampling clocks. The bandwidth of these introduced LPFs is adaptively adjusted by the same DF⟨2:0⟩, which is the absolute value of the truncated frequency code generated by the frequency integrator in the digital loop filter. Particularly, the minimum bandwidth of the LPFs is about 4 MHz while the maximum one is around 50 MHz. In addition, a limiter is utilized to set the DF⟨2:0⟩ to its
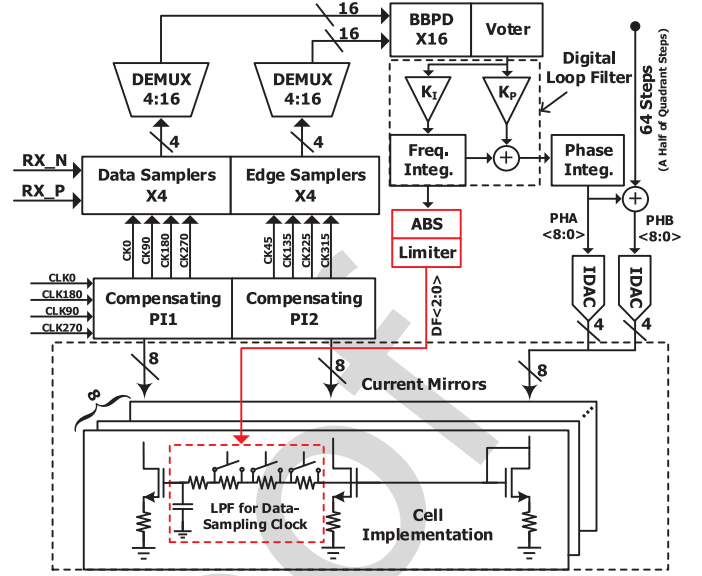

Fig. 10.   Block diagram of the modified CDR architecture.
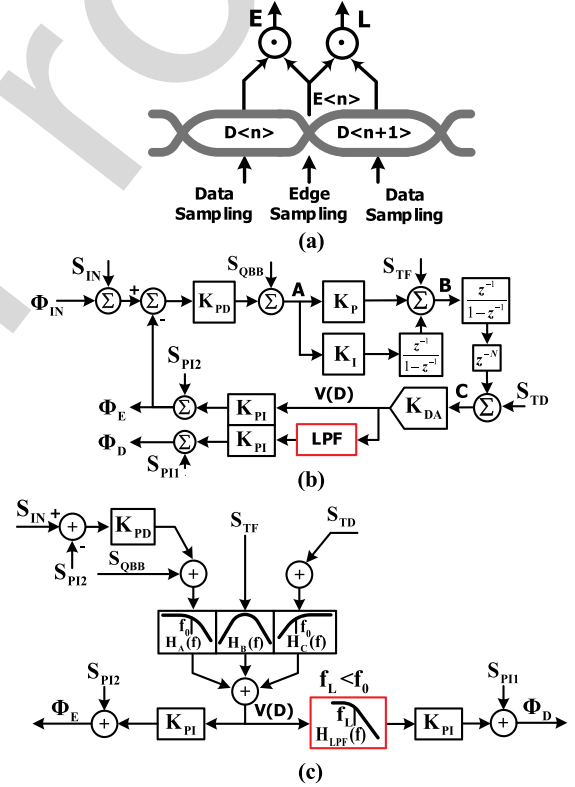
Fig. 11.   Functional view of the introduced LPFs. (a) Principle of the BBPD. (b) Linearized CDR model. (c) Jitter transfer functions.

maximum value when the frequency code goes too large. In principle, a large frequency code indicates a continuous phase slewing to accommodate to the accumulative jitter tracking. Thus, a wide bandwidth is chosen to improve the jitter tracking ability. On the contrary, a small frequency code implies that there is little trackable jitter. Accordingly, a narrow bandwidth is selected to suppress the high-frequency jitter.

The working principle of the BBPD is shown in Fig. 11(a). Considering the fact that the data sampling occurring at the

Fig. 12. Effect of the LPFs with a bandwidth of (a) 4 MHz, (b) 20 MHz, (c) 50 MHz, and (d) adaptively adjusting.

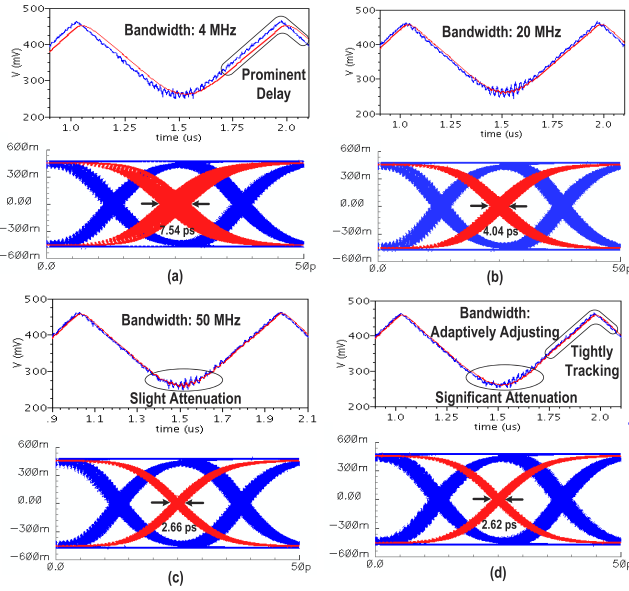Fig. 13. Properties of the adaptive-bandwidth jitter suppression.

center of the eye-diagram serves as a reference to judge whether the edge sampling is leading or lagging the input data transitions, there should be sufficient margin for the data sampling. Accordingly, the outputs of the data samplers show a fairly low sensitivity to phase errors in normal operating CDRs, which means that further jitter suppression on data-sampling clocks exhibits little effect on the loop parameters for jitter tracking. Leveraging this characteristic of the BBPD, we introduce LPFs into the data-sampling path to further filter the output jitter while keeping the loop parameters unchanged to satisfy the JTOL specification. Fig. 11(b) shows the small-signal model of the modified CDR, where the LPF located outside of the feedback loop is able to provide additional jitter suppression for the data-sampling clocks [see Fig. 11(c)]. Therefore, the dithering jitter caused by the limit-cycle oscillation can be effectively attenuated. The noise sources are also shown in Fig. 11(b), including the input noise (S_{IN}), quantization noise (S_{QBB}) of the BBPD, truncation noise I (S_{TF}) due to finite resolution of the integral path, truncation noise II (S_{TD}) due to limited resolution of the IDAC, and nonlinearity noise (S_{PI1}, S_{PI2}) of the PIs. Fig. 11(c) shows the transfer function characteristics for these noise sources. It can be seen that the introduced LPFs can dramatically attenuate the remaining band-frequency and high-frequency components from S_{TF} and S_{TD}. The low-frequency components of S_{IN}, S_{PI2}, and S_{QBB} can be further reduced by these LPFs when lower bandwidths are employed. In addition, the potential jitter peak can be suppressed to alleviate the jitter amplification problem.

Note that the phase delay caused by the LPFs should be small enough to ensure that the data-sampling clocks stay in the vicinity of the optimal sampling point. Otherwise, the high-frequency jitter suppression could be overwhelmed by the delay-caused phase shift, thus deteriorating the overall CDR performance. Fig. 12 shows the filtering effect on the current
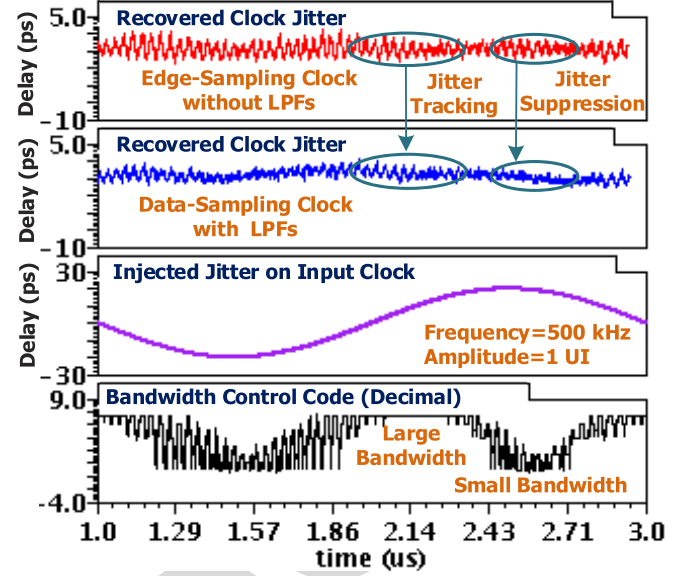
mirror bias for 0°-phase and the jitter performance of the data-sampling clock with different LPF bandwidths, where the eye-diagrams are overlapped from 0.9 to 2.1 μs. These simulations are performed under the condition that a 500-kHz sinusoidal jitter with a 1 UI amplitude and a 5-ps peak-to-peak random jitter are respectively injected into the input clock and input data using PRBS7. For the simulated diagrams with the bandwidth of 4 MHz in Fig. 12(a), the high-frequency ripples on the bias can be significantly suppressed by the LPF. However, the dithering jitter of the data-sampling clock reaches 7.54 ps, which is much larger than that of the edge-sampling clock without the LPF (3.04 ps). It means that the CDR performance is actually deteriorated. This is mainly because of the prominent phase shift caused by the LPF delay. As the bandwidth increases, the delay-caused phase shift becomes smaller, thus indicating a descending trend in dithering jitter of the sampling clock [see Fig. 12(b) and (c)]. For the bandwidth fixed at 50 MHz, the dithering jitter of the data-sampling clock (2.66 ps) becomes smaller than that of the edge-sampling clock (3.04 ps). This implies that the jitter optimization contributed by the bias-ripple suppression overwhelms the delay-caused phase shift. Based on the above-mentioned discussion, it can be found that adopting a fixed bandwidth is inadvisable, since the low bandwidth suffers from delay-caused phase shift while the high bandwidth exhibits limited jitter suppression. Fig. 12(d) shows the simulation results when utilizing the proposed bandwidth-adaptively adjusting technique, where the low dithering jitter is achieved by balancing the bias tracking and ripple suppression. When the input pattern ranges from PRBS7 to PRBS15, PRBS23, and PRBS31, the CDR exhibits a similar balance between high-frequency ripple suppression and low-frequency bias tracking but with a slightly increased jitter due to the increased run length of "1s" or "0s".

To further explore the bandwidth-adaptively adjusting process, Fig. 13 gives the transient simulation waveforms
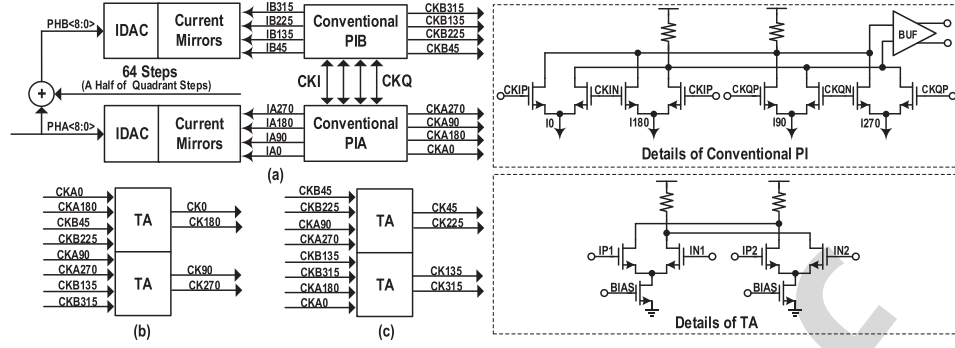
Fig. 14. Proposed compensating PI. (a) Quarter-rate 45°-spaced clock generation. (b) In-phase I, Q clock generation for the data sampling. (c) 45° phase-shifted I, Q clock generation for the edge sampling.
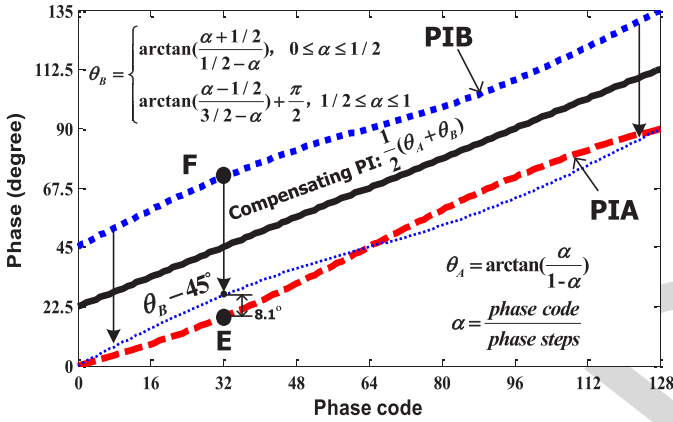

Fig. 15. Phase transfer characteristics based on trigonometric-function approximation.
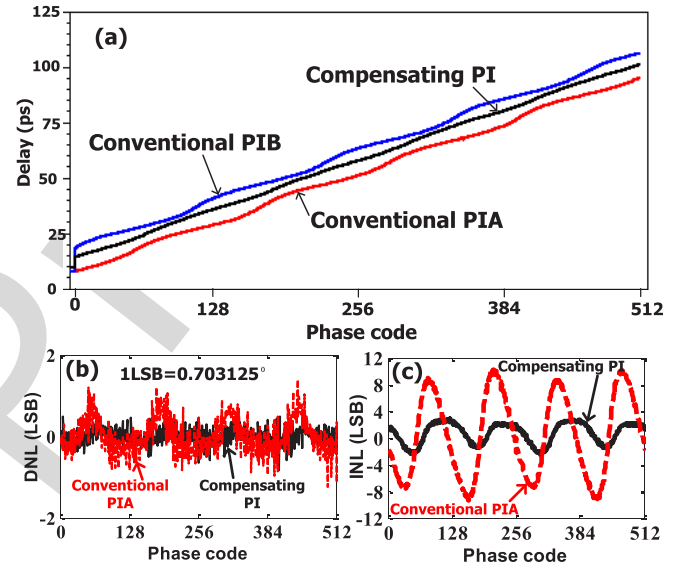

Fig. 16. Simulation results of the phase-compensating PI. (a) Simulated phase transfer characteristics. (b) DNL performance. (c) INL performance.

using PRBS7. For the fast input jitter changing region (a jitter tracking region), a large frequency code is accumulated in the frequency integrator (see Fig. 10), thus a high bandwidth control code $DF\langle 2:0 \rangle$ for the LPFs can be obtained (see the bottom waveform in Fig. 13). As a result, the data-sampling clocks can tightly track the edge-sampling clocks to avoid data-sampling lagging. For the slow input jitter changing region (a jitter suppression region), the frequency code becomes small and so does the bandwidth control code $DF\langle 2:0 \rangle$. Correspondingly, the bandwidth of the LPFs decreases, thus exhibiting prominent jitter suppression effect. Owing to the proposed adaptive bandwidth-adjusting scheme, the jitter suppression and jitter tracking can be automatically balanced in this CDR. Overall, this automatic bandwidth selection technique makes it possible to use a low bandwidth to significantly suppress the high-frequency jitter while exhibiting little effect on the low-frequency jitter tracking ability.

D. Compensating PI

Fig. 14(a) shows the widely used scheme for 45°-spaced clock generation, where two conventional PIs (PIA and PIB) with 1/2-quadrant-step spaced phase codes (PHA$\langle 8:0 \rangle$ and PHB$\langle 8:0 \rangle$) are utilized to produce the two sets of 45°-spaced clocks (CKA0-90-180-270 and CKB45-135-225-315) [2], [12]. Their phase transfer characteristics based

on trigonometric-function approximation can be described by the respective red dashed and blue dotted lines in Fig. 15. When PIA rotates to point E and PIB rotates to point F, the phase shift between them can reach a maximum of 8.1° (or 0.09 UI). Since the edge-sampling clocks tightly track the edge transitions in the received data stream, any phase-spacing variation between the edge-sampling and data-sampling clocks could make the data-sampling clocks drift away from the expected decision point. Moreover, improving the PI resolution cannot optimize this effect since fine step weights cannot change the shape of the phase transfer characteristics.

To address these issues, we develop a phase-compensating technique, which applies four time averaging (TA) [see Fig. 14(b) and (c)] to further average the two sets of 45°-spaced clocks. Specifically, the data-sampling clocks (CK0-90-180-270) are obtained by averaging CKA0-90-180-270 and CKB45-135-225-315, while the edge-sampling clocks (CK45-135-225-315) are attained by averaging CKA90-180-270-0 and CKB45-135-225-315.
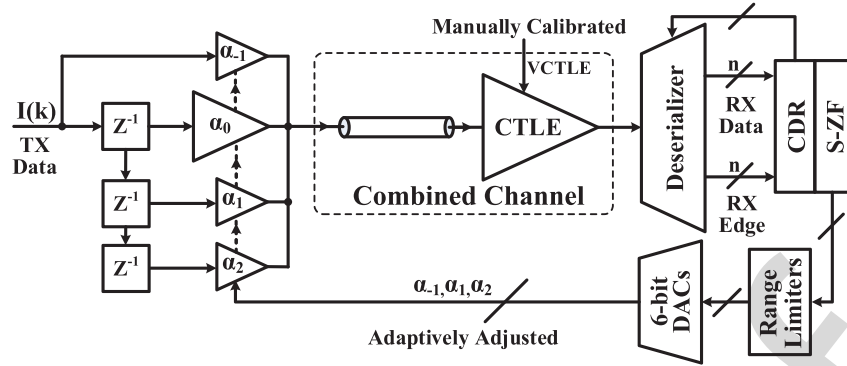
Fig. 17.   Implemented equalization scheme with the proposed S-ZF algorithm.

Mathematic analysis shows that the phase transfer function of the proposed compensating PI is a combination of two *arctan* functions given in Fig. 15, where a more linear phase transfer curve with negligible phase deviations smaller than 0.17° can be achieved. In practical implementation (see the schematic details of PI and TA in Fig. 14), the linearity optimization is degraded by the transistors' inherent nonlinearity and nonideal input clock waveform. Simulation results shown in Fig. 16 imply that the INL can be controlled below 2.5 LSB (or 1.8°), which is only a quarter of that of the conventional PI. The simulation also shows that the additional PI and TAs in each compensating PI consume around 10 mW.

IV. Channel Equalization

The equalization scheme consisting of a TX-FFE and an RX-CTLE is utilized to compensate for the channel loss. As shown in Fig. 17, the RX-CTLE is manually calibrated while the tap weights of the TX-FFE are adaptively adjusted by an edge-data correlation-based S-ZF algorithm in the RX side. The digital tap weights generated by the S-ZF engine are first constrained by three range limiters and then applied to three 6-bit DACs to produce the bias voltages for the TX-FFE taps. These bias voltages are transferred to the TX through PCB traces. The TX-FFE is performed by a CML-based four-tap FFE combiner, where the tap weights are adjusted by changing the bias voltages of the current sources (see Fig. 1). The RX-CTLE schematic details and its frequency responses are described in Fig. 18.

A. Previous Adaptation Algorithms

According to different evaluation criteria [18]–[20], [31]–[34], previous adaptation algorithms for wireline communications can be mainly categorized into sign–sign least mean square (SS-LMS) [18]–[20], [31], ZF [32], [33], and maximum eye opening (MEO) [34]. A common drawback of these methods is that they need auxiliary circuits to extract the error information. Particularly, the SS-LMS algorithm requires additional samplers to detect the signed errors between the equalized and expected eye heights [18]–[20], [31]. The traditional ZF necessitates an extra ADC to convert the equalized output voltages into digital codes [32], [33]. The MEO requests an even more complicated eye monitor, which usually

incorporates threshold-adjusting samplers, phase-adjusting PIs, micro-controller, and measurement software [34], to measure the internal eye opening. These auxiliary circuits make these methods less competitive for applications at tens of Gb/s due to the following reasons: 1) maximum bandwidth deterioration because their input capacitances are directly connected to the critical signal path; 2) substantial power consumption as the additional circuits usually operate at high speed; and 3) more complicated layout placing and routing.

B. Edge-Data Correlation-Based S-ZF Adaptation Algorithm

To preclude the auxiliary circuits in previous adaptation algorithms [18]–[20], [31]–[34], a low-cost S-ZF algorithm utilizing edge-data cross correlation is developed. The target is to force the cross correlation between the sign of the edge-sampling error and received data to zero. The iterative procedure of the TX-FFE tap weights is given by

$$\alpha_l(k+1) = \alpha_l(k) - \lambda \cdot \text{sign}[e(k)] \cdot D(k-l)$$
$$(l = -1, 0, 1, 2) \quad (1)$$

where $\alpha_l(k)$ is the instant l-tap weight, $\text{sign}[e(k)]$ represents the sign of the edge-sampling error, $D(k)$ denotes the recovered data, and λ stands for the scale factor controlling the adjustment rate and its value is usually much smaller than 1. The sign of the edge-sampling error $\text{sign}[e(k)]$ caused by the ISI is directly mapped from the quantized edge sequence $E(k)$, and it is correlated with the data bit $D(k-l)$ to produce the product $\text{sign}[e(k)] \cdot D(k-l)$. The result is then integrated to update the FFE tap weight $\alpha_l(k)$.

The main feature of this approach is that it only involves the existing quantized edge sequence $E(k)$ and recovered data sequence $D(k)$. As a result, the essential auxiliary circuits, such as samplers, ADCs, and PIs in previous adaptive equalizations [18], [19], [31]–[34], are removed, thus exhibiting more potentials on operation speed and cost effectiveness.

C. Derivation of the Edge-Data Correlation-Based S-ZF Adaptation

For a TX with l-tap UI-spaced FFE, the pre-distorted output can be represented by

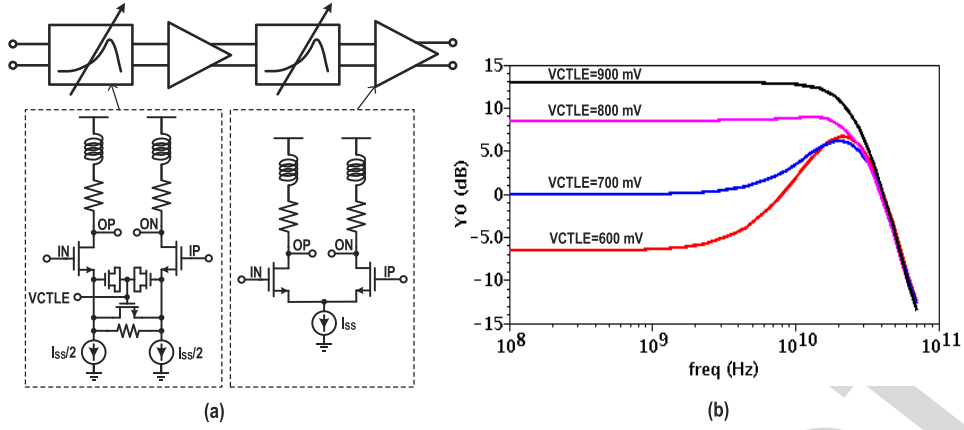$$t(k) = \sum_l \alpha_l I(k-l) \quad (2)$$

Fig. 18. RX-CTLE. (a) Schematic details. (b) Frequency responses for different control voltages.
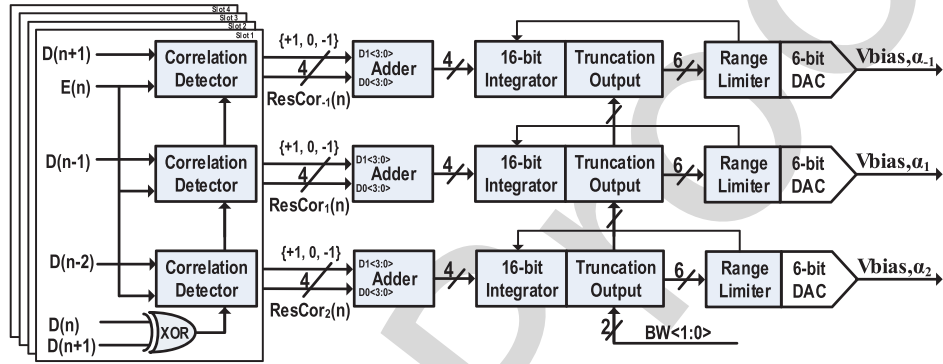

Fig. 19. Block diagram of the edge-data correlation-based S-ZF adaptation algorithm.

where $I(k)$ is the transmitting sequence, α_l denotes the tap weight, and l is the tap index [34]. To make the analysis more compact, the cascaded passive channel and RX-CTLE are treated as a combined channel with a new pulse response of c_k. By calculating the convolution of pre-distorted output $t(k)$ and the channel pulse response c_k, the received discrete-time sequence before binary quantization can be given by

$$r(k) = \sum_l \alpha_l \left(\sum_i I(i)c_{k-l-i} \right). \tag{3}$$

According to the discussion in [35], the cross-correlation coefficient $\rho_{y,x}(n)$ between the output signal $y(m)$ and the input signal $x(m)$ is exactly equal to the impulse response $h(n)$. Applying this conclusion and replacing the recovered data sequence $D(k)$ with the input sequence $I(k)$, we attain the cross-correlation coefficient between the edge-sampling error sequence $r(k+0.5)$ and the recovered data sequence $D(k)$

$$\hat{\rho}_{e,d}(n) = \sum_l \alpha_l c_{n-l+0.5}. \tag{4}$$

The reason why $I(k)$ can be considered equivalent to $D(k)$ is because the bit error rate (BER) is usually quite low ($<$1e-12) for normal operation links.

For an ideally equalized serial link, the edge-sampling error sequence is supposed to be a 0-sequence. Hence, all the cross-correlation coefficients should be zero. However, this needs infinite taps to cancel all the residual ISI. Considering the

fact that the ISI tail decreases exponentially as the time goes on, it is reasonable to assume that the ISI affects a finite number of symbols and previous research has demonstrated that equalizers with a specific number of taps can effectively compensate for legacy channels [17], [19], [31], [34], [36]. In principle, when the tap weights are adjusted close to the targeted values, the resulting cross-correlation coefficient $\hat{\rho}_{e,d}(n)$ should be forced toward zero. Taking the implemented four-tap FFE in this design as an example, for a group of proper tap weights, we have

$$\hat{\boldsymbol{\rho}}_{e,d} = \boldsymbol{C}\boldsymbol{\alpha} = \boldsymbol{0} \tag{5}$$

where

$$\hat{\boldsymbol{\rho}}_{e,d} = (\hat{\rho}_{e,d}(-1), \hat{\rho}_{e,d}(0), \hat{\rho}_{e,d}(1), \hat{\rho}_{e,d}(2))^T$$
$$\boldsymbol{\alpha} = (\alpha_{-1}, \alpha_0, \alpha_1, \alpha_2)^T$$
$$\boldsymbol{C} = \begin{pmatrix} c_{0.5} & c_{-0.5} & c_{-1.5} & c_{-2.5} \\ c_{1.5} & c_{0.5} & c_{-0.5} & c_{-1.5} \\ c_{2.5} & c_{1.5} & c_{0.5} & c_{-0.5} \\ c_{3.5} & c_{2.5} & c_{1.5} & c_{0.5} \end{pmatrix}.$$

To find the optimal TX-FFE tap weights, a recursive equation is constructed as

$$\boldsymbol{\alpha}(k+1) = \boldsymbol{\alpha}(k) - \lambda \boldsymbol{C}\boldsymbol{\alpha}(k) = \boldsymbol{\alpha}(k) - \lambda \hat{\boldsymbol{\rho}}_{e,d}(k). \tag{6}$$

In each iteration, a small portion of the instant cross-correlation coefficient vector $\lambda \hat{\boldsymbol{\rho}}_{e,d}(k)$ is subtracted from the
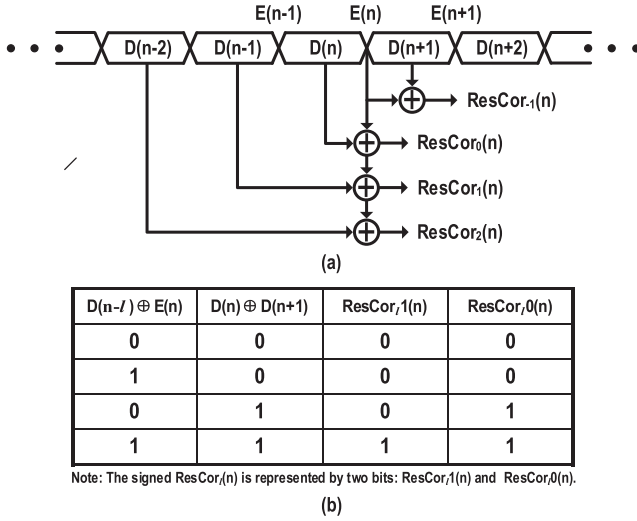
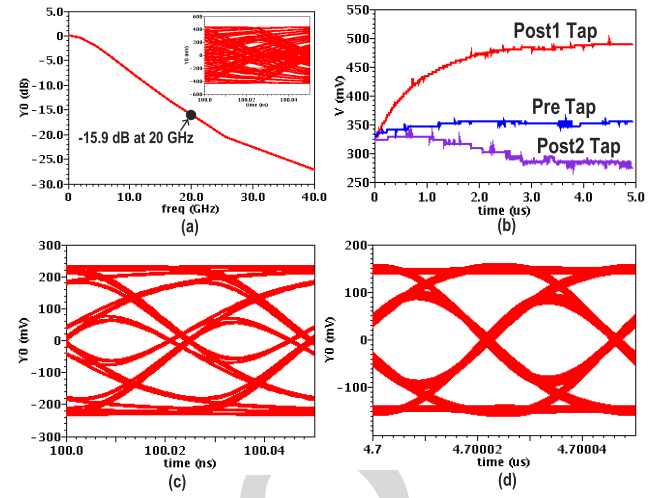Fig. 20.   CD. (a) Operation principle illustration. (b) Function table.

Fig. 21.   Transistor-level simulation of the S-ZF adaptation. (a) Channel frequency response. (b) Convergence process of the TX-FFE tap weights. (c) Eye-diagram with zero TX-FFE tap weights. (d) Eye-diagram with adaptively adjusted TX-FFE tap weights.

tap-weight vector $\boldsymbol{\alpha}(k)$ to make it closer to the targeted value. For the convergence, mathematic analysis indicates that a sufficient condition is to keep the 1-norm of matrix $\boldsymbol{I} - \lambda \boldsymbol{C}$ smaller than 1 (i.e., the maximum absolute column sum is smaller than 1). For any bandwidth-limited channel, the transmitted symbol will spread over multiple symbols at the RX side, thus making the above conditions held. Consequently, a set of optimal tap weights of the TX-FFE can be obtained by the iterative (6). To handle unexpected divergence, range limiters are inserted between the S-ZF and DACs (see Fig. 17) to keep the control codes received by the DACs not larger (or smaller) than the specific maximum (or minimum) values.

Taking sign$[e(k)]$ as the binary quantization of the edge-sampling error, the cross correlation between the sign of the edge-sampling error and received data: sign$[e(k)] \cdot D(k - l)$ can be considered as an instant estimation of $\hat{\rho}_{e,d}(l)$. Hence, the final iterative equation presented in previous part can be obtained [refer to (1)].

D. Implementation of the Edge-Data Correlation-Based S-ZF

Fig. 19 shows the implementation of our S-ZF adaptation algorithm, which contains three identical paths to process the quantized data/edge sequences to produce the desired bias voltages for TX-FFE taps. Here, the main tap weight is pre-fixed to accelerate the convergence speed. In each path, the edge and data streams with proper time shift are applied to a correlation detector (CD) to generate the residual correlation ResCor$_l(n)$, which denotes sign$[e(n)] \cdot D(n - l)$ in (1). These parallel correlation coefficients are first summed and then fed into a 16-bit integrator to execute the iteration of (1), where λ is determined by the subsequent truncation operation. In this design, a set of consecutive 4-bit data/edge of the 1/16-rate demultiplexed data/edge are employed, which ensures that the data/edge information used for equalization adaptation comes from different samplers. This decentralized error collection method reduces the possibility of non-optimal adaptation caused by imperfections, such as fabrication mismatch, duty cycle distortion, and I, Q quadrature error. Fig. 20

further details the operation principle and function table of the CD. Clearly, if there is no transition $[D(n) \oplus D(n + 1) = 0]$, ResCor$_l(n)$ is assigned 0. In case of a data transition $[D(n) \oplus D(n + 1) = 1]$, ResCor$_l(n)$ is assigned +1 or −1 when the polarities of $D(n - l)$ and $E(n)$ are identical $[D(n - l) \oplus E(n) = 0]$ or opposite $[D(n - l) \oplus E(n) = 1]$.

Fig. 21 gives the transistor-level simulation results of the serial link with the S-ZF adaptation, where the control voltage of the RX-CTLE is pre-set to 700 mV, and the dispersive channel is imitated by an LPF with a −15.9 dB loss at 20 GHz. The channel frequency response and the eye-diagram after the channel are shown in Fig. 21(a). Fig. 21(b) describes the convergence process of the TX-FFE tap weights. Fig. 21(c) and (d) shows the eye-diagrams (measured at the output of the RX-CTLE) with zero and adaptively adjusted tap weights, respectively. It can be easily seen that the developed S-ZF adaptation algorithm can gradually tune the TX-FFE tap weights to optimal values, which can effectively optimize the eye opening and eyelid thickness.

V. EXPERIMENTAL RESULTS

The TX and RX chips are fabricated in a 65-nm CMOS process. The chips are mounted on PCBs through wire bonding and they are connected to the testing instruments via SMA connectors and connection cables. Fig. 22 shows the micro-graphs and power breakdown when applying a 1.2-V supply at 40 Gb/s. The TX chip occupies an area of 0.6 mm^2 and consumes a total power of 145 mW with a 400-mV single-end swing. The RX chip occupies 1.92 mm^2 (including the testing circuits) and dissipates 225-mW power (excluding the testing circuits).

A. Transmitter Chip Measurement

The TX output is measured after a channel consisting of a doubled bonding wire, a 4-cm PCB trace, and a 0.5-m
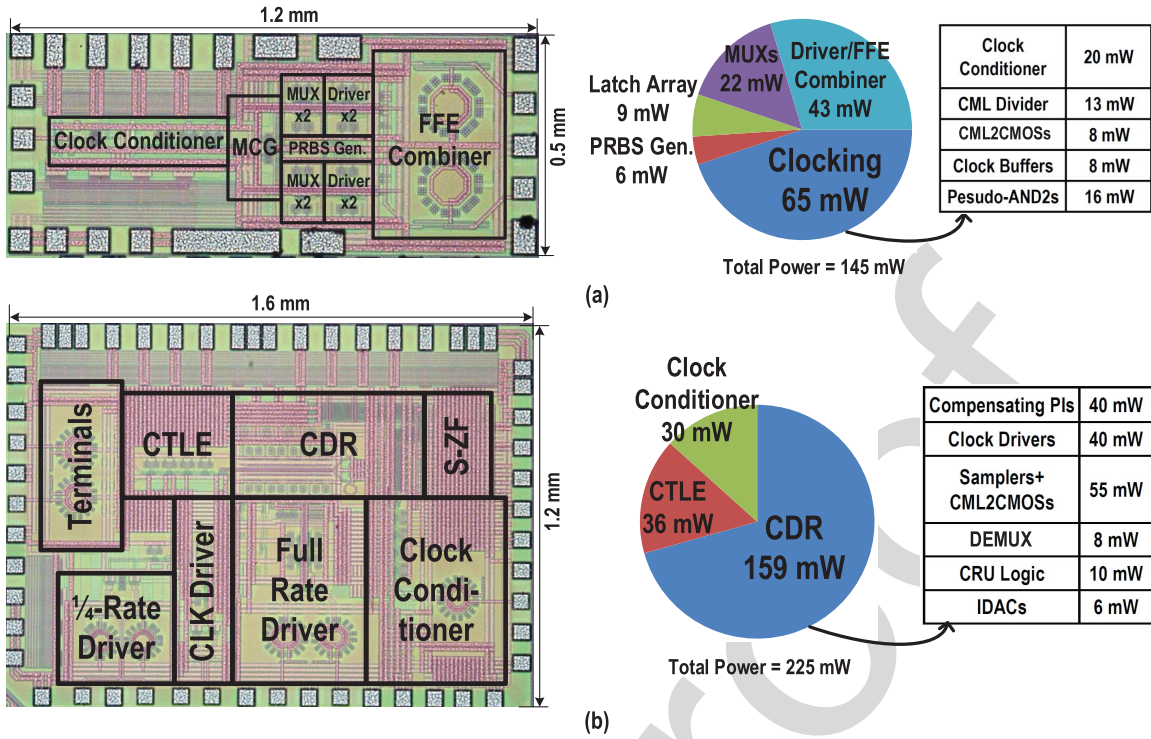
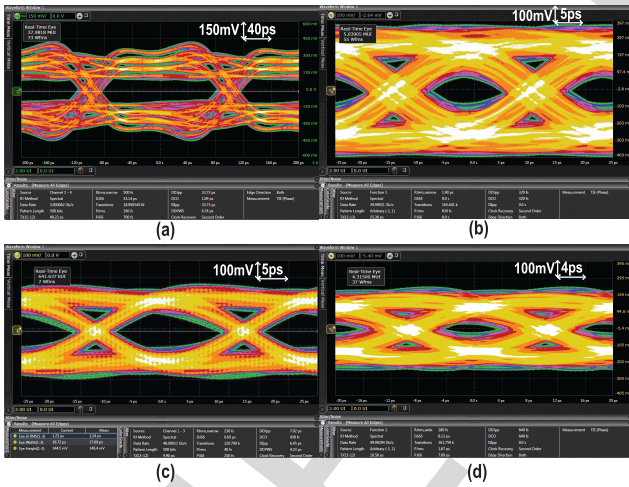Fig. 22. Micrographs and power breakdown of (a) TX chip and (b) RX chip.

Fig. 23. Measured output eye-diagrams of the TX at (a) 5 Gb/s with over equalization, (b) 40 Gb/s without equalization, (c) 40 Gb/s with proper equalization, and (d) 50 Gb/s with proper equalization.
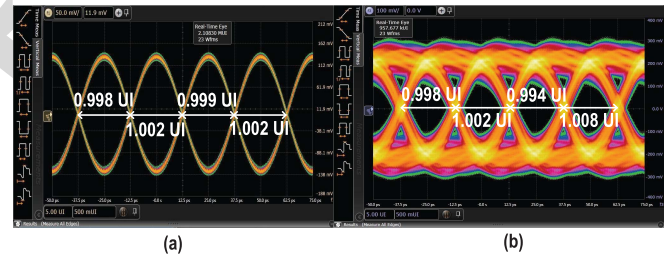

Fig. 24. Measured output eye-diagrams with four separate eyes. (a) Clock pattern. (b) PRBS pattern.

connection cable. Fig. 23(a) shows the over-equalized eye-diagram at 5 Gb/s, where the four sub-levels are contributed by the four FFE taps. Fig. 23(b) and (c) gives the output eye-diagrams at 40 Gb/s before and after applying the four-tap FFE. Obviously, the FFE can significantly improve the eye opening. The eye height and eye width are optimized from 140 mV and 0.45 UI to 180 mV and 0.68 UI, respectively. Moreover, the thickness of the eyelid is dramatically reduced from around 330 to 140 mV. Fig. 23(d) shows the properly compensated eye-diagram at the maximum operation speed of 50 Gb/s. Its eye height and eye width are 50 mV and 0.38 UI. Clearly, a wide operation range from 5 to 50 Gb/s is achieved, which is mainly attributed to the multi-MUX-based FFE implementation. Fig. 24 further shows the TX output with four separate eyes. It can be seen that the horizontal eye widths for both fixed clock and PRBS patterns are almost identical, thus proving that the four sampling phases are properly aligned.

B. Receiver Chip Measurement

The RX standalone measurement results are presented in this part. Fig. 25(a) shows the eye-diagram of the 40-Gb/s input data generated by an Anritsu MP1812A through combining four 10-Gb/s PRBS7 sequences, where the single-end eye height and eye width are around 360 mV and 0.71 UI. Fig. 25(b) shows the eye-diagram of the 10-Gb/s recovered

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

Transmitter Chip				
	[4]	[16]	[20]	This work
Technology (nm)	65	14	65	65
Supply (V)	1.2	N/A	1.2	1.2
Data Rate (Gb/s)	50-64	16-40	38.8-42	5-50
Area (mm²)	1.2 × 1.0	0.215 × 0.13	0.9 × 0.7	1.2 × 0.5
TX Equalization	4-tap FFE	4-tap FFE	5-tap FFE	4-tap FFE
1UI-Delay Gen.	LC-Delay	Multi-MUX	CML-Delay	Multi-MUX
MUX Type	4:1	4:1	N/A	4:1
Data Jitter RJ (ps_rms)	N/A	0.33@28Gb/s 0.51@40Gb/s	N/A	0.23@40Gb/s 0.18@50Gb/s
Data Jitter (ps) TJ (BER=1e-12)	N/A	10.72@28Gb/s 12.89@40Gb/s	15.1@40Gb/s	9.90@40Gb/s 10.58@50Gb/s
Power (mW)	199*	518	135**	145*
Energy Efficiency (pJ/bit)	3.1	12.9	3.4	3.6

*Exclude PLL power consumption, ** Standalone FFE without data serializer.

Receiver Chip			
	[2]	[17]	This work
Technology (nm)	28	22	65
Supply (V)	1.1/0.85	1.07	1.2
Data Rate (Gb/s)	40	4-32	40
Area (mm²)	0.81/Lane*	0.079/Lane	1.92
Sampling Rate	Quarter-Rate	Half-Rate	Quarter-Rate
Equalization Adaptation	Minimum-BER Engine	SS-LMS Engine	Edge-Data Correlation Based S-ZF
Multi-phase Gen.	DLL+PIs	MCDLL+PIs	DIV2+PIs
Jitter Suppression Technique	Split-Path CDR	N/A	Adaptive-BW LPFs
JTOL Amplitude (UI)	0.2@80MHz	0.2@40MHz	0.41@100MHz
JTOL Bandwidth (MHz)	10	20**	20
Power (mW)	630	79.64	225

* Area of whole transceiver, ** Estimated from jitter tolerance results.
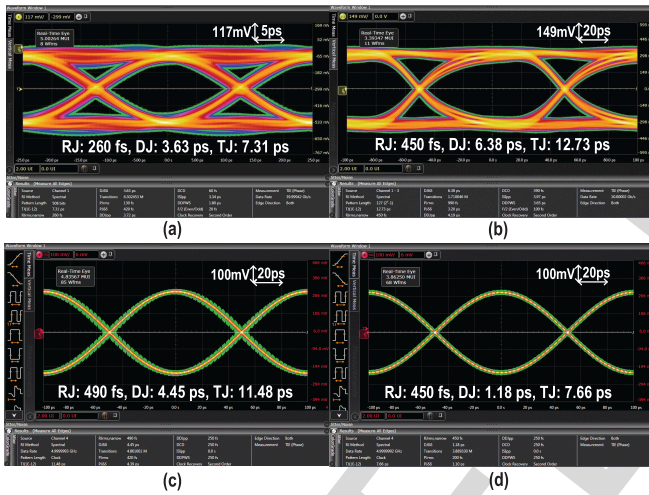

Fig. 25. Measured eye-diagrams for (a) input data at 40 Gb/s, (b) recovered data at 10 Gb/s, (c) recovered edge-sampling clock without LPFs at 5 GHz, and (d) recovered data-sampling clock with LPFs at 5 GHz.
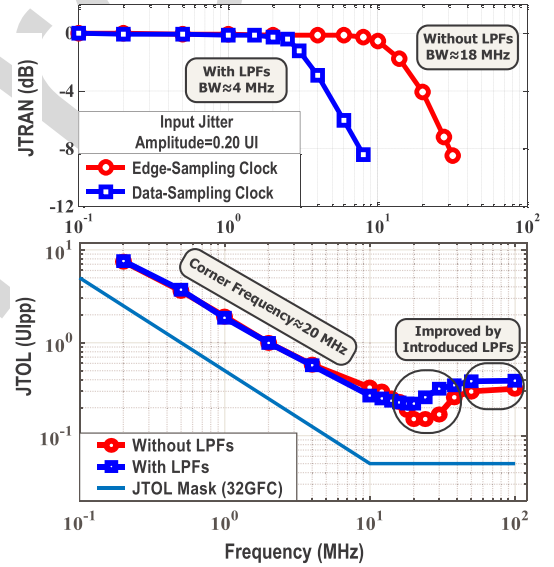

Fig. 26. Measured JTRAN and JTOL with PRBS7 at 28 Gb/s.

data with a total jitter of 12.73 ps. The eye-diagrams of the recovered clocks (divided by 2) for the edge sampling and data sampling are shown in Fig. 25(c) and (d), which reveal that the introduced LPFs can optimize the total jitter from 11.48 to 7.66 ps. To demonstrate the effect of the LPFs with adaptively adjusting bandwidth, the jitter transfer (JTRAN) and JTOL curves are measured using a Tektronix BSA286C with a CDR block. The input peak-to-peak swing is tuned to 800 mV and the control voltage of the CTLE is manually set to 710 mV. The JTRAN curves in Fig. 26 illustrate that the bandwidth of the data-sampling path depending on the LPFs is 4 MHz, which is much smaller than 18 MHz for the edge-sampling path determined by the loop parameters. The measured JTOL in Fig. 26 indicates that the embedded LPFs result in a significant dip attenuation around the corner frequency and improve the JTOL amplitudes apparently at high jitter frequencies. Meanwhile, the adaptively adjusting bandwidth of the LPFs makes them exhibit little effect on the phase-tracking slew rate at low jitter frequencies. Additionally, the corner frequency of the JTOL is about 20 MHz, which is much larger than the JTRAN bandwidth of 4 MHz.

C. Adaptive Equalization Validation

To demonstrate the effectiveness of the developed edge-data cross correlation-based S-ZF algorithm, a chip-to-chip interconnect is constructed, as shown in Fig. 27(a). The outputs of the TX chip and the inputs of the RX chip are separately wire bonded to the two terminals of a 12-cm PCB channel. An auxiliary PCB with a TX chip bonding to a replica channel is manufactured to measure the far-end eye-diagrams. Fig. 27(b) shows the frequency response of the PCB channel,
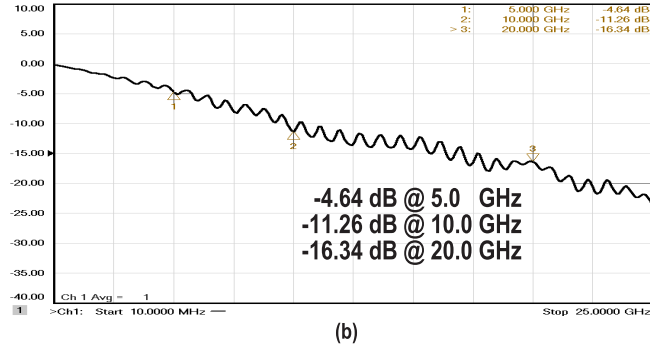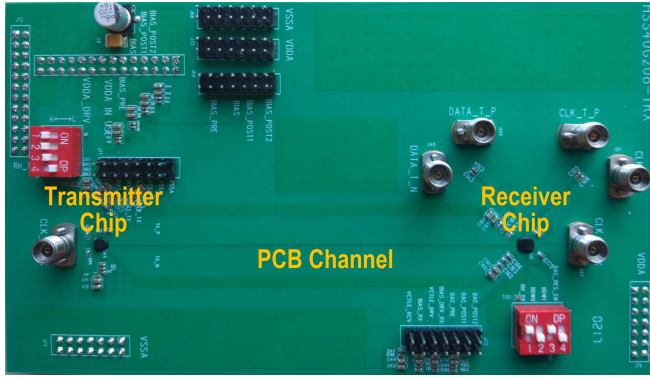
Fig. 27. Constructed chip-to-chip interconnect. (a) PCB photograph. (b) Channel frequency response.
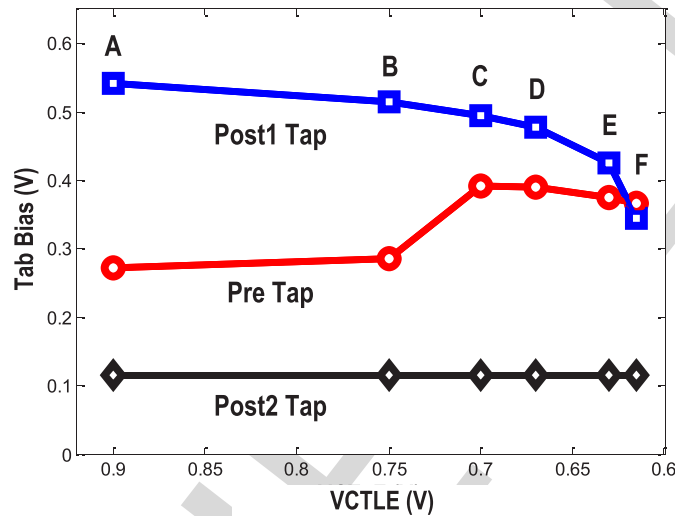

Fig. 28. Adaptively adjusted bias voltages of the TX-FFE with different RX-CTLE control voltages.
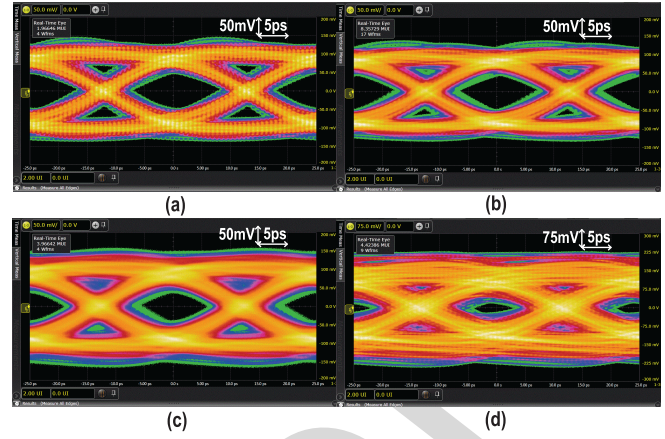

Fig. 29. Measured far-end eye-diagrams for (a) bias condition A, (b) bias condition B, (c) bias condition D, and (d) bias condition F shown in Fig. 28.
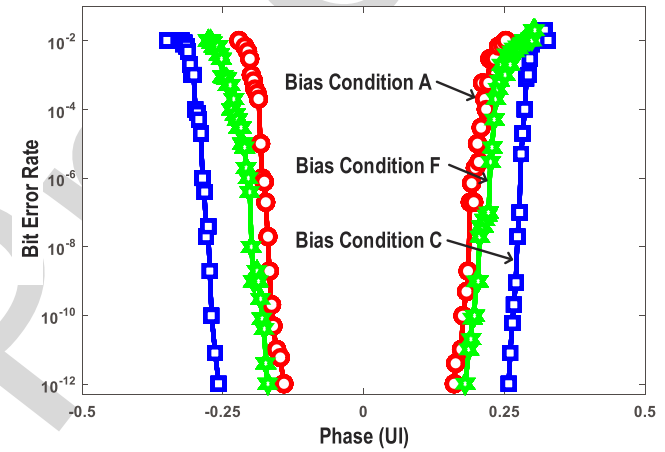

Fig. 30. Measured bathtub curves under different bias conditions shown in Fig. 28.

where the channel loss at the half-baud frequency is over 16 dB. Fig. 28 shows the adaptively adjusted bias voltages of the TX-FFE taps as the control voltage of the RX-CTLE changes from 900 to 615 mV [see the corresponding equalization abilities in Fig. 18(b)] when operating at 40 Gb/s. Fig. 29 shows the far-end eye-diagrams under the bias conditions of A, B, D, and F shown in Fig. 28. As the control voltage of the RX-CTLE is decreased (i.e., improving the high-frequency peaking ability of the RX-CTLE), the TX-FFE bias voltages are adjusted accordingly to decrease the equalization capability of the TX-FFE, thus maintaining the frequency response of the combined TX-FFE, RX-CTLE, and transmission channel close to a flat profile. By detecting the BER while adjusting the sampling positions, the bathtub diagram can be obtained. Fig. 30 shows the measured bathtub curves under the bias conditions of A, C, and F described in Fig. 28. For the balanced equalization coefficient allocation under bias condition C, the horizontal eye opening at BER = 1e-12 achieves 0.51 UI, which is much better than those measured under bias condition A (0.30 UI) and bias condition F (0.35 UI). This proves that a combination scheme of the TX-FFE and RX-CTLE is a good choice for the equalization of the 40-Gb/s link.

D. Performance Summary and Comparison

The performance summary and comparison with previous studies are given in Table I. The results indicate that the TX chip achieves good jitter performance and power efficiency, even in comparison with the TX embedding *LC*-delay-based FFE [4] and the standalone CML-based FFE combiner [20]. This is mainly because of the proposed high-speed 4:1 MUX

and the compact interleaved-latching scheme. For the RX, the maximum tolerable amplitude of sinusoidal jitter at high frequency outperforms the other two, owing to the introduced LPFs and the developed compensating PI. By removing the auxiliary circuits for error information extraction, the proposed edge-data correlation-based S-ZF algorithm not only avoids introducing the capacitance overhead to the critical path, but also helps to optimize the power efficiency.

VI. Conclusion

This paper implements a 40-Gb/s TX and RX chipset over a >16-dB loss PCB channel using a 65-nm CMOS process. The TX utilizes a bandwidth-enhanced 4:1 MUX and an interleaved-retiming latch array to obtain wide operation range, high power efficiency, and small area occupation. By introducing bandwidth-adaptively adjusting LPFs into the clock path for data sampling, the CDR achieves high performance on both low-frequency jitter tracking and high-frequency jitter suppression. To further improve the CDR performance, a TA-based compensating PI is designed to optimize the phase-step uniformity and reduce the phase-spacing shift between edge-sampling and data-sampling clocks. A combined TX-FFE and RX-CTLE is employed to compensate for the channel loss, where a low-cost edge-data correlation-based S-ZF adaptation algorithm is proposed to automatically adjust the TX-FFE's tap weights.

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References

[1] U. Singh et al., "A 780 mW 4 × 28 Gb/s transceiver for 100 GbE gearbox PHY in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3116–3129, Dec. 2014.
[2] R. Navid et al., "A 40 Gb/s serial link transceiver in 28 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 814–827, Apr. 2015.
[3] P.-C. Chiang, J.-Y. Jiang, H.-W. Hung, C.-Y. Wu, G.-S. Chen, and J. Lee, "4×25 Gb/s transceiver with optical front-end for 100 GbE system in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 573–585, Feb. 2015.
[4] M.-S. Chen and C.-K. K. Yang, "A 50–64 Gb/s serializing transmitter with a 4-tap, LC-ladder-filter-based FFE in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1903–1916, Aug. 2015.
[5] J. Lee et al., "Design of 56 Gb/s NRZ and PAM4 SerDes transceivers in CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2061–2073, Sep. 2015.
[6] T. Takemoto et al., "A 25-Gb/s 2.2-W 65-nm CMOS optical transceiver using a power-supply-variation-tolerant analog front end and data-format conversion," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 471–485, Feb. 2014.
[7] B. Welch. (May 2014). *400G Optics-Technologies, Timing, and Transceivers*. Accessed: Oct. 22, 2016. [Online]. Available: http://www.ieee802.org/3/bs/public/14_05/welch_3bs_01_0514.pdf
[8] *InfiniBand Roadmap*. Accessed: Oct. 22, 2016. [Online]. Available: http://www.infinibandta.org/content/pages.php?pg=technology_overview
[9] P.-C. Chiang, H.-W. Hung, H.-Y. Chu, G.-S. Chen, and J. Lee, "60 Gb/s NRZ and PAM4 transmitters for 400 GbE in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 42–43.
[10] H. Tao et al., "40–43-Gb/s OC-768 16:1 MUX/CMU chipset with SFI-5 compliance," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2169–2180, Dec. 2003.
[11] A. A. Hafez, M.-S. Chen, and C.-K. K. Yang, "A 32–48 Gb/s serializing transmitter using multiphase serialization in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 763–775, Mar. 2015.
[12] B. Raghavan et al., "A sub-2 W 39.8–44.6 Gb/s transmitter and receiver chipset with SFI-5.2 interface in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3219–3228, Dec. 2013.
[13] K. Kanda et al., "A single-40 Gb/s dual-20 Gb/s serializer IC with SFI-5.2 interface in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3580–3589, Dec. 2009.
[14] S. Kaeriyama et al., "A 40 Gb/s multi-data-rate CMOS transmitter and receiver chipset with SFI-5 interface for optical transmission systems," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3568–3579, Dec. 2009.
[15] P. Chiang, W. J. Dally, M. J. E. Lee, R. Senthinathan, Y. Oh, and M. A. Horowitz, "A 20-Gb/s 0.13-μm CMOS serial link transmitter using an LC-PLL to directly drive the output multiplexer," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 1004–1011, Apr. 2005.
[16] J. Kim et al., "A 16-to-40 Gb/s quarter-rate NRZ/PAM4 dual-mode transmitter in 14 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 60–61.
[17] T. Musah et al., "A 4–32 Gb/s bidirectional link with 3-tap FFE/6-tap DFE and collaborative CDR in 22 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3079–3090, Dec. 2014.
[18] C. Thakkar, L. Kong, K. Jung, A. Frappe, and E. Alon, "A 10 Gb/s 45 mW adaptive 60 GHz baseband in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 952–968, Apr. 2012.
[19] J. Jaussi et al., "A 205 mW 32 Gb/s 3-tap FFE/6-tap DFE bidirectional serial link in 22 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 440–441.
[20] M.-S. Chen, Y.-N. Shih, C.-L. Lin, H.-W. Hung, and J. Lee, "A fully-integrated 40-Gb/s transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 627–640, Mar. 2012.
[21] A. Cavaciuti et al. (Jul. 2014). *CAUI4 Channel Loss Variation Due to Temperature*. Accessed: Oct. 22, 2016. [Online]. Available: http://www.ieee802.org/3/bm/public/jul14/interim/tooyserkani_01_0714_optx.pdf
[22] H. Wang and J. Lee, "A 21-Gb/s 87-mW transceiver with FFE/DFE/analog equalizer in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 909–920, Apr. 2010.
[23] D. Cui et al., "A dual-channel 23-Gbps CMOS transmitter/receiver chipset for 40-Gbps RZ-DQPSK and CS-RZ-DQPSK optical transmission," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3249–3260, Dec. 2012.
[24] C. Menolfi et al., "A 28 Gb/s source-series terminated TX in 32 nm CMOS SOI," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 334–335.
[25] X. Zheng et al., "A 5–50 Gb/s quarter rate transmitter with a 4-tap multiple-MUX based FFE in 65 nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2016, pp. 305–308.
[26] R. Reutemann et al., "A 4.5 mW/Gb/s 6.4 Gb/s 22+1-lane source synchronous receiver core with optional cleanup PLL in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2850–2860, Dec. 2010.
[27] B. Casper and F. O'Mahony, "Clocking analysis, implementation and measurement techniques for high-speed data links—A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 1, pp. 17–39, Jan. 2009.
[28] N. Kalantari and J. F. Buckwalter, "A multichannel serial link receiver with dual-loop clock-and-data recovery and channel equalization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 2920–2931, Nov. 2013.
[29] L. Rodoni, G. von Buren, A. Huber, M. Schmatz, and H. Jackel, "A 5.75 to 44 Gb/s quarter rate CDR with data rate selection in 90 nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1927–1941, Jul. 2009.
[30] M. Hossain et al., "A 4×40 Gb/s quad-lane CDR with shared frequency tracking and data dependent jitter filtering," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[31] M. Pozzoni et al., "A multi-standard 1.5 to 10 Gb/s latch-based 3-tap DFE receiver with a SSC tolerant CDR for serial backplane communication," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1306–1315, Apr. 2009.
[32] J. W. M. Bergmans, *Digital Baseband Transmission and Recording*. Dordrecht, The Netherlands: Springer, 1996.
[33] H. Higashi et al., "A 5–6.4-Gb/s 12-channel transceiver with pre-emphasis and equalization," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 978–985, Apr. 2005.
[34] K. Krishna et al., "A multigigabit backplane transceiver core in 0.13-μm CMOS with a power-efficient equalization architecture," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2658–2666, Dec. 2005.

[35] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4th ed. Pearson, 2006.

[36] H. Kimura *et al.*, "A 28 Gb/s 560 mW multi-standard SerDes with single-stage analog front-end and 14-tap decision feedback equalizer in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3091–3103, Dec. 2014.

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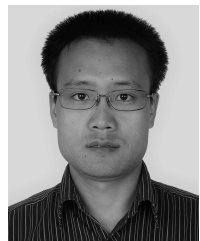
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